Study of Inherent Gate Coupling Nonuniformity of InAs/GaSb Vertical TFETs

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***Abstract*— An electrostatic nonuniformity in the cantilever vertical tunneling FETs intrinsically exists in the InAs/GaSb junction to InAs cantilever transition region. The effects of the coupling ratio (CR) nonuniformity are investigated in this paper. The results show that the switching characteristics are degraded by the CR nonuniformity, especially in the case of large InAs/GaSb band offset. This paper also reveals that the nonuniformity in InAs/GaSb vertical tunneling FETs can be mitigated with the optimized band offset of heterojunction, scaling of oxide thickness, and acute angle etching profile.**

***Index Terms*— Band offset, coupling ratio (CR), InAs/GaSb tunneling FETs (TFETs), nonuniformity, quantum confinement.**

I. Introduction

TUNNELING FETs (TFETs) have been extensively studied due to the potential for low-power logic applications [1]–[14]. Table I shows the comparison of double-gate TFETs with different materials. InAs/GaSb heterojunction is one of the promising materials with low supply voltage. Its low tunneling barrier can lead to high ON-current, meanwhile sustain steep switching characteristics. Therefore, InAs/GaSb TFET is regarded as a candidate for high-performance logic device for post-silicon CMOS application.

Previous works have shown that the surface states of the exposed InAs surface enhance the nonuniformity issue of the vertical InAs/GaSb TFETs, and the dual-metal gate can be used to suppress the tunneling onset voltage nonuniformity caused by surface states and other factors [15]. In this paper, the nonuniformity factor arising from the intrinsic device geometry of cantilever-type InAs/GaSb TFET is discussed. The band offset of InAs/GaSb affects the uniformity of threshold voltage; hence, the quantum confinement effect [16] is also included in this investigation. The detail mechanism will be discussed later. Fig. 1(a) shows the structure used for the simulation, and the band diagram of cutline is shown in Fig. 1(b).

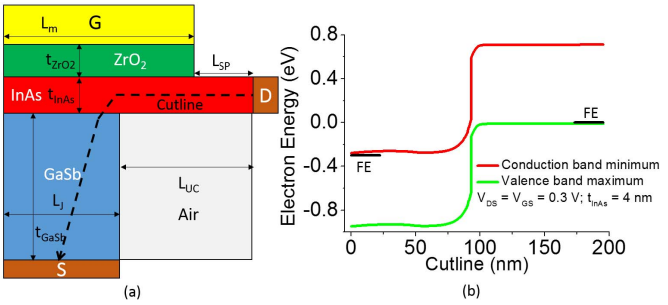

Fig. 1. (a) Simulated device structure. $L_G = 80$ nm, $L_{SP} = 50$ nm, undercut $L_{UC} = 90$ nm, junction width $L_J = 40$ nm, default ZrO_2 thickness $t_{ZrO2} = 10$ nm, GaSb thickness $t_{GaSb} = 100$ nm, n-type doping concentration in InAs $N_D = 1 \times 10^{17}$ cm^{-3}, p-type doping concentration in GaSb $N_A = 1 \times 10^{19}$ cm^{-3}, and work function of gate metal is 4.7 eV. (b) Band diagram along cutline A in (a).

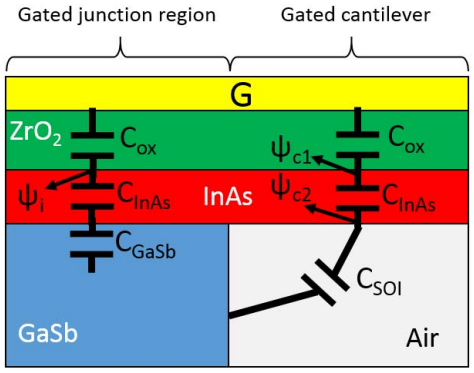

Fig. 2. Schematic of the capacitance in the cantilever-type vertical TFETs. C_{OX} is the gate oxide capacitance, C_{InAs} is the depletion capacitance of n-InAs, C_{GaSb} is the depletion capacitance of p+GaSb, and C_{SOI} is the capacitance across air, and hence can be assumed as zero.

Fig. 2 shows the simplified schematic of capacitances in cantilever vertical InAs/GaSb TFETs. For cantilever-type vertical TFETs, the gated InAs cantilever behaves like a parasitic ultrathin body (UTB) MOSFET. The coupling ratio [(CR), defined as the ratio of potential change in InAs channel over gate voltage change $\Delta\psi/\Delta V_G$] of the gated InAs cantilever

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TABLE I
COMPARISON OF DOUBLE-GATE TFETS WITH DIFFERENT MATERIALS

	Gate length	Body thickness	Voltage	On-current	I_{ON}/I_{OFF} ratio	Subthreshold swing	Method
WSe_2 [9]	15 nm	Mono-layer	V_{DS} = 0.5 V	127 μA/μm	-	>14 mV/dec	NEGF
WTe_2 [9]	15 nm	Mono-layer	V_{DS} = 0.5 V	4.6 μA/μm	-	>10 mV/dec	NEGF
MoS_2 [9]	15 nm	Mono-layer	V_{DS} = 0.5 V	0.3 μA/μm	-	-	NEGF
Graphene [10]	40 nm	Bi-layer	V_{DS} = 0.1 V	45 μA/μm	$>10^4$	10 mV/dec	NEGF
Phosphorene [11]	15 nm	Bi-layer	V_{DS} = 0.5 V	1000 μA/μm	10^6	~20 mV/dec	NEGF
GaN/InN/GaN [12]	20 nm	12 nm	V_{DS} = 0.5 V	44 μA/μm	-	25 mV/dec	TCAD/NEGF
InAs [13]	20 nm	7 nm	V_{DS} = 0.2 V	110 μA/μm	$>10^4$	<60 mV/dec	NEGF
InSb [14]	40 nm	5 nm	V_{DS} = 0.5 V	333.1 μA/μm	$>10^5$	19.9 mV/dec	NEGF
InAs/GaSb [14]	40 nm	5 nm	V_{DS} = 0.5 V	752 μA/μm	$>10^7$	10.6 mV/dec	NEGF

can be approximated as

$$\mathrm{CR}_c = \frac{\Delta\psi_{c1}}{\Delta V_G} = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + \frac{C_{\mathrm{InAs}}C_{\mathrm{SOI}}}{C_{\mathrm{InAs}}+C_{\mathrm{SOI}}}} \sim \frac{\Delta\psi_{c2}}{\Delta V_G} = \frac{\frac{C_{\mathrm{InAs}}C_{\mathrm{ox}}}{C_{\mathrm{InAs}}+C_{\mathrm{ox}}}}{C_{\mathrm{SOI}} + \frac{C_{\mathrm{InAs}}C_{\mathrm{ox}}}{C_{\mathrm{InAs}}+C_{\mathrm{ox}}}} \sim 1 \quad (1)$$

where CR_c is the CR of mid gated cantilever. C_{SOI} is assumed to be zero by the nature of UTB structure. Potential across the mid of the InAs cantilever from ZrO_2/InAs interface to InAs/air interface is about the same value $\psi_{C1} = \psi_{C2}$.

For gated InAs/GaSb junction region, the potential of the interior region ψ_i refers to the potential near the InAs/ZrO_2 interface (the initial tunneling location in the interior region). The CR of the interior-gated InAs/GaSb junction region can be expressed as

$$\mathrm{CR}_i = \frac{\Delta\psi_i}{\Delta V_G} = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + \frac{C_{\mathrm{InAs}}C_{\mathrm{GaSb}}}{C_{\mathrm{InA}}+C_{\mathrm{GaSb}}}} \sim \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\mathrm{InAs}}} < 1 \quad (2)$$

where the depletion capacitance of GaSb C_{GaSb} is very large owing to the heavy doping in GaSb. It is clear that an inherent CR nonuniformity caused by the device geometry exists in the cantilever vertical TFET. Furthermore, the nonuniformity between the junction and the cantilever affects the potential at the edge of the junction and results in different tunneling onset voltages (the gate voltage at which the conduction band edge of InAs starts to overlap the valence band edge of GaSb). Here, screen effect by mobile charge is neglected in the simple analysis above, because the valence band is nearly fully occupied and the conduction band is nearly empty at onset in a well-designed TFET. In other words, InAs should be depleted. In addition, t_{InAs} is small.

II. DEVICE SIMULATION

As shown in Fig. 1(a), the simulation structure contains InAs QW on bulk GaSb with 10-nm ZrO_2 ($\varepsilon_{\mathrm{ox}} = 23.2$) as gate oxide. Different thicknesses of InAs QW are considered, ranging from 8 to 4 nm. The first sub-band of InAs QW was calculated by solving the Schrodinger equation with effective masses corrected with nonparabolicity [17]. The calculated sub-band energy then entered into the Sentaurus simulator as the conduction band minimum (CBM) of InAs.

TABLE II
SUMMARY OF BAND OFFSETS

t_{InAs} (nm)	m^*_{InAs}	InAs E_G (eV)	Band offset (meV)
8	0.038	0.512	2
7	0.04	0.534	24
6	0.043	0.564	54
5	0.0464	0.608	98
4	0.0513	0.669	159

Table II summarizes the band offset between the CBM of InAs and the valence band maximum (VBM) of GaSb with different values of t_{InAs}. In the simulation, the WKB-based dynamic nonlocal path band-to-band tunneling model was enabled [18], [19]. In the InAs/GaSb junction, the tunneling path between the conduction band of InAs and the light hole band of GaSb is dominated. Therefore, effective mass of InAs conduction band m^*_{InAs} and effective mass of GaSb light hole band need to be considered. The m^*_{InAs} values with different values of t_{InAs} are listed in Table II. The light hole effective mass of GaSb used in this paper is 0.05. Degeneracy of the tunneling is 2. The electron–phonon scattering was not considered in this paper. Neglect of electron–phonon scattering might causes overrating of the device electrical characteristics; however, it does not cloud the conclusion. To avoid the effect of drain-induced barrier lowering at the tunneling junction, we design the gated InAs cantilever having rather large gate length to avoid short channel effect

$$l_g \geq 3\left(t_{\mathrm{ox}}\frac{\varepsilon_s}{\varepsilon_{\mathrm{ox}}} + t_s\right). \quad (3)$$

The gate length of the gated InAs cantilever is set as 40 nm. The choice of dimensions helps to focus on the electrostatic analysis rather than other effects. The default V_{DD} is set as 0.3 V.

III. SIMULATION RESULTS AND DISCUSSION

A. Onset Voltage Nonuniformity

Fig. 3(a) shows the I_{DS}–V_{GS} curves with different values of t_{InAs}. The switching characteristics degrade with smaller t_{InAs}. Fig. 3(b) shows the I_{DS}–V_{DS} curves with different V_{GS} biases for 8 nm t_{InAs} and 4 nm t_{InAs}, respectively. Under the same $V_{\mathrm{GS}} - V_{\mathrm{TH}}$ bias, it can be seen that the

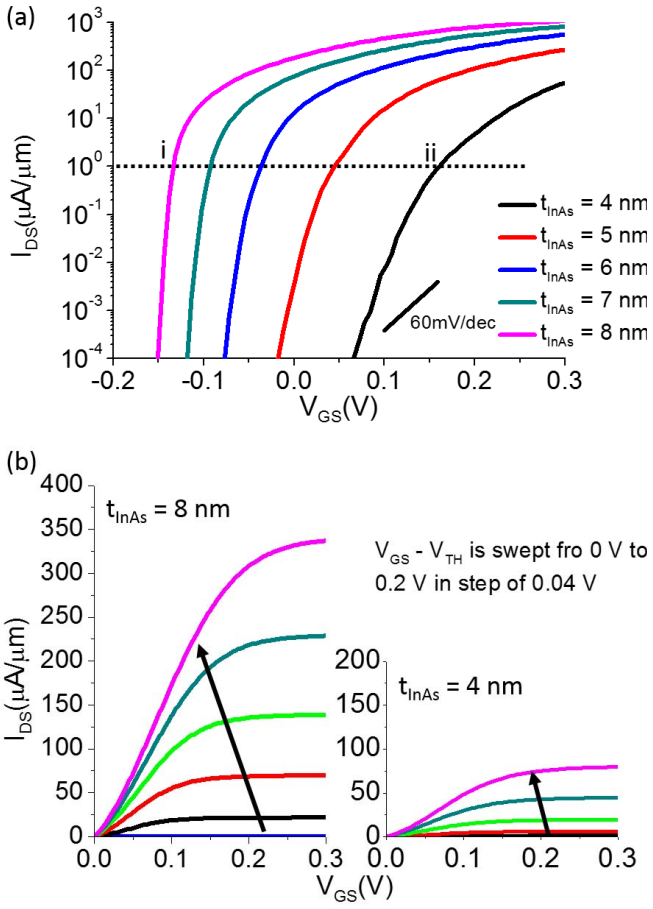

Fig. 3. (a) I_{DS}–V_{GS} curves with different InAs thicknesses. (b) I_{DS}–V_{DS} curves with $t_{InAs} = 8$ nm and 4 nm, respectively.

8-nm t_{InAs} case has higher ON-current and lower ON-resistance due to the smaller tunneling barrier. The V_{TH} is referred to the gate voltage with $I_{DS} = 0.1\ \mu A/\mu m$. Fig. 4 shows the band diagrams along cutlines in the interior junction region and in the middle of the gated InAs cantilever. Fig. 4(a) and (b) shows the cases of 4-nm InAs QW under flat band and $I_{DS} = 1\ \mu A/\mu m$, respectively. It should be noted that potential of the cantilever and the interior junction region are very close at the flat band condition of GaSb. As a result, the flat-band voltage V_{FB} for both the cantilever region and the interior region is about the same. Fig. 4(b) shows the fact that CR_c is larger than CR_i, which makes the CBM of the cantilever lower than the CBM of the interior region when positive V_{GS}–$V_{FB}$is applied. Hence, tunneling onset voltage of the junction edge is lower than the onset voltage at the interior region. The onset voltage nonuniformity reflects the degraded switching characteristics of the I_{DS}–V_{GS} curve of 4-nm InAs case, as shown in Fig. 3(a). The nonuniformity of the tunneling onset voltage can be derived in a simplified formula as below. The tunneling onset voltage for cantilever $V_{th,c}$, interior $V_{th,i}$, and edge $V_{th,e}$ can be formulated as

$$V_{th,\upsilon} - V_{FB} = \frac{1}{CR_\upsilon} \times V_{offset}; \quad \upsilon = c, i \tag{4}$$

$$V_{th,e} = \gamma\, V_{th,c} + (1-\gamma)\, V_{th,i}; \quad 0 < \gamma < 1 \tag{5}$$

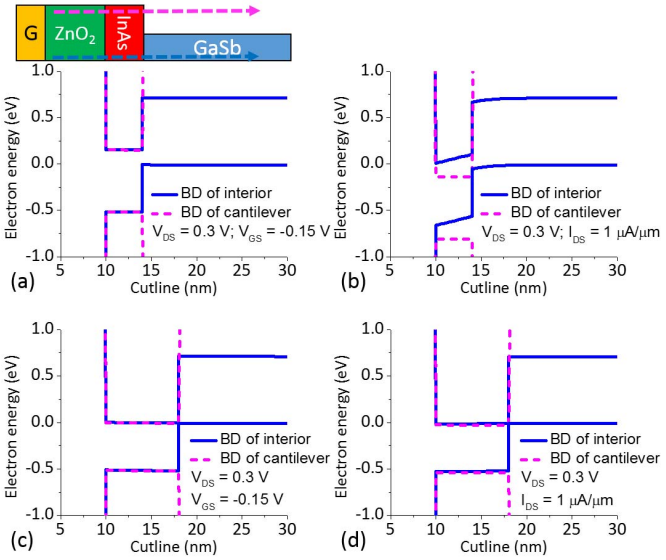

Fig. 4. Comparison of band diagrams in the interior of the junction (blue cutline) and in the middle of the cantilever (purple cutline). (a) $t_{InAs} = 4$ nm and in flat band condition. (b) $t_{InAs} = 4$ nm and $I_{DS} = 1\ \mu A/\mu m$. (c) $t_{InAs} = 8$ nm and in flat band condition. (d) $t_{InAs} = 8$ nm and $I_{DS} = 1\ \mu A/\mu m$.

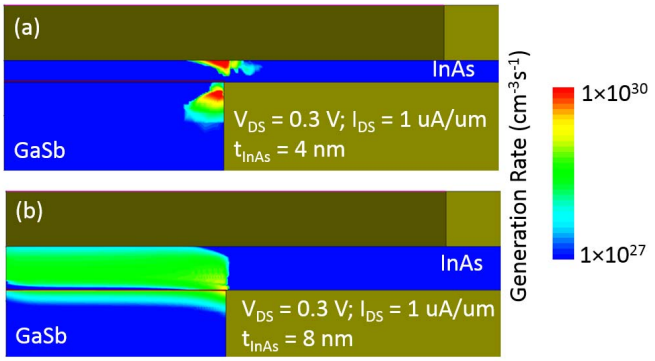

Fig. 5. Carrier generation rate contour plots for (a) $t_{InAs} = 4$ nm and (b) $t_{InAs} = 8$ nm corresponding to points ii and i in Fig. 3, respectively.

where V_{offset} is the band offset. The cantilever onset voltage $V_{th,c}$ only refers as the CBM of InAs becoming lower than VBM of GaSb. No tunneling actually occurred in the cantilever region. The γ value is used to address the fact that $V_{th,e}$ is a value between $V_{th,i}$ and $V_{th,c}$. The onset voltage difference across junction from edge to interior ΔV_{th} can be derived as

$$\Delta V_{th} = V_{th,e} - V_{th,i} = \gamma \left(\frac{1}{CR_c} - \frac{1}{CR_i} \right) V_{offset}. \tag{6}$$

From (6), it is clear that the band offset can affect ΔV_{th}. Fig. 4(c) and (d) shows the case of 8-nm InAs under flat band and $I_{DS} = 1\ \mu A/\mu m$, respectively. Comparing with the 4-nm InAs case, the band offset of the 8-nm InAs case is reduced to 2 meV and ΔV_{th} is also reduced as indicated in (6). As shown in Fig. 4(d), the difference of CBM between the cantilever and the interior region is very small. Thus, the CR nonuniformity is minimized in this case. This results in the sharp subthreshold slope curve in Fig. 3(a).

Fig. 5 shows the tunneling-induced carrier generation rate contours for the $t_{InAs} = 4$ nm case [Fig. 5(a)] and the case

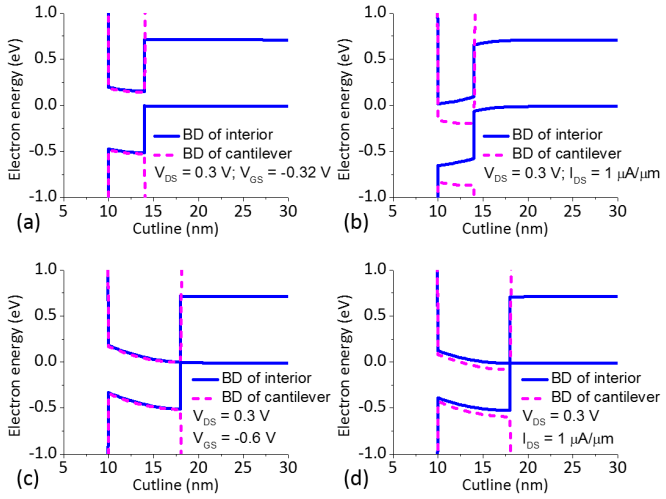

Fig. 6. Band diagrams in the interior of the junction (blue cutline in Fig. 4) and in the middle of the cantilever (purple cutline in Fig. 4) for $N_D = 4 \times 10^{18}$ cm^{-3}. (a) $t_{\mathrm{InAs}} = 4$ nm and in flat band condition. (b) $t_{\mathrm{InAs}} = 4$ nm and $I_{\mathrm{DS}} = 1\ \mu$A/μm. (c) $t_{\mathrm{InAs}} = 8$ nm and in flat band condition. (d) $t_{\mathrm{InAs}} = 8$ nm and $I_{\mathrm{DS}} = 1\ \mu$A/μm.

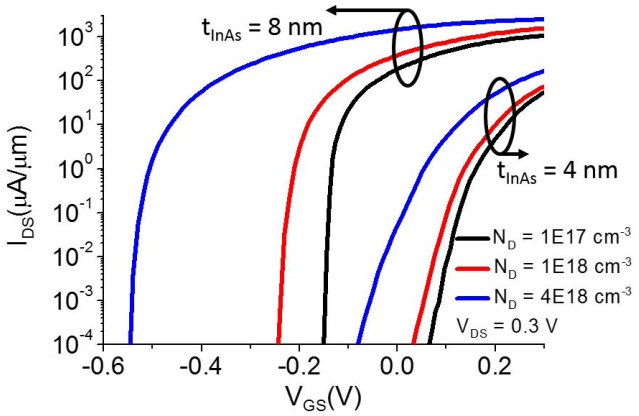

Fig. 7. I_{DS}–V_{GS} curves with different values of N_D for $t_{\mathrm{InAs}} = 4$ and 8 nm.

of $t_{\mathrm{InAs}} = 8$ nm [Fig. 5(b)]. The contours show electron generation rate in the InAs region and the hole generation rate in the GaSb region. These plots are for $I_{\mathrm{DS}} = 1\ \mu$A/μm, as the horizontal line indicates in Fig. 3(a). Fig. 5(a) shows that electrons only tunnel from the top-left corner of the valence band (generating holes) of GaSb into the conduction band (generating electrons) of the InAs QW. On the other hand, Fig. 5(b) manifests that both the interior and the edge regions contribute to the tunneling current, which implies a uniform turn-ON over the whole InAs/GaSb junction. These plots are consistent with the results shown in Fig. 4.

The onset voltage nonuniformity also exists in higher InAs doping cases, as shown in Fig. 6. Fig. 7 shows the I_{DS}–V_{GS} curves for $t_{\mathrm{InAs}} = 4$ and 8 nm with three channel doping densities. The switching characteristics can be improved by reducing the band offset for all the three N_D cases.

B. Coupling Ratio Matching

Besides engineering, the band offset value in (6) by InAs thickness modulation or including ternary compounds (InGaAs and AlGaSb), methods like CR matching, and dual-metal

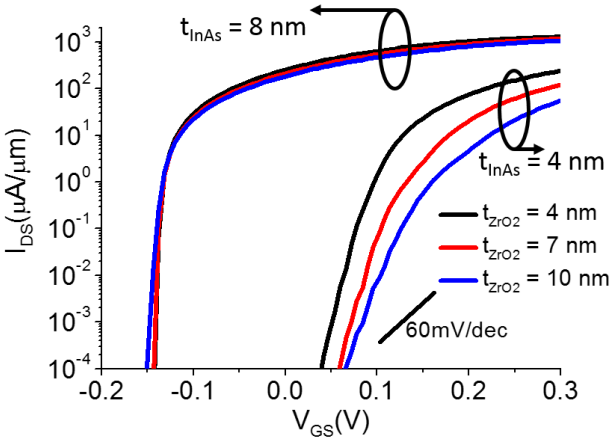

Fig. 8. I_{DS}–V_{GS} curves with different ZrO_2 thicknesses.

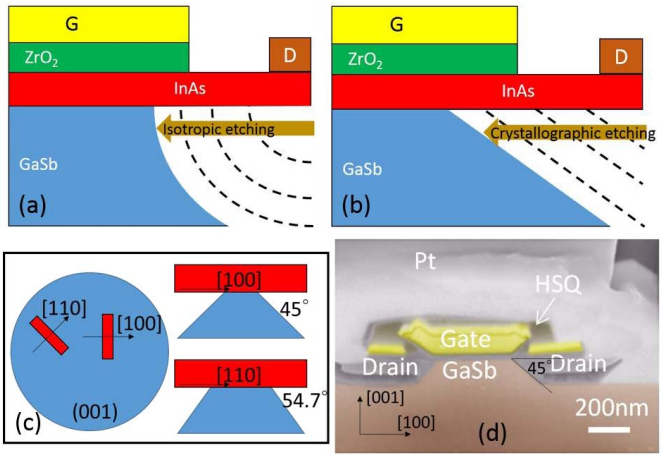

Fig. 9. (a) Schematic of isotropic lateral etching, edge angle in this case is 90 degree. (b) Schematic of crystallographic etching, edge angle is dependent on the slowest crystalline plane of etching. (c) Device orientation also affects the etching edge angle. (d) SEM picture of postlateral-etching TFET.

structure [15] can also be used to improve the subthreshold slope. Here the method for CR matching is discussed as follows. The CR of interior CR_i can approach 1 when the oxide thickness is aggressively scaled down, and then makes the CR term $(1/\mathrm{CR}_c) - (1/\mathrm{CR}_i)$ in (6) to be reduced. Fig. 8 shows the I_{DS}–V_{GS} curves with different values of t_{ZnO2}. The subthreshold slope is improved when the oxide thickness is scaled down.

On the other hand, CR matching can also be achieved by lateral etching profile optimization, as shown in Fig. 9 [21], [22]. The acute etching profile can be obtained by proper etching and device orientation. In Fig. 9(d), the acute etching profile of 45° was obtained by diluted HCl (8%), etching with device orienting along [100] direction as reference [22] suggested. The acute etching profile can increase C_{SOI}. Therefore, CR_c turns lower and closer to CR_i. The I_{DS}–V_{GS} curves with different junction edge angles are shown in Fig. 10. With acute angle, the switching characteristics dose show improvement. Fig. 11 shows the carrier generation contour plots with $V_{\mathrm{GS}} = 0.1$ V. Fig. 11(b) exhibits

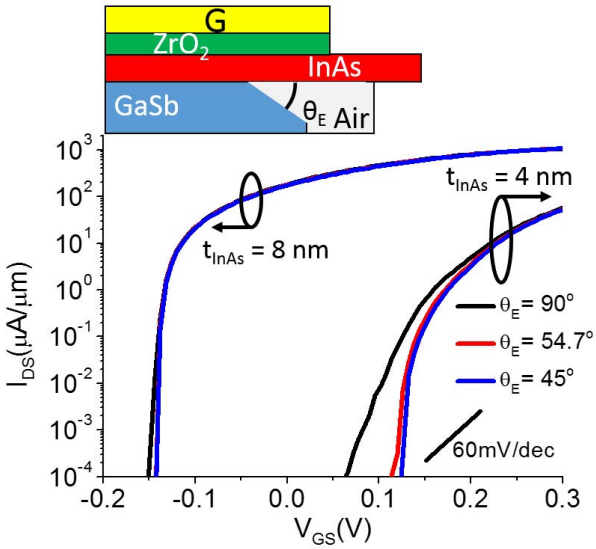

Fig. 10. I_{DS}–V_{GS} curves with different undercut edge angles θ_E.

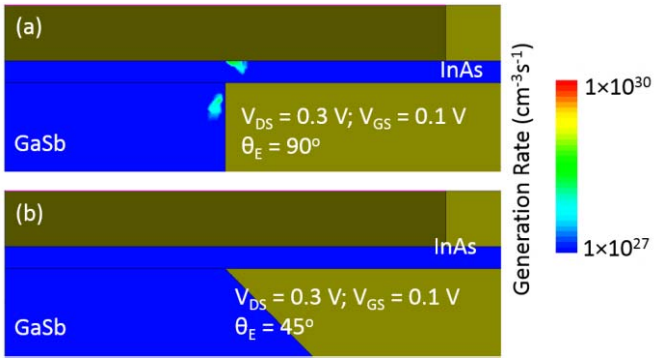

Fig. 11. Carriers generation rate contour plots for (a) $\theta_E = 90°$ and (b) $\theta_E = 45°$. The gate bias is referred to $V_{GS} = 0.1$ V.

the suppression of the early turn-ON at the edge by acute etching profile. This is consistent with the results shown in Fig. 10.

IV. Conclusion

The nonuniform tunneling onset voltage across the junction region of InAs/GaSb cantilever-type TFET leads to the degradation of the I_{DS}–V_{GS} curve steepness. The nonuniform CR between the junction region and the cantilever region is a main contribution. With proper choice of InAs thickness, the band offset of InAs/GaSb heterojunction can be optimized to mitigate the nonuniformity of tunneling onset voltage. The high-k oxide thickness scaling and GaSb substrate etching profile can also be used to improve the CR uniformity, so that a steeper switching characteristic can be achieved.

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