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Compiler Transformations Meet CPU Clock Modulation and Power Capping

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Motivation

- Bounded power consumption to achieve exascale computing
- Various power management techniques exist for applications energy control
- Impact of power management techniques on compiler transformations

CPU Clock Modulation

- Write Specific Value to IA32_CLOCK_MODULATION (0x19a) MSR
- Modify /dev/cpu/cpu{0:15}/msr with root privilege
- Invoke wrmsr inline assembly from applications using added System Call

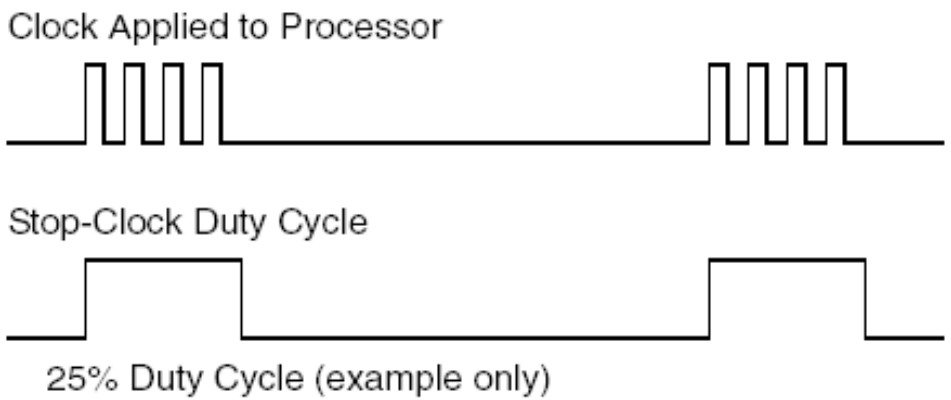


Figure: CPU Clock Modulation. Sample Modulation with 25% Duty Cycle. (Source: IA-32 Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide)

Available Frequencies

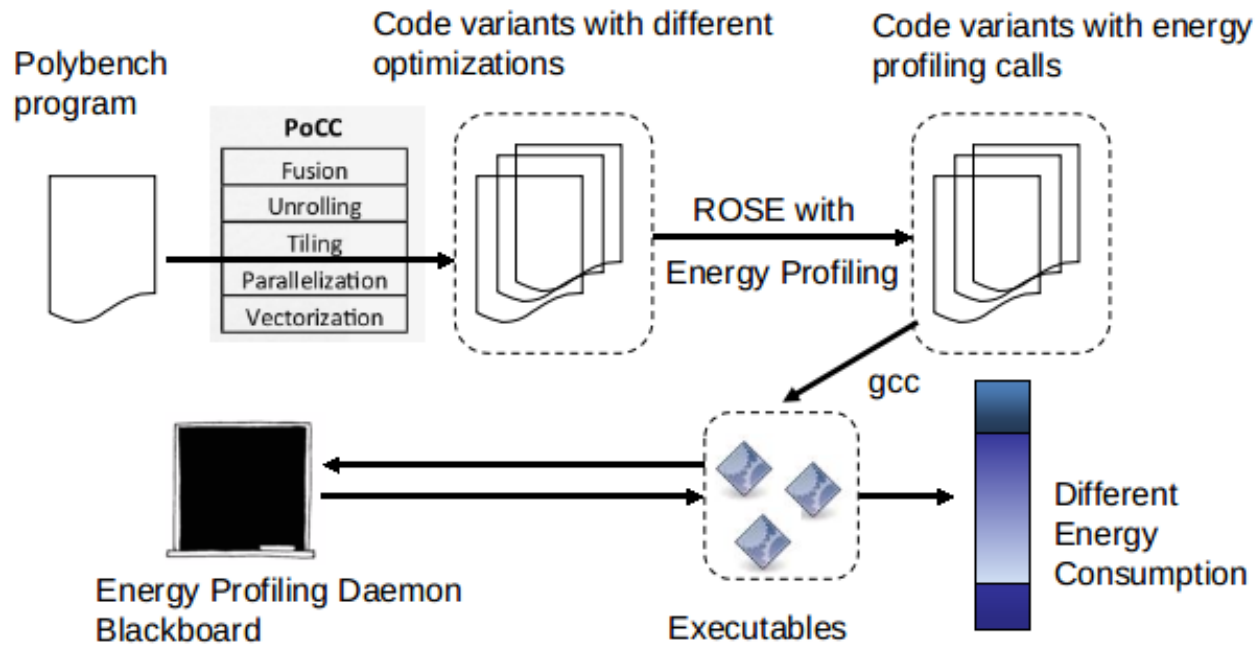
Duty Cycle Level	*Binary*	*Decimal*	*Hexadecimal*	*Effective Frequency*
1	10001B	17	11H	6.25%
2	10010B	18	12H	12.5%
3	10011B	19	13H	18.75%
4	10100B	20	14H	25%
5	10101B	21	15H	31.25%
6	10110B	22	16H	37.5%
7	10011B	23	17H	43.75%
8	11000B	24	18H	50%
9	11001B	25	19H	56.25%
10	11010B	26	1AH	63.5%
11	11011B	27	1BH	69.75%
12	11100B	28	1CH	75%
13	11101B	29	1DH	81.25%
14	11110B	30	1EH	87.5%
15	11111B	31	1FH	93.75%
16	00000B	0	00H	100%

Power Capping and Measurement on Intel Architecture

- Based on RAPL (Running Average Power Limit)
- Power Capping - Write MSR_PKG_RAPL_POWER_LIMIT MSR
- Power Measurement - Read MSR_PKG_ENERGY_STATUS MSR (Use RCRTool to avoid overflow)

Compiler Transformations

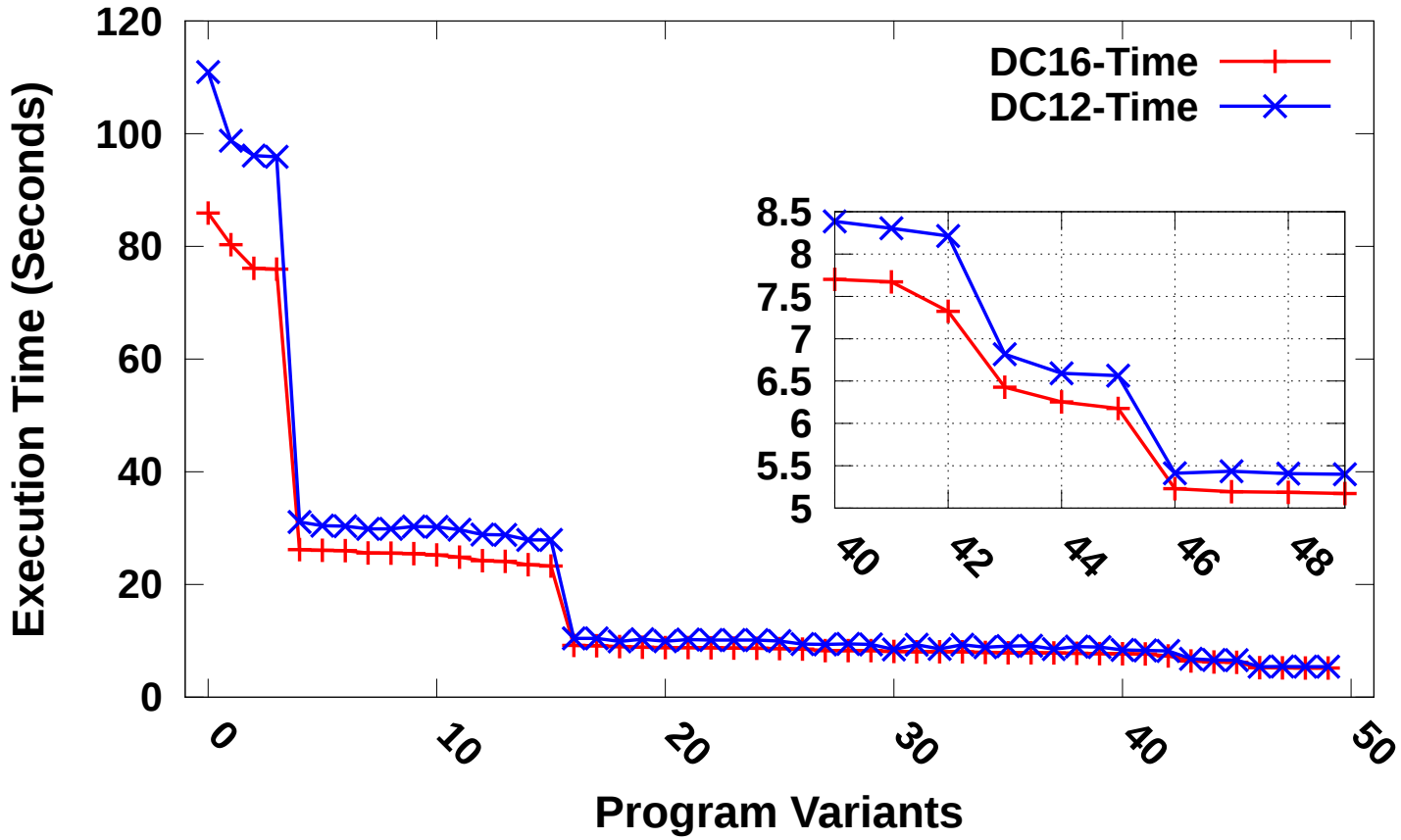
- Loop Tiling
- Loop Fusion



Experiments Setup

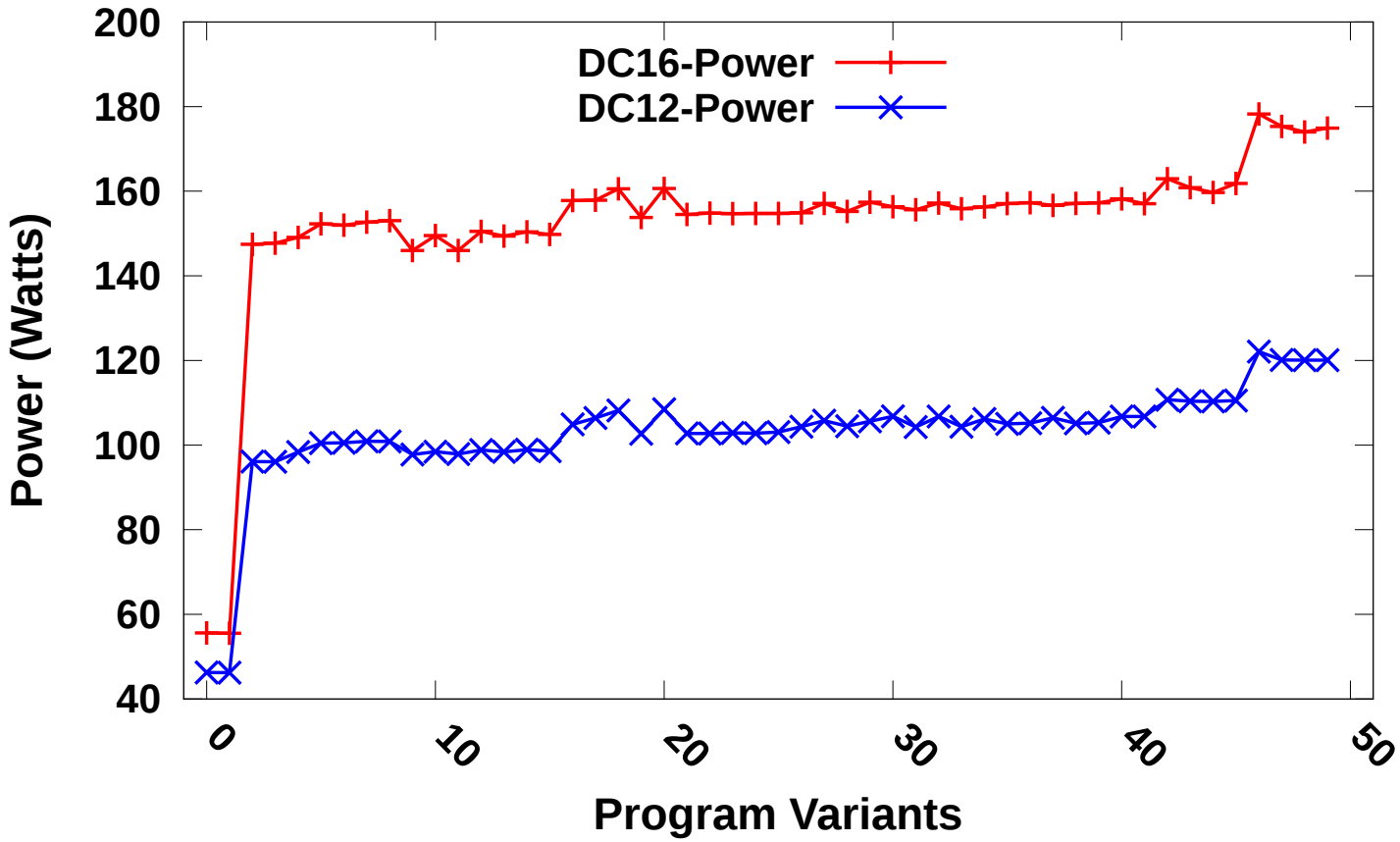
- Intel Xeon E5-2680 (dual socket 8-core processor with 20MB cache, Sandy Bridge architecture)
- Linux Kernel: 2.6.32
- Polyhedral Compilers: PoCC v1.2
- Benchmarks: 2mm, gesummv, jacobi-2D, and fdtd-2d Polybench
- Compiler: Intel ICC v14.0.2 (-O3)

Compiler Transformations with CPU Clock Modulation



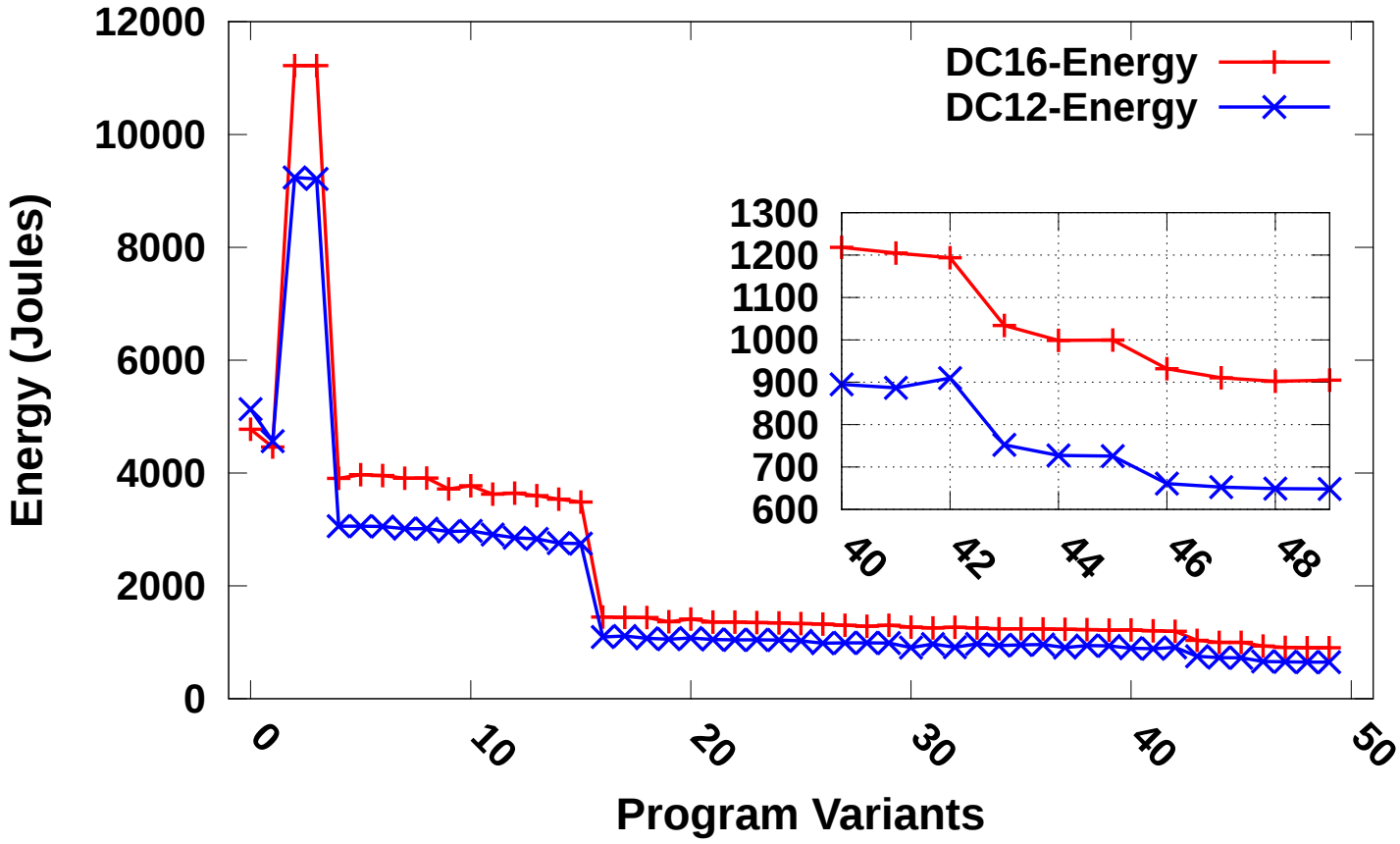
(a) Execution time of transformed program versions under Duty Cycle Modulation setting of 16 (DC16) and 12 (DC12)

Compiler Transformations with CPU Clock Modulation



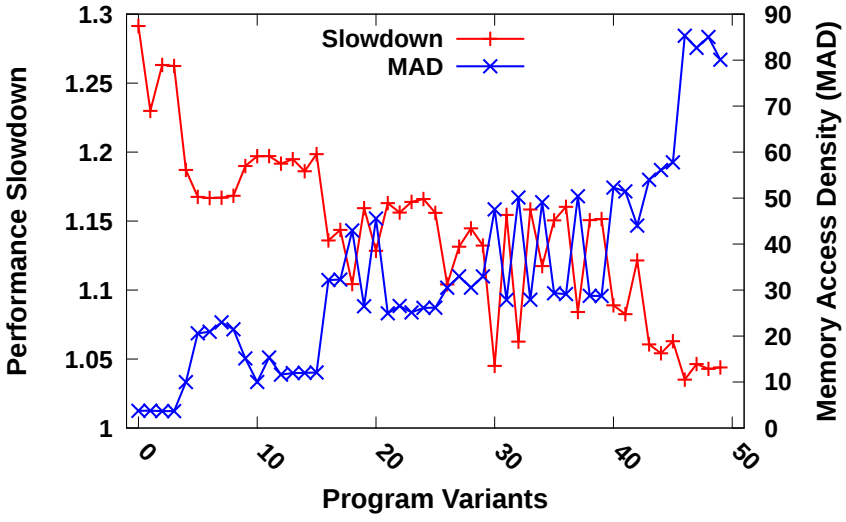
(b) Power consumption of transformed program versions under Duty Cycle Modulation setting of 16 (DC16) and 12 (DC12)

Compiler Transformations with CPU Clock Modulation

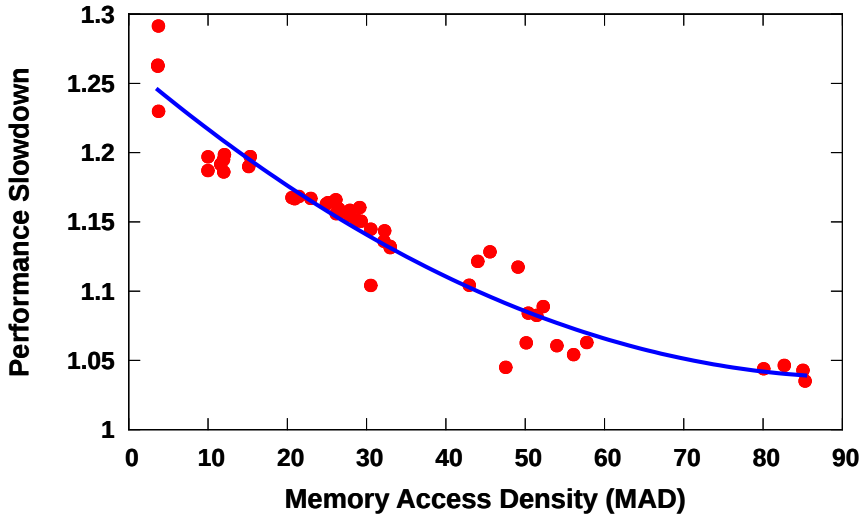


(c) Energy consumption of transformed program versions under Duty Cycle Modulation setting of 16 (DC16) and 12 (DC12) respectively.

Memory Access Density VS. Performance



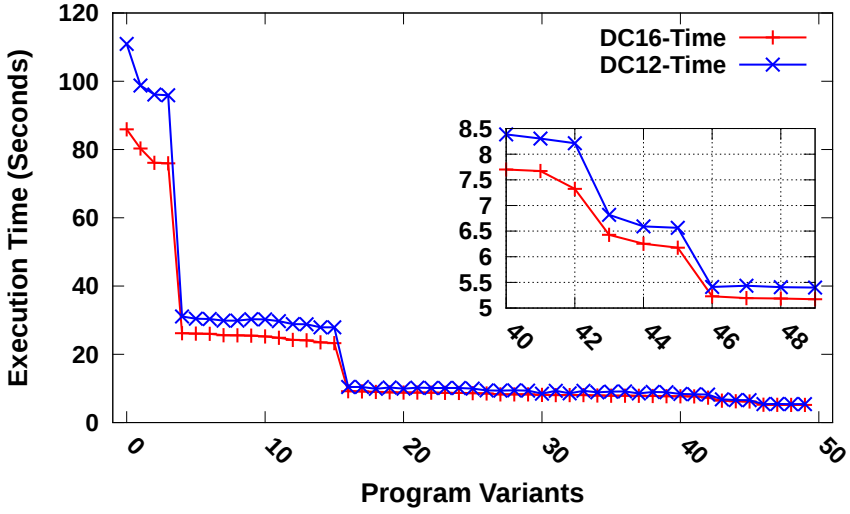
(a) The performance slowdown and the Memory Access Density of all compiler transformed programs.



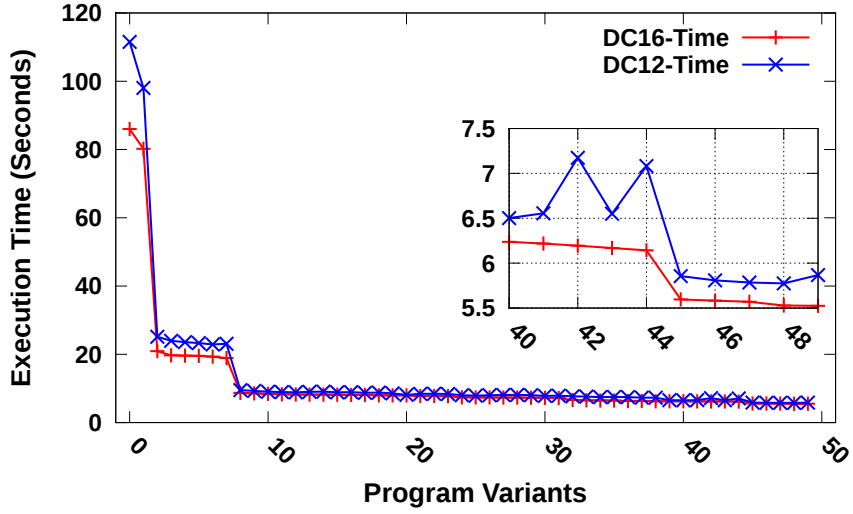
(b) The scattered plot of performance slowdown over the Memory Access Density and the trend line.

Figure: The correlation of the Memory Access Density metric and the performance slowdown of jacobi-2D benchmark.

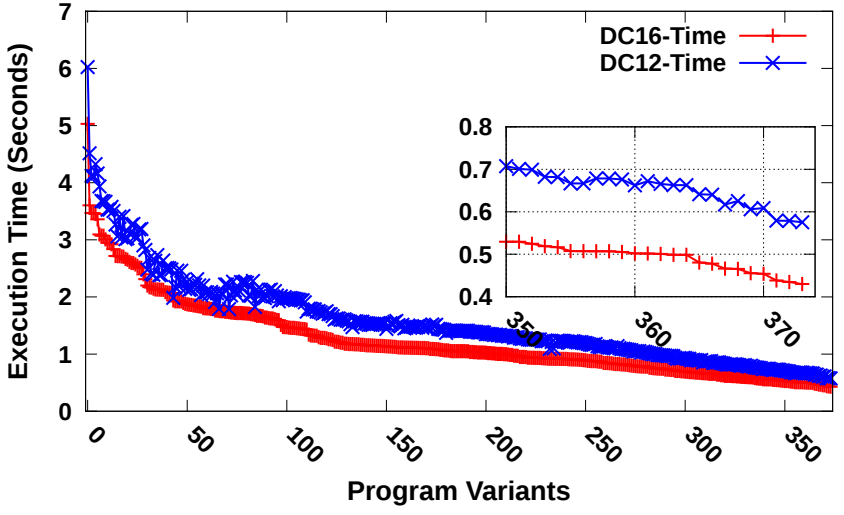
Performance Impact of Clock Modulation for Four Benchmarks



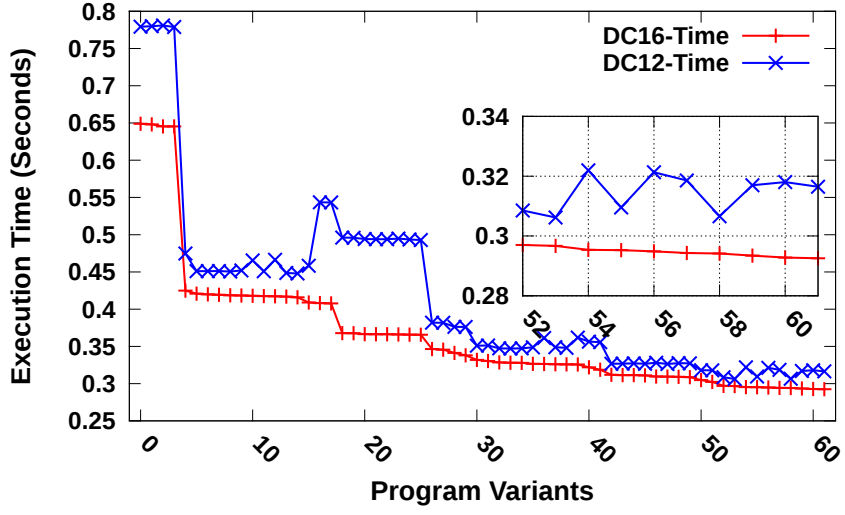
(a) jacobi-2D



(b) fdtd-2D

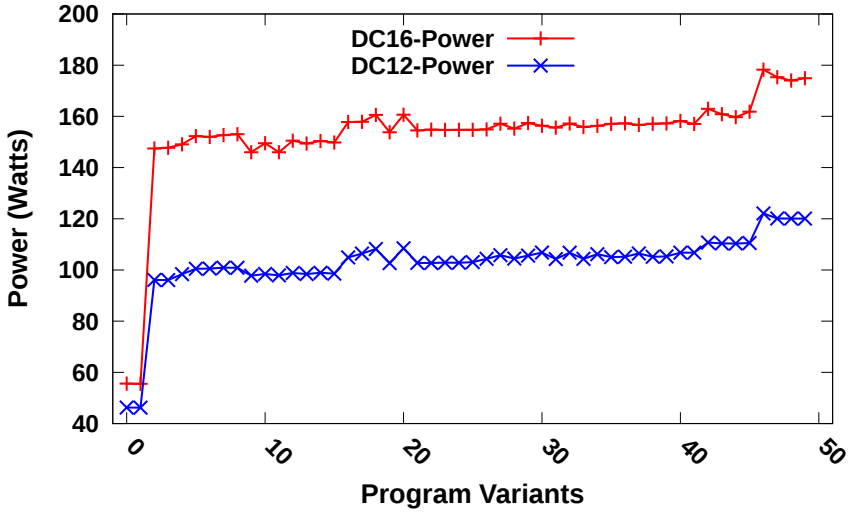


(c) 2mm

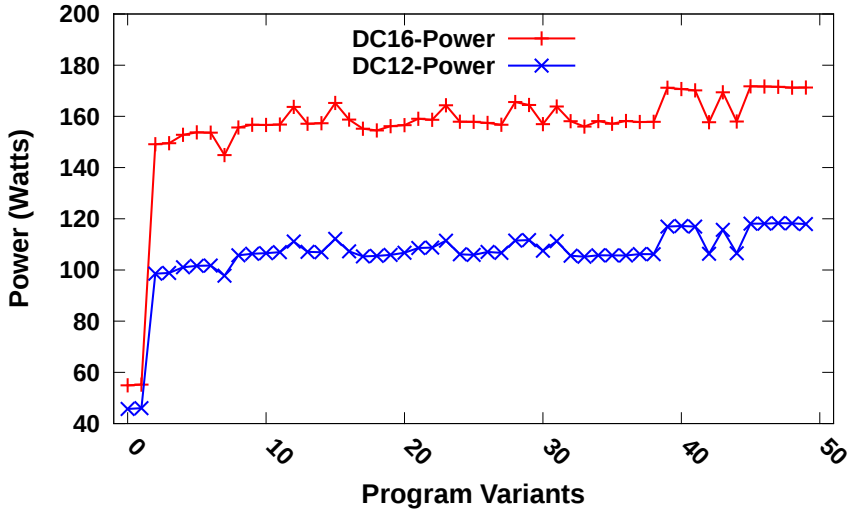


(d) gesummv

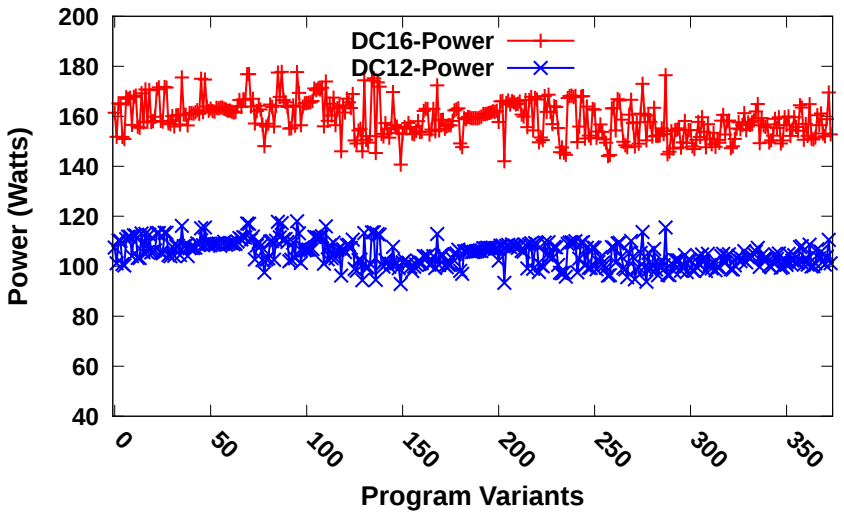
Power Impact of Clock Modulation for Four Benchmarks



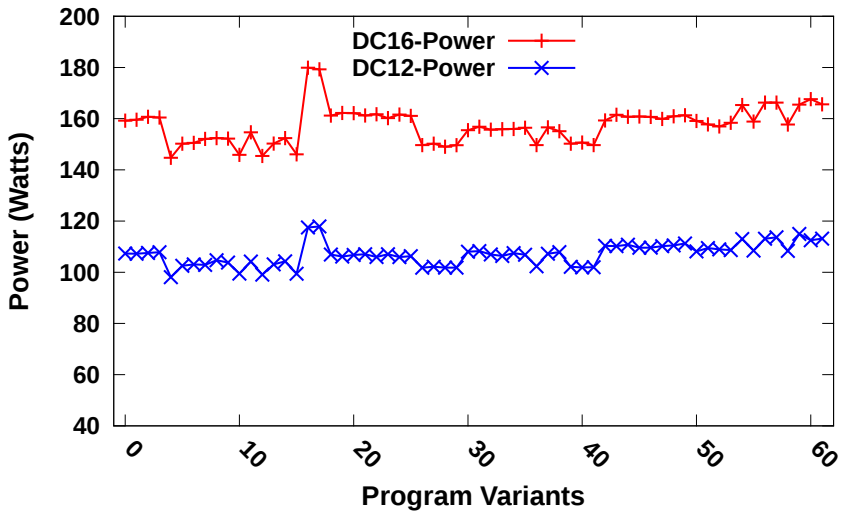
(a) jacobi-2D



(b) fdtd-2D

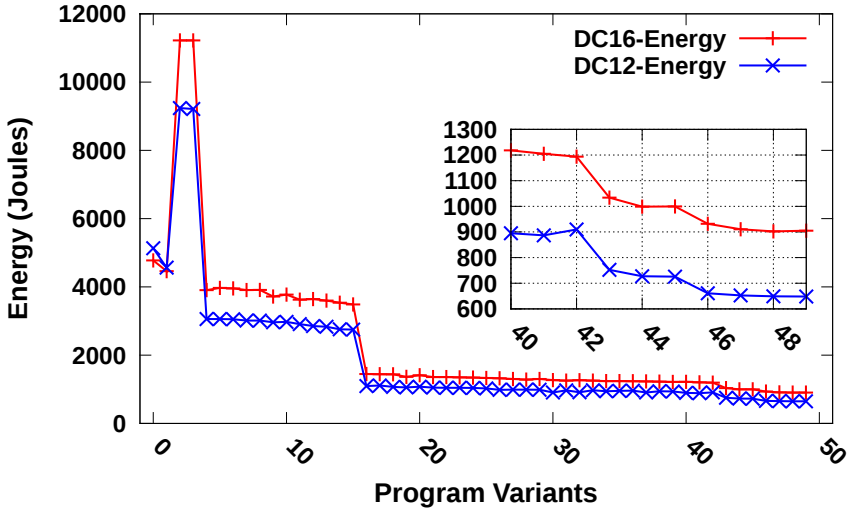


(c) 2mm

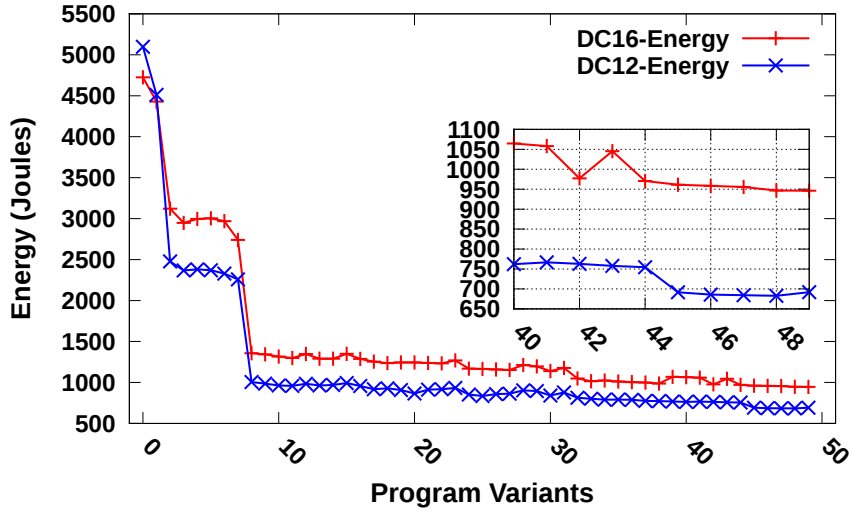


(d) gesummv

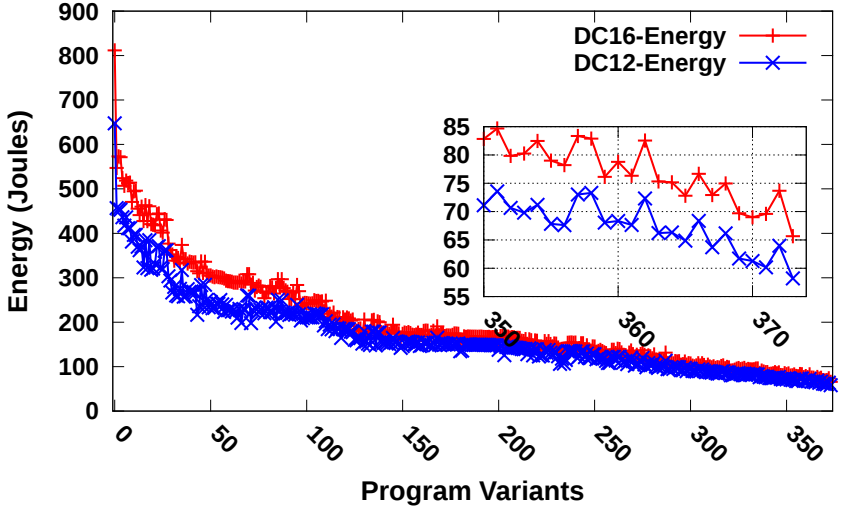
Energy Impact of Clock Modulation for Four Benchmarks



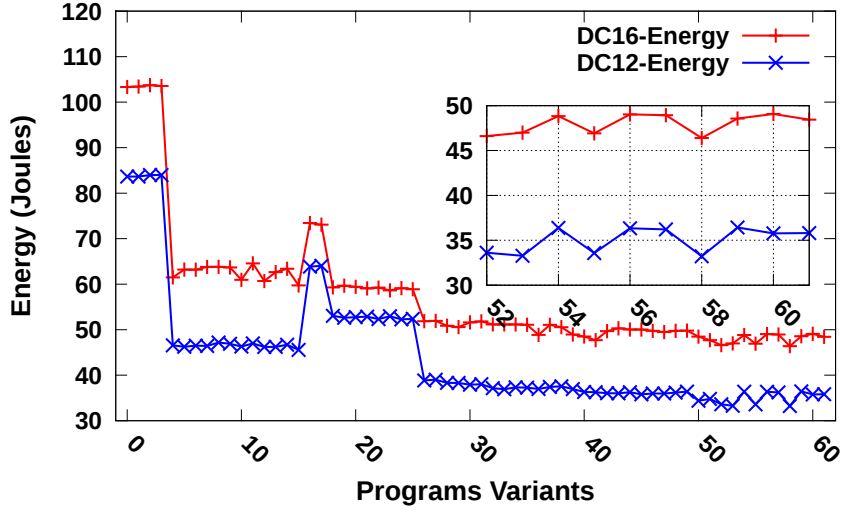
(a) jacobi-2D



(b) fdtd-2D



(c) 2mm



(d) gesummv

Jacobi-2D with 60 Watts Power Cap

DC Level	Time (seconds)	Energy (Joules)	Power (Watts)
10	136.65	5712.81	41.81
12	111.36	5103.09	45.82
14	102.49	4971.64	48.51
16	118.91	5602.35	47.12

Jacobi-2D without Power Cap

DC Level	Time (seconds)	Energy (Joules)	Power (Watts)
10	136.50	5735.15	42.01
12	110.94	5132.13	46.26
14	98.12	4890.33	49.84
16	85.91	4776.52	55.60

Jacobi-2D (Fastest Version) with 60 Watts Power Cap

DC Level	Time (seconds)	Energy (Joules)	Power (Watts)
10	21.31	1174.35	55.10
12	21.22	1173.67	55.31
14	20.92	1157.27	55.32
16	21.22	1168.4	55.07

Jacobi-2D (Fastest Version) without Power Cap

DC Level	Time (seconds)	Energy (Joules)	Power (Watts)
10	5.44	647.45	118.96
12	5.41	649.21	120.06
14	5.35	750.03	140.31
16	5.18	902.20	174.02

Conclusion

- Compiler transformations affected differently by power management techniques
- Fastest program variants observed to consume more power
- With power capping, non-optimal program sped up by reducing frequency

Acknowledgment

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3. U.S. Department of Energy: XPress project

Q & A

Thanks!