Vishal Saxena

Publications

Last Updated: November 16, 2023

Publications

Note: I followed the 'sequence determines credit' (SDC) approach for author credits till year 2016 and switched to the more prevalent 'first-last-author-emphasis' (FLAE) norm starting 2017.

Refereed Journal Publications

[J1] A. Dorzhigulov and **V. Saxena**, "Spiking CMOS-NVM Mixed-Signal Neuromorphic ConvNet with Circuit- and Training-optimized Temporal Subsampling," *Frontiers of Neuroscience: Neuromorphic Engineering*, vol. 17, p. 1177592, 2023, impact factor: 5.512.

[J2] M. J. Shawon and **V. Saxena**, "Fully Automatic In-Situ Reconfiguration of Optical Filters in a CMOS-Compatible Silicon Photonic Process," *IEEE Journal of Lightwave Technology (JLT)*, vol. 41, pp. 1286 – 1297, 2022, impact factor: 4.439 (1 Citation).

[J3] **V. Saxena**, "Neuromorphic computing: From emerging devices to integrated circuits," *(invited) Journal of Vacuum Science & Technology (JVST)-B*, vol. 39, pp. 010 801 (1–19), 2021, impact factor: 3.234 (11 Citations).

[J4] **V. Saxena**, "Mixed-Signal Neuromorphic Computing Circuits using Hybrid CMOS-RRAM Integration," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 581–586, 2021, impact factor: 3.691 (10 Citations).

[J5] R. Vaila, J. Chiasson, and **V. Saxena**, "A Deep Unsupervised Feature Learning Spiking Neural Network with Binarized Classification Layers for EMNIST Classification," *IEEE Transactions on Emerging Topics in Computational Intelligence (TETCI)*, pp. 1–12, 2020, impact factor: 4.34 (25 Citations).

[J6] M. J. Shawon and **V. Saxena**, "Rapid Simulation of Photonic Integrated Circuits Using Verilog-A Compact Models," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 10, pp. 3331–3341, 2020, impact factor: 4.14 (21 Citations).

[J7] **V. Saxena**, X. Wu, I. Srivastava, and K. Zhu, "Towards neuromorphic learning machines using emerging memory devices with brain-like energy efficiency," *(invited) Special Issue CMOS Low Power Design, Journal of Low Power Electronics and Applications (JLPEA)*, vol. 8, no. 4, 2018, impact factor: 2.1 (28 Citations).

[J8] X. Wu and **V. Saxena**, "Dendritic Processing Enables Bio-Plausible Stochastic STDP in Compound Binary Synapse," *IEEE Transaction on Nanotechnology (TNANO)*, vol. 18, pp. 149–159, 2018, impact factor: 2.967 (15 Citations).

[J9] K. Zhu and **V. Saxena**, "From Design to Test: A High-Speed PRBS," *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*, vol. 26, no. 10, pp. 2099 – 2107, 2018, impact factor: 2.8 (9 Citations).

[J10] K. Zhu and **V. Saxena**, "Case Study of a Hybrid Optoelectronic Limiting Receiver," *IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers*, vol. 64, no. 10, pp. 2797 – 2805, 2017, impact factor: 4.14.

[J11] S. Balagopal, K. Zhu, X. Wu, and **V. Saxena**, "Design-to-Test: A Low-Power, 1.25 GHz, Single-Bit Single-Loop Continuous-Time Modulator with 15 MHz Bandwidth and 60 dB Dynamic Range," *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 90, no. 3, pp. 625–638, 2017.

[J12] X. Wu, **V. Saxena**, and K. Zhu, "Homogeneous Spiking Neuromorphic System for Real-World Pattern Recognition," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 5, no. 2, pp. 254 – 266, June 2015, impact factor: 5.01 (74 Citations).

[J13] X. Wu, **V. Saxena**, and K. Zhu, "A CMOS Spiking Neuron for Brain-Inspired Neural Networks with Resistive Synapses and In-Situ Learning," *IEEE Transactions on Circuits and Systems (TCAS) II: Express Briefs*, vol. 62, no. 11, pp. 1088–1092, 2015, impact factor: 3.691 (143 Citations).

[J14] K. Zhu, **V. Saxena**, X. Wu, and W. Kuang, "Design Considerations for Traveling-Wave Modulator Based CMOS Photonic Transmitters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 4, pp. 412 – 416, April 2015, impact factor: 3.691 (29 Citations).

[J15] S. Balagopal and **V. Saxena**, "A 1 GSps, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT Delta-Sigma ADC with 1.5 Cycle Quantizer Delay and Improved STF," *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 78, no. 2, pp. 275–286, 2014.

[J16] T. Tran, A. Rothenbuhler, E. H. Barney Smith, **V. Saxena**, and K. A. Campbell, "Reconfigurable Threshold Logic Gates using Memristive Devices," *Journal of Low Power Electronics and Applications*, vol. 3, no. 2, pp. 174–193, 2013, impact factor: 2.1 (46 Citations).

[J17] S. Balagopal and **V. Saxena**, "A Low-Power Single-bit Continuous-time Delta-Sigma Converter with 92.5 Dynamic Range for Biomedical Applications," *Journal of Low Power Electronics and Applications*, vol. 2, no. 3, pp. 197–209, 2012, impact factor: 2.1 (11 Citations).

[J18] **V. Saxena**, A. Kumar, S. Mishra, S. Palermo, and K. Lakshmikumar, "Optical Interconnects using Hybrid Integration of CMOS and Silicon-Photonic ICs: Tutorial Brief," *IEEE Transactions on Circuits and Systems (TCAS) II: Express Briefs*, 2024, impact factor: 3.691.

[J19] **V. Saxena** and M. J. Shawon, "Compact Modeling and Rapid Simulation of Silicon Photonic Micro-Ring and Disk Modulators," *submitted to the Optics Express*, 2023, impact factor: 3.833.

[J20] M. J. Shawon and **V. Saxena**, "Optical Linearization of Silicon Photonic Ring-Assisted Mach-Zehnder Modulator," *under review in the IEEE Journal of Lightwave Technology (JLT)*, 2023, impact factor: 4.439.

Journal Manuscript Preprints

[K1] R. Vaila, J. Chiasson, and **V. Saxena**, "Deep Convolutional Spiking Neural Networks for Image Classification," *arXiv:1903.12272*, 2019, (29 citations).

Note: IEEE conference manuscripts are peer-reviewed and typically 4-5 pages in length.

Refereed Conference Publications

[C1] V. Kumar, S. Mishra, and **Saxena, V.**, "Power Linear DACs (PLDACs) for Configuration and Control of Silicon Photonic Integrated Circuits," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, Monterey, CA, May 2023.

[C2] M. J. Shawon and **V. Saxena**, "A Silicon Photonic Reconfigurable Optical Analog Processor (SiROAP) with a 4x4 Optical Mesh," in *IEEE International Solid State Circuits Conference (ISSCC)*, San Francisco, Feb 2023, impact factor: 6.12.

[C3] M. J. Shawon and **V. Saxena**, "Automatic In-situ Optical Linearization of Silicon Photonic Ring-Assisted MZ Modulator for Integrated RF Photonic SoCs," in *Optical Fiber Communications Conference and Exhibition (OFC)*, San Diego, Mar 2023.

[C4] A. Dorzhigulov and **V. Saxena**, "Hybrid CMOS-RRAM Spiking CNNs with Time-Domain Max-Pooling and Integrator Re-Use," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, Austin, TX, May 2022.

[C5] S. Mishra, M. J. Shawon, and **V. Saxena**, "A Hybrid CMOS Photonic 25Gbps Microring Transmitter with a -0.5-1.2V Direct-Coupled Drive," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, Austin, TX, May 2022.

[C6] **V. Saxena**, "A Mixed-Signal Convolutional Neural Network Using Hybrid CMOS-RRAM Integration," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, Daegu, South Korea, 2021.

[C7] J. Shawon, Md. and **V. Saxena**, "Analysis of RF Photonic Link using SiliconPhotonic Ring-Assisted Mach Zehnder Modulator," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020.

[C8] R. Vaila, J. Chiasson, and V. Saxena, ""continuous learning in a single-incremental-task scenario with spike features"," in *ICONS 2020: International Conference on Neuromorphic Systems*, 2020.

[C9] **V. Saxena**, "A Process-Variation Robust RRAM-Compatible CMOS Neuron for Neuromorphic System-on-a-Chip," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, Seville, Spain, 2020.

[C10] R. Vaila, J. Chiasson, and V. Saxena, "Feature extraction using spiking convolutional neural networks," in *ACM Proceedings of the International Conference on Neuromorphic Systems (ICONS)*, 2019, p. 14.

[C11] J. Shawon, Md. and **V. Saxena**, "Rapid Simulation of Photonic Integrated Circuits using Verilog-A Compact Models," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C12] R. Wang and **V. Saxena**, "A CMOS Photonic Optical PAM-4 Transmitter Linearized using Three-Segment Ring Modulator," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C13] **V. Saxena**, "High LRS-Resistance CMOS Memristive Synapses for Energy-Efficient Edge-AI and Neuromorphic System-on-a-Chip," in *(invited) IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C14] C. Li, K. Yu, J. Rhim, K. Zhu, N. Qi, M. Fiorentino, T. Pinguet, M. Peterson, V. Saxena, and S. Palermo, "A 3d-integrated 56 gb/s NRZ/PAM4 reconfigurable segmented mach-zehnder modulator-based si-photonics transmitter," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*. IEEE, Oct. 2018. [Online]. Available: https://doi.org/10.1109/bcicts.2018.8551089

[C15] J. Shawon, Md., R. Wang, and **V. Saxena**, "Design and Modeling of Silicon Photonic Ring-Based Linearized RF-to-Optical Modulator," in *in the proceedings of IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

[C16] R. Wang, J. Shawon, Md., and **V. Saxena**, "Design and Compact Modeling of Silicon-Photonic Coupling-Based Ring Modulators for Optical Interconnects," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

[C17] **V. Saxena**, X. Wu, and K. Zhu, "Energy-Efficient CMOS Memristive Synapses for Mixed-Signal Neuromorphic System-on-a-Chip," in *IEEE International Symposium on Circuits & Systems (ISCAS)*, 2018.

[C18] **V. Saxena**, X. Wu, I. Srivastava, and K. Zhu, "Towards Spiking Neuromorphic System-on-a-Chip with Bio-plausible Synapses using Emerging Devices," in *(invited) ACM NanoCom, Washington D.C.*, 2017.

[C19] R. Kehan, Z. Wang, X. Wu, and **V. Saxena**, "Behavioral Modeling and Characterization of Silicon Photonic Mach-Zehnder Modulator," in *(invited) International Midwest Symposium on Circuits and System (MWSCAS), Boston*, Aug 2017.

[C20] K. Zhu, S. Balagopal, X. Wu, and **V. Saxena**, "Realization of a 10 GHz PLL in IBM 130 nm SiGe BiCMOS Process for Optical Transmitter," in *proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, 2017.

[C21] X. Wu and **V. Saxena**, "Enabling Bio-Plausible Multi-level STDP using CMOS Neurons with Dendrites and Bistable RRAMs," in *International Joint Conference on Neural Networks (IJCNN), Anchorage, Alaska*, July 2017.

[C22] J. Browning, **V. Saxena**, D. Plumlee, T. Akinwande, M. Worthington, and B. Hay, "A phase-controlled magnetron using a modulated electron source," in *IEEE International Conference on Plasma Science (ICOPS)*. IEEE, 2016, pp. 1–1.

[C23] Z. Kehan, **V. Saxena**, and X. Wu, "Modeling and Optimizing Bond Wire Packaging Interface in a Hybrid CMOS Photonic Traveling-Wave MZM Transmitter," in *proceedings of the IEEE System-on-a-Chip Conference (SOCC), Seattle*, 2016.

[C24] Z. Kehan, C. Li, N. Qi, K. Yu, R. Fiorentino, Marco Bluesoleil, and **V. Saxena**, "Modeling of MZM-Based Photonic Link Power Budget," in *proceedings of the Optical Interconnects Conference 2016, San Diego*, 2016.

[C25] Z. Kehan, **V. Saxena**, and X. Wu, "A Comprehensive Design Approach for a MZM Based PAM-4 Silicon Photonic Transmitter," in *International Midwest Symposium on Circuits and System (MWSCAS), Fort Collins, USA*, Aug 2015.

[C26] X. Wu, **V. Saxena**, and Zhu, "A CMOS Spiking Neuron for Dense Memristor- Synapse Connectivity for Brain-Like Computing," in *International Joint Conference on Neural Networks (IJCNN), Killarney, Ireland*, July 2015.

[C27] Z. Kehan, **V. Saxena**, X. Wu, and S. Balagopal, "Design Analysis of a 12.5 GHz PLL in 130 nm SiGe BiCMOS Process," in *submitted to IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2015.

[C28] Z. Kehan, **V. Saxena**, and W. Kuang, "Compact Verilog-A Modeling of Silicon Traveling-Wave Modulator for Hybrid CMOS Photonic Circuit Design," in *proc. 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station*, 2014.

[C29] W. Xinyu, **V. Saxena**, and K. A. Campbell, "Energy-efficient STDP-based learning circuits with memristor synapses," in *proc. SPIE Machine Intelligence and Bio-inspired Computation, Baltimore*, 2014.

[C30] Z. Kehan, S. Balagopal, and **V. Saxena**, "Design of a 10-Gb/s Integrated Limiting Receiver for Silicon Photonics Interconnects," in *proc. 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus*, 2013.

[C31] S. Balagopal, Z. Kehan, and **V. Saxena**, "Systematic Synthesis of Cascaded Continuous-time Delta-Sigma ADCs for Wideband Data Conversion," in *(invited) proc. 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus*, Aug 2013.

[C32] Z. Kehan, S. Balagopal, and **V. Saxena**, "Systematic Design of a 10-bit Pipelined ADC," in *submitted to IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2013.

[C33] T. Tran, A. Rothenbuhler, E. Barney Smith, **V. Saxena**, and K. Campbell, "Reconfigurable Threshold Logic gates using Memristive Devices," in *IEEE Subthreshold Microelectronics Conference, Waltham, MA*, 2012.

[C34] S. Balagopal and **V. Saxena**, "Design of Wideband Continuous-Time Delta-Sigma ADCs Using Two-Step Quantizers," in *(invited) proc. 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise*, Aug 2012.

[C35] S. Balagopal and **V. Saxena**, "A 1 GSps, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT Delta-Sigma ADC with 1.5 Cycle Quantizer Delay and Improved STF," in *proc. 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise*, Aug 2012.

[C36] R. Koppula, S. Balagopal, and **V. Saxena**, "Multi-bit Continuous-time Delta-Sigma Modulator for Audio Applications," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2012.

[C37] G. VanAckern, R. J. Baker, A. J. Moll, and **V. Saxena**, "On-Chip 3D Inductors using Thru-Wafer Vias," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2012.

[C38] R. M. R. Koppula, S. Balagopal, and **V. Saxena**, "Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs," in *proceedings of IEEE System on Chip Conference (SOCC), Taipei, Taiwan*, Sep 2011.

[C39] **V. Saxena**, S. Balagopal, and R. J. Baker, "Systematic Design of Three-Stage Opamps using Split-Length Compensation," in *(invited) proceedings of the 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, S. Korea*, 2011.

[C40] S. Balagopal, R. M. R. Koppula, and **V. Saxena**, "Systematic Design of Multibit Continuous-time Delta-Sigma Modulators using Two-step Quantizers," in *(student paper contest) proceedings of the 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, S. Korea*, Aug 2011.

[C41] **V. Saxena**, S. Balagopal, and H. Chen, "Reconfigurable Continuous-time Delta-Sigma ADCs for Sofware-Defined and Multistandard Radios," in *SDR'11 WinnComm*, 2011.

[C42] S. Balagopal and **V. Saxena**, "A Low-Power Single-bit Continuous-time Delta-Sigma Converter with 92.5 dB Dynamic Range and design of Low-Voltage Delta-Sigma ADCs," in *IEEE/MITLL Subthreshold Microelectronics Conference, Boston*, Sep 2011.

[C43] S. Balagopal, R. M. Koppula, and **V. Saxena**, "A 110uW Single-Bit Continuous-time Delta-Sigma Converter with 94.4dB Dynamic Range," in *proceedings of Dallas Workshop on Circuits and Systems (DCAS)*, Oct 2010.

[C44] **V. Saxena** and R. J. Baker, "Indirect Compensation Techniques for Three-Stage Fully-Differential Opamps," in *(invited) proceedings of the 53rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2010.

[C45] **V. Saxena** and R. J. Baker, "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," in *proceedings of the 53rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2010.

[C46] S. Gupta, **V. Saxena**, K. Campbell, and R. Baker, "W-2W Current Steering DAC for Programming Phase Change Memory," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2009, pp. 59–62.

[C47] **V. Saxena** and R. J. Baker, "Indirect Compensation Techniques for Three-Stage CMOS Op-amps," in *proceedings of the 52nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2009, pp. 9–12.

[C48] **V. Saxena**, K. Li, G. Zheng, and R. Baker, "A K-Delta-1-Sigma Modulator for Wideband Analog-to-Digital Conversion," in *proceedings of the 52nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2009, pp. 411–415.

[C49] **V. Saxena** and R. J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors," in *proceedings of the 51st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2008, pp. 109–112.

[C50] **V. Saxena** and R. J. Baker, "Indirect Feedback Compensation of CMOS Op-Amps," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 3–4.

[C51] K. Duvvada, **V. Saxena**, and R. J. Baker, "High Speed Digital Input Buffer Circuits," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 11–12.

[C52] **V. Saxena**, T. Plum, J. Jessing, and R. J. Baker, "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 17–18.

Peer-Reviewed Conference Publications in Progress

[E1] **V. Saxena** and M. J. Shawon, "A 7x4 Mesh Silicon Photonic Programmable Analog Optical Processor with Algorithmic Calibration," in *submitted to the IEEE International Solid State Circuits Conference (ISSCC)*, San Francisco, Feb 2024, impact factor: 6.12.

Non-Peer-Reviewed Conference Publications

[D1] **V. Saxena** and M. J. Shawon, "Reconfigurable RF Photonic Processor Architecture using a Silicon Photonics MPW Platform," in *GOMACTech Conference*, Miami, March 2022.

[D2] **V. Saxena**, "Neuromorphic computing: From emerging devices to neuromorphic system-on-a-chip," *(invited abstract) AVS 66th International Symposium & Exhibition*, 2020.

[D3] **V. Saxena**, X. Wu, and M. Mitkova, "Addressing Challenges in Neuromorphic Computing with Memristive Synapses," in *U.S. DoE Neuromorphic Computing Workshop, Oak Ridge National Laboratory*, July 2016.

[D4] **V. Saxena** and R. J. Baker, "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," in *proceedings of the 4th Annual Austin Conference on Integrated Circuits and Systems*, 2009, pp. 24–25.

[D5] K. Li, **V. Saxena**, G. Zheng, and R. Baker, "Full Feed-Forward K-Delta-1-Sigma Modulator," in *proceedings of the 4th Annual Austin Conference on Integrated Circuits and Systems*, 2009, pp. 26–27.

[D6] **V. Saxena** and R. J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors," in *Indirect Compensation Technique for Low-Voltage Op-Amps,", proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, 2008.

Book Chapters

[B1] **V. Saxena**, *"Challenges and Recent Advances in NVM-based Neuromorphic Computing ICs," Chapter in the Selected Topics in Intelligent Chips with Emerging Devices, Circuits and Systems*, 1st ed., A. James and B. Choubey, Eds. River Publishers, 2023.

[B2] **V. Saxena**, *"High-performance CMOS Operational Amplifiers for Signal Processing," Chapter in the High Performance Analog and Power Management Circuit Design Techniques for Modern SoCs*, A. Garimella and P. M. Furth, Eds. Springer International Publishing AG, 2016.

[B3] **V. Saxena**, *"Fully-Differential Operational Amplifiers Design and Simulation," Chapter in the High Performance Analog and Power Management Circuit Design Techniques for Modern SoCs*, A. Garimella and P. M. Furth, Eds. Springer International Publishing AG, 2016.

[B4] **V. Saxena** and R. J. Baker, *"Analog and Digital VLSI Design," Chapter 19 in the Fundamentals of Industrial Electronics, Wilamowski, B. M. and Irwin, J. D. (editors)*, 2nd ed. CRC Press, 2011.

Conference Poster Presentations

[P1] V. Saxena, "Monolithically Integrated CMOS-NVM Neuromorphic System on a Chip for Real-Time Cognition," in *SRC DARPA JUMP2.0 Workshop*, 2019.

[P2] V. Saxena, "Silcion Photonics enabled Reconfigurable Optical Analog Processor (SiROAP)," in *DARPA YFA PI Meetings*, 2019, 2021, 2022.

[P3] R. Vaila, J. Chiasson, and V. Saxena, "Spiking CNNs with PYNN and NEURON," in *5th Neuro Inspired Computational Elements Workshop (NICE 2018)*, July 2018.

[P4] J. Shawon and V. Saxena, "Compact Modeling of Linearized CMOS Photonic Modulators for Millimeter-Wave Wireless," in *NSF mmWave RCN Workshop, Tucson*, 1 2018.

[P5] V. Saxena, "Linearized CMOS Photonic Modulators for Millimeter-Wave Wireless," in *NSF mmWave RCN Workshop, Madison*, July 2017.

[P6] V. Saxena, "Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing," in *5th Neuro Inspired Computational Elements Workshop (NICE 2017)*, July 2018.

[P7] V. Saxena, "Hybrid CMOS Photonic Integrated Circuits for Millimeter Wave Communication," in *NSF mmWave RCN Workshop*, July 2016.

[P8] V. Saxena, "Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing," in *SRC DARPA JUMP Workshop*, July 2017.

[P9] V. Molina and **V. Saxena**, "Tunable Vernier Ring Filters in an Integrated CMOS Photonic Platform," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2016.

[P10] R. M. R. Koppula, S. Balagopal, and **V. Saxena**, "Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, Apr 2011.

[P11] S. Stickel and **V. Saxena**, "A Four-Phase Charge Pump with Power Supply Rejection Based Regulation," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2011.