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(54) **MEMORY CONTROLLED CIRCUIT SYSTEM AND APPARATUS**

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G11C 7/22	(2006.01)

(52) **U.S. Cl.**

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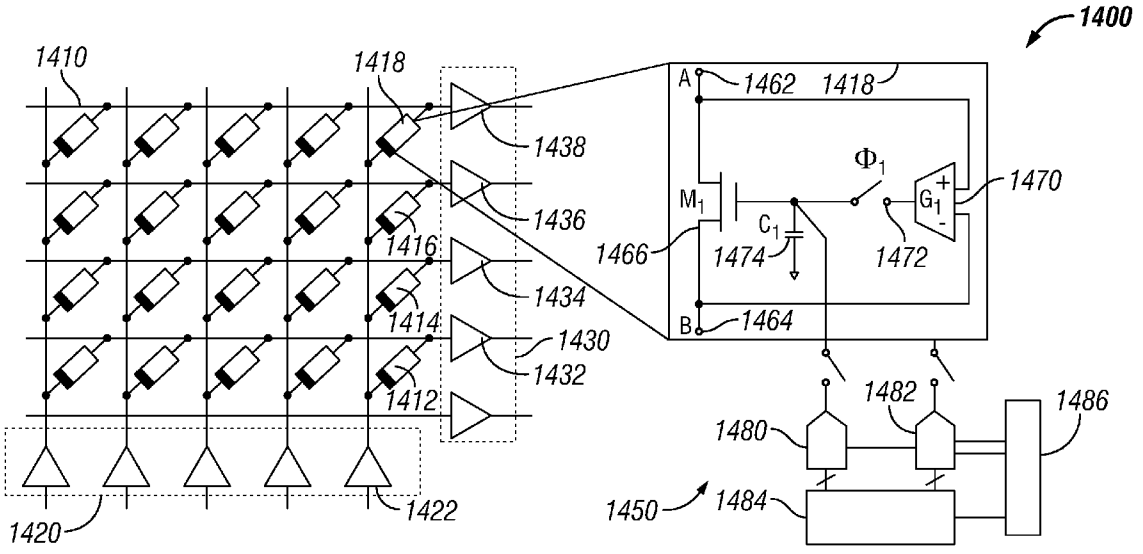
(57) **ABSTRACT**

In an embodiment, a memory controlled circuit includes a configurable circuit element electrically coupled to a first terminal and to a second terminal. The memory controlled circuit further includes a weight update circuit. A first input of the weight update circuit is electrically coupled to the first terminal and a second input of the weight update circuit is electrically coupled to the second terminal. The memory controlled circuit also includes a dynamic analog memory electrically coupled to the configurable circuit element and to the weight update circuit.



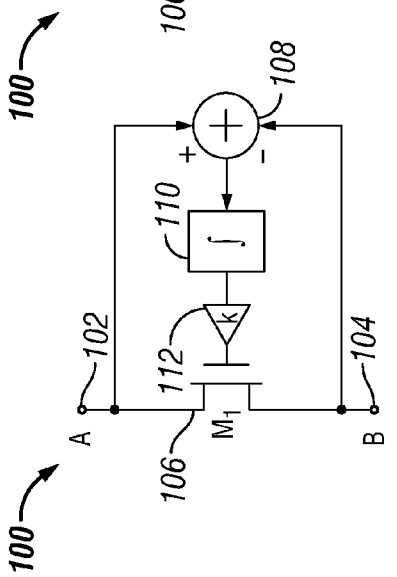


FIG. 1A

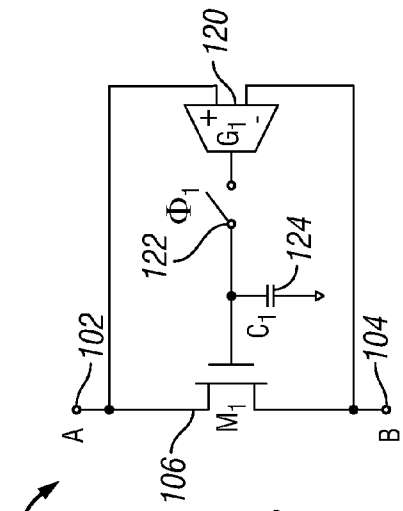


FIG. 1B

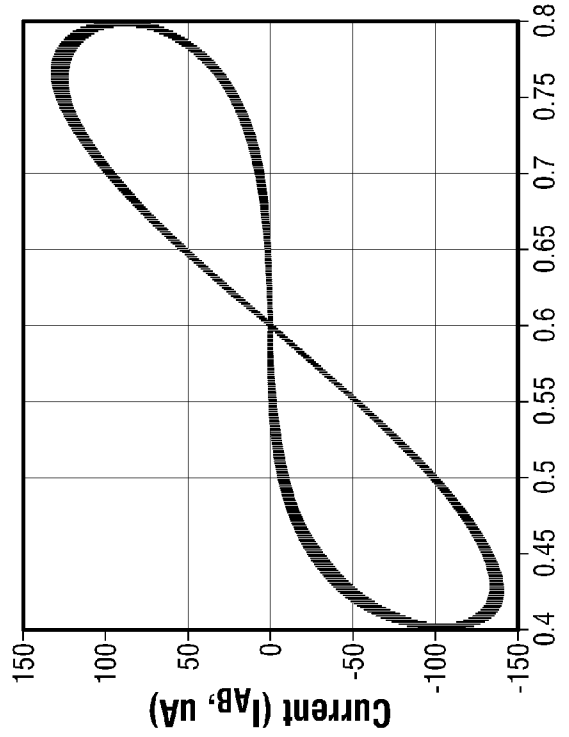


FIG. 2A

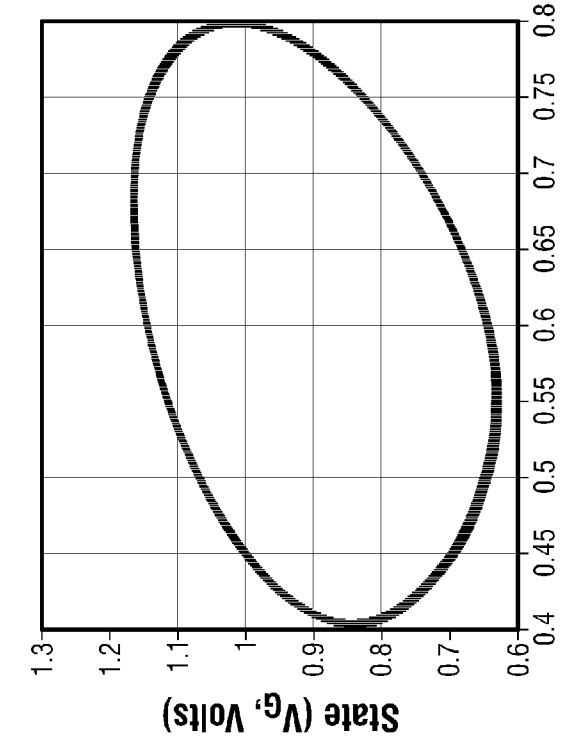


FIG. 2B

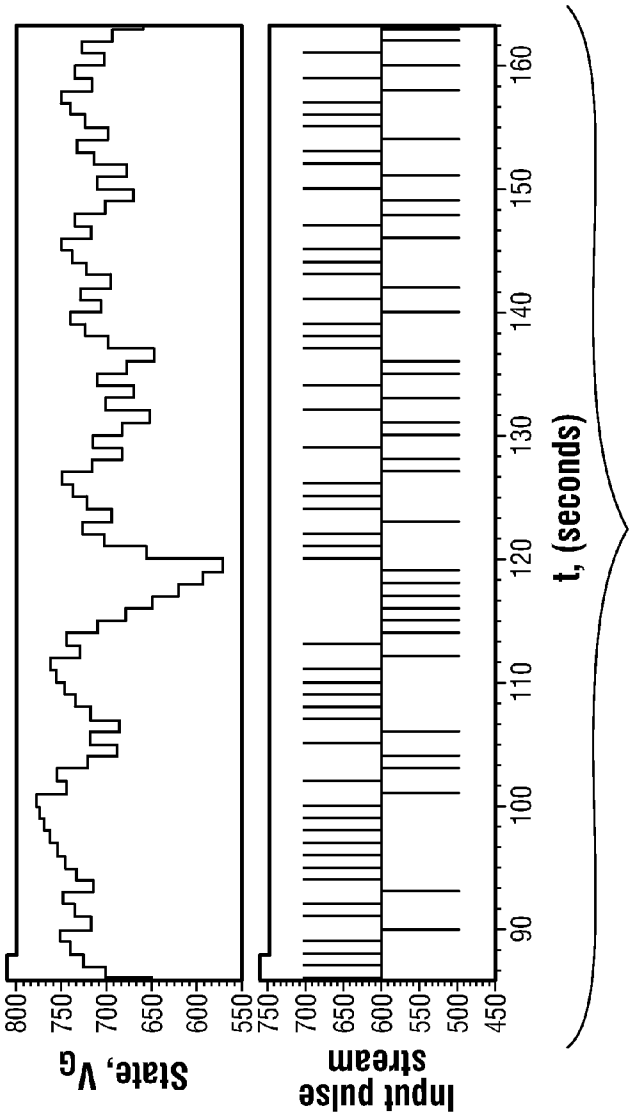

State, V_G
Input pulse stream
t, (seconds)
800
750
700
650
600
550
750
700
650
600
550
500
450
90
100
110
120
130
140
150
160

FIG. 3

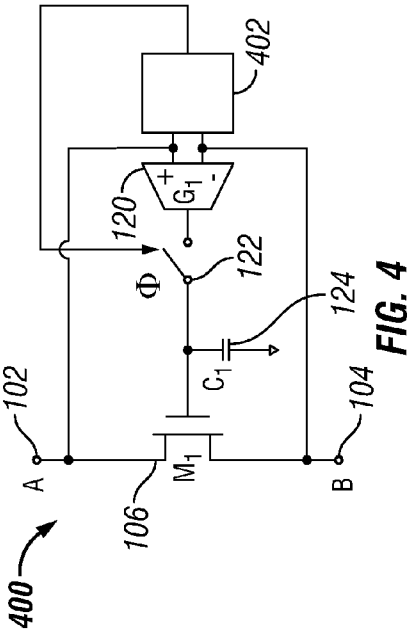

400
102
A
106
M_1
C_1
124
B
104
Φ
120
122
G_1
+
-
402

FIG. 4

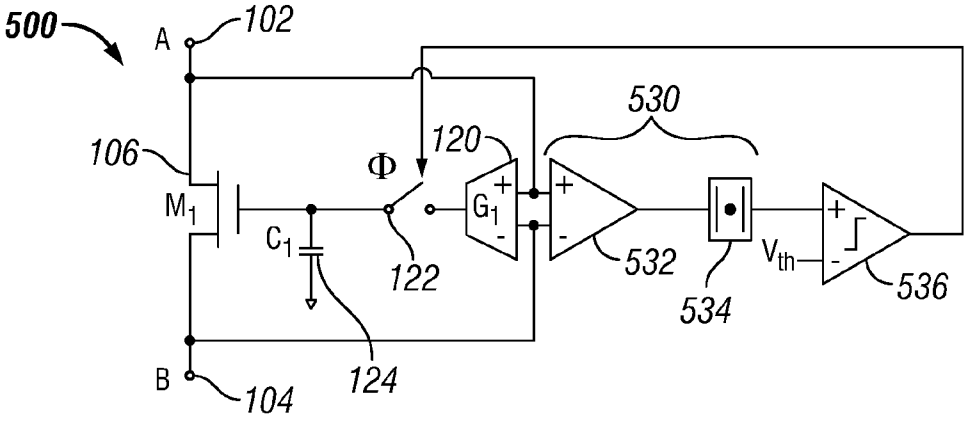

500
A
102
106
M1
C1
Φ
120
G1
122
124
B
104
530
532
534
Vth
536

FIG. 5A

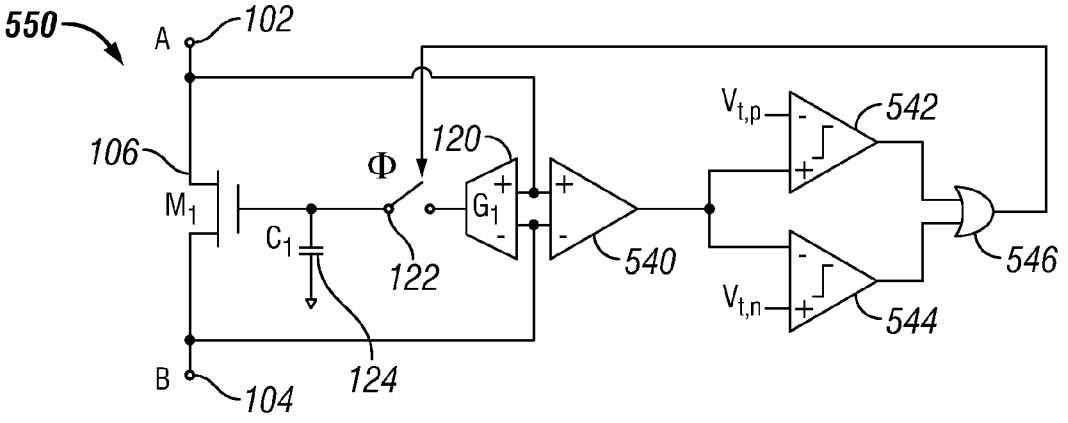

550
A
102
106
M1
C1
Φ
120
G1
122
124
B
104
540
Vt,p
542
Vt,n
544
546

FIG. 5B

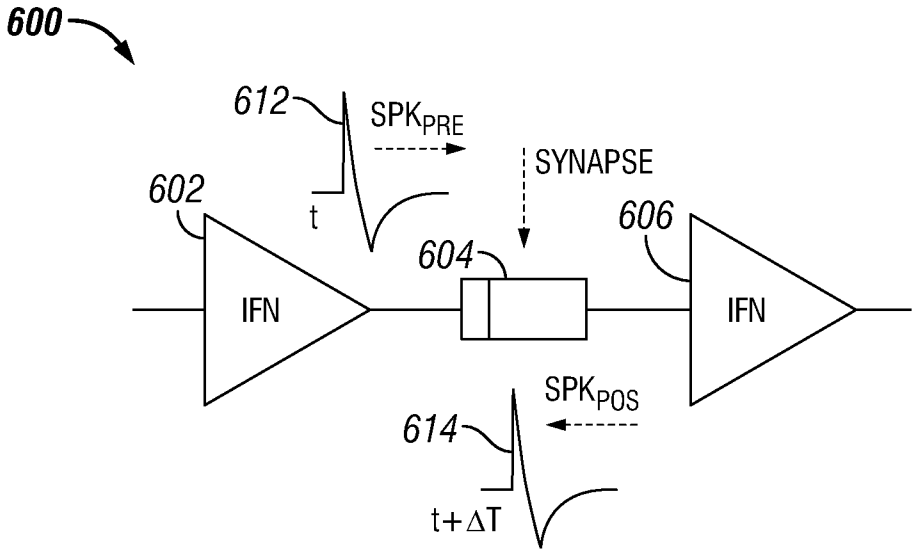

600
612
SPK_PRE
t
SYNAPSE
602
606
604
IFN
IFN
SPK_POS
614
t+ΔT

FIG. 6A

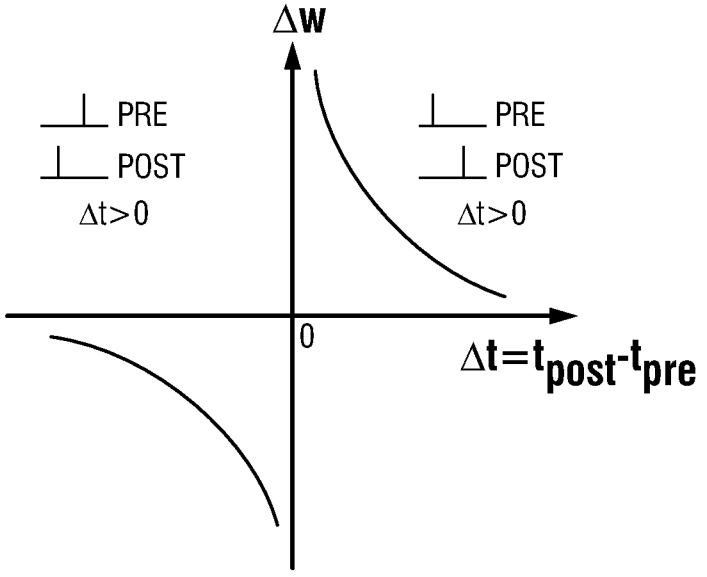

Δw
PRE
POST
Δt>0
PRE
POST
Δt>0
0
Δt=t_post-t_pre

FIG. 6B

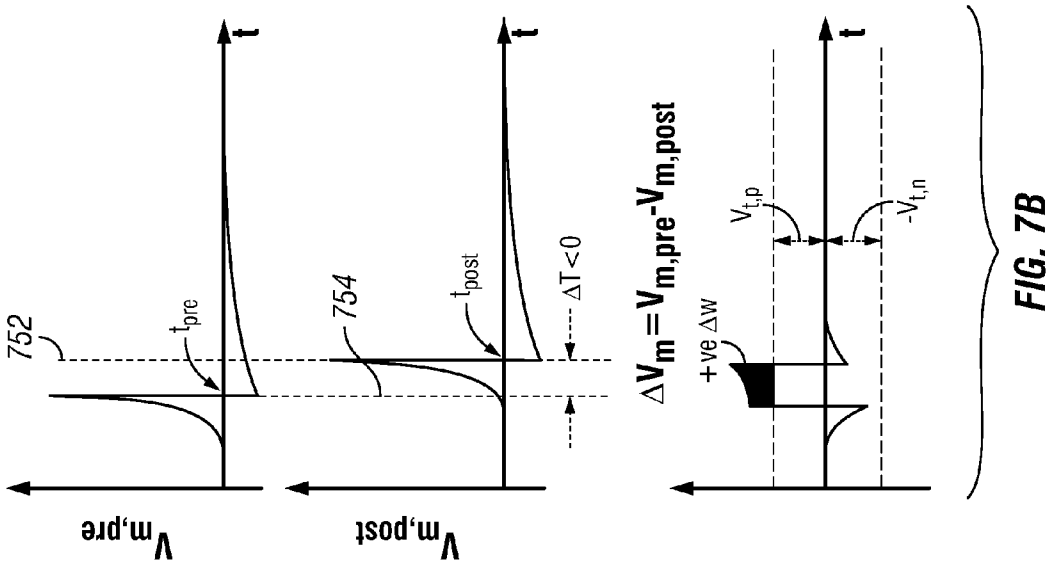

752
754
t_{pre}
t_{post}
ΔT<0
$V_{m,pre}$
$V_{m,post}$
t
$\Delta V_m = V_{m,pre} - V_{m,post}$
+ve Δw
$V_{t,p}$
$-V_{t,n}$

FIG. 7B

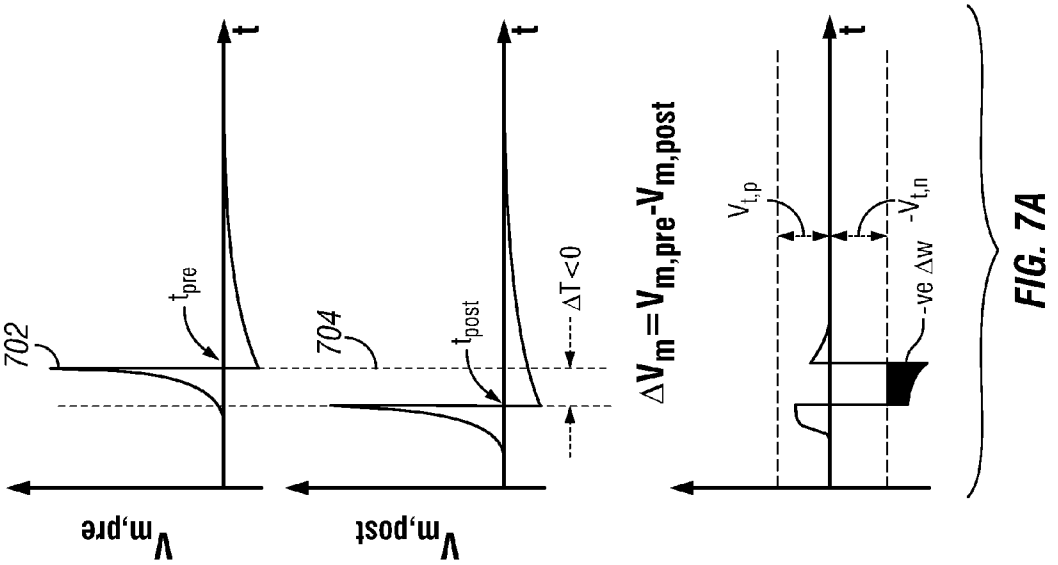

702
704
t_{pre}
t_{post}
ΔT<0
$V_{m,pre}$
$V_{m,post}$
t
$\Delta V_m = V_{m,pre} - V_{m,post}$
$V_{t,p}$
$-V_{t,n}$
-ve Δw

FIG. 7A

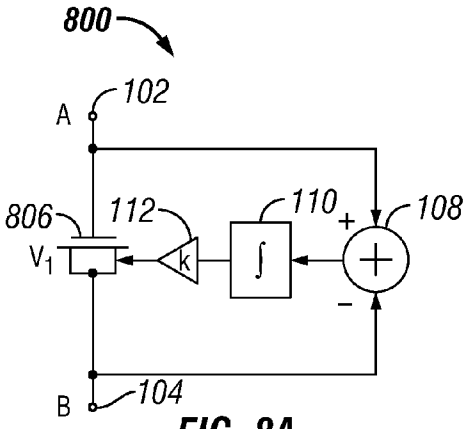


FIG. 8A

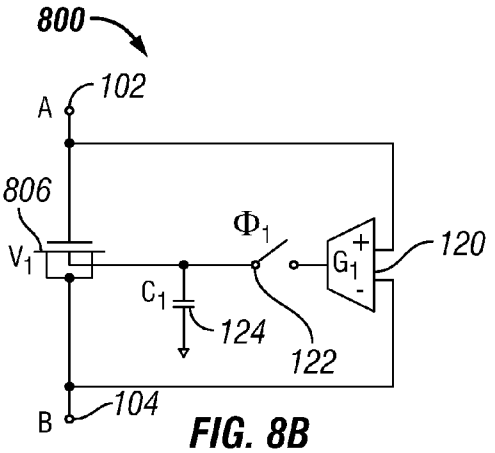


FIG. 8B

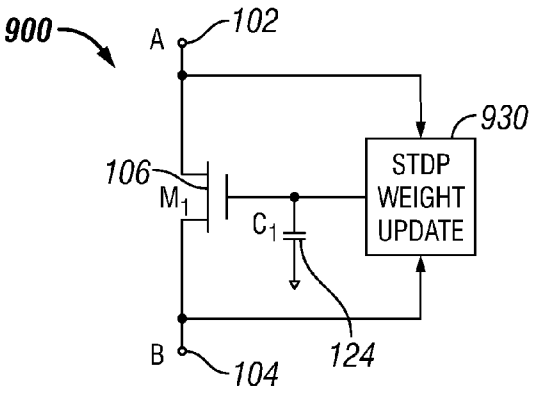


FIG. 9A

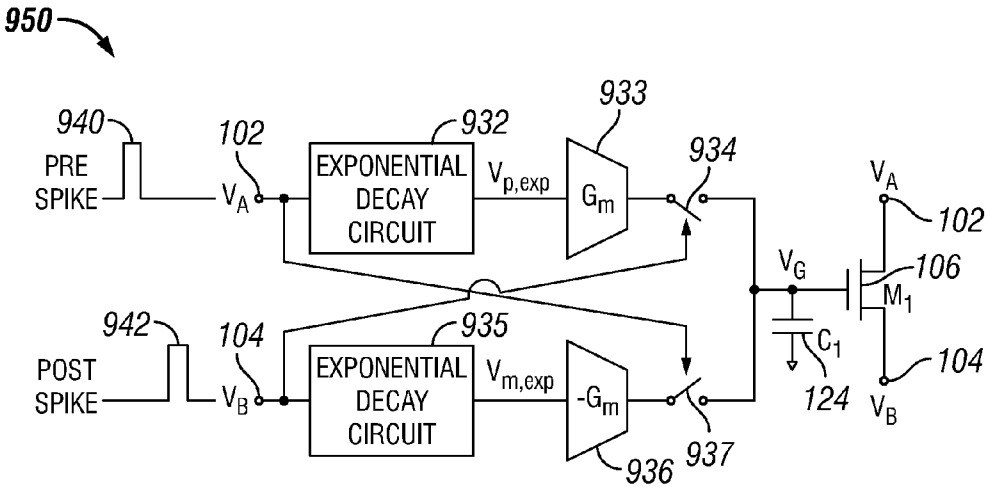


FIG. 9B

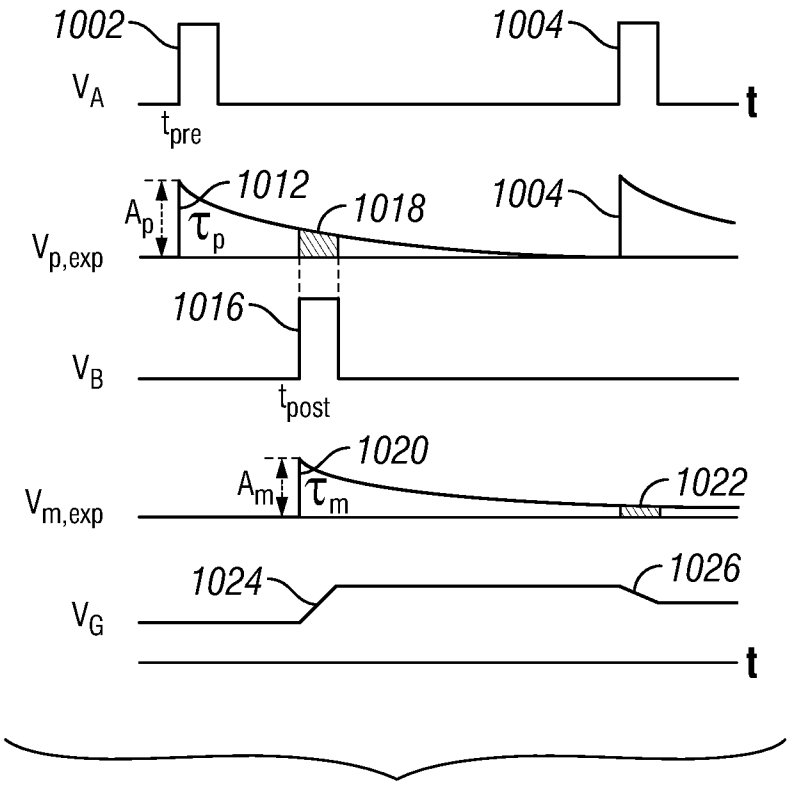


FIG. 10A

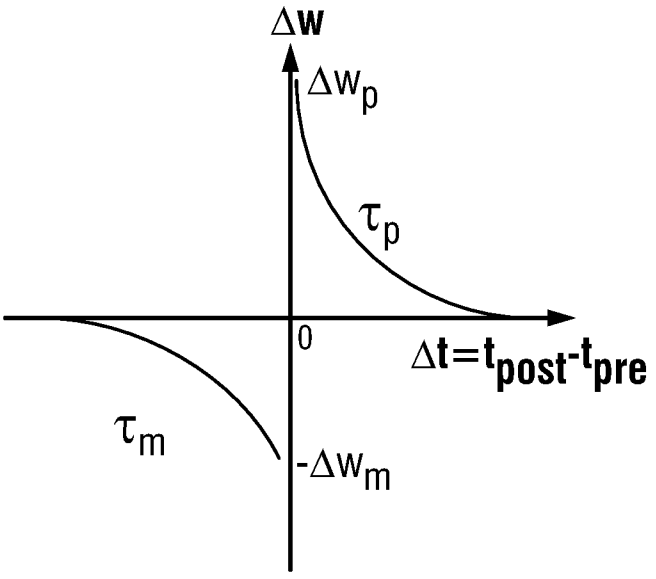


FIG. 10B

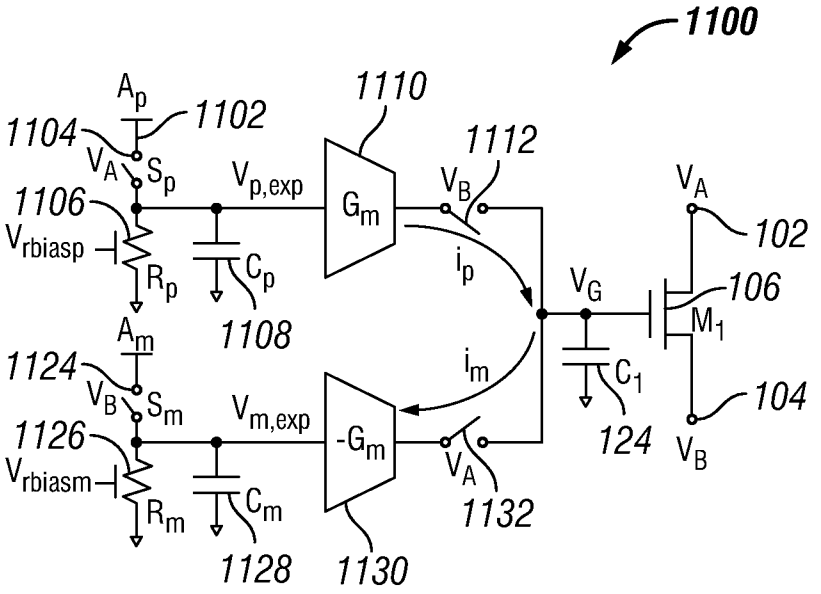

1100
A_p
1102
1104
V_A
S_p
$V_{p,exp}$
1110
G_m
1112
V_B
V_A
102
1106
V_{rbiasp}
R_p
C_p
1108
i_p
V_G
106
M_1
A_m
1124
V_B
S_m
$V_{m,exp}$
i_m
C_1
104
1126
V_{rbiasm}
R_m
C_m
$-G_m$
V_A
124
V_B
1128
1130
1132

FIG. 11

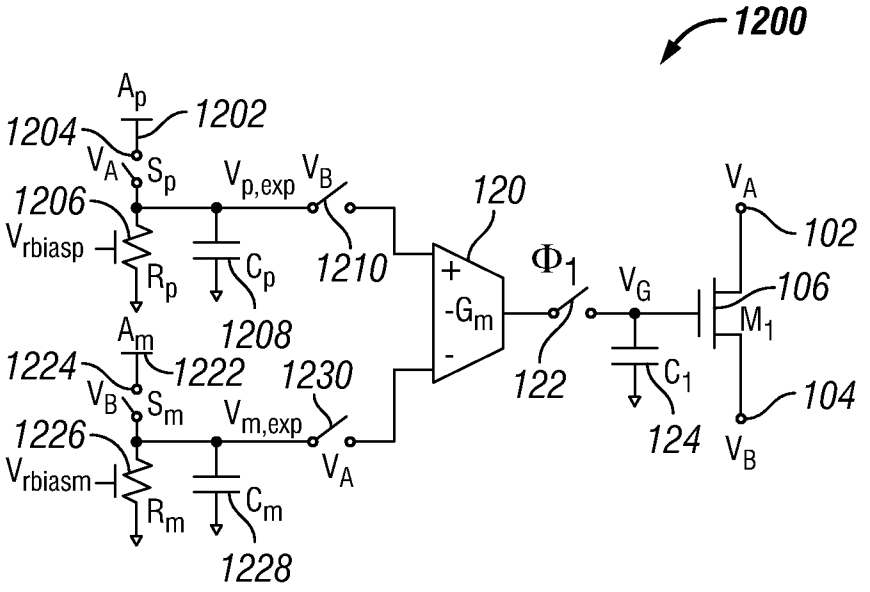

1200
A_p
1202
1204
V_A
S_p
$V_{p,exp}$
V_B
120
V_A
102
1206
V_{rbiasp}
R_p
C_p
1210
+
$-G_m$
-
Φ_1
V_G
106
M_1
1208
A_m
1224
1222
1230
V_B
S_m
$V_{m,exp}$
122
C_1
104
1226
V_{rbiasm}
R_m
C_m
V_A
124
V_B
1228

FIG. 12

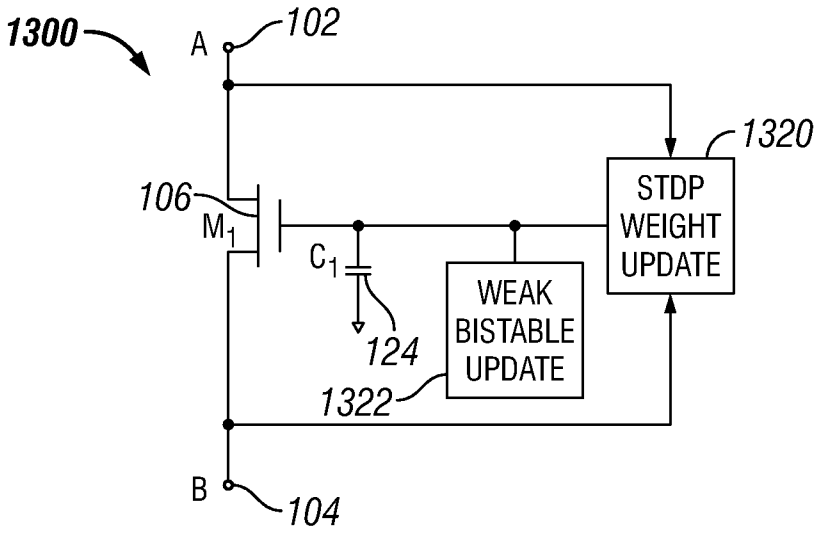


FIG. 13A

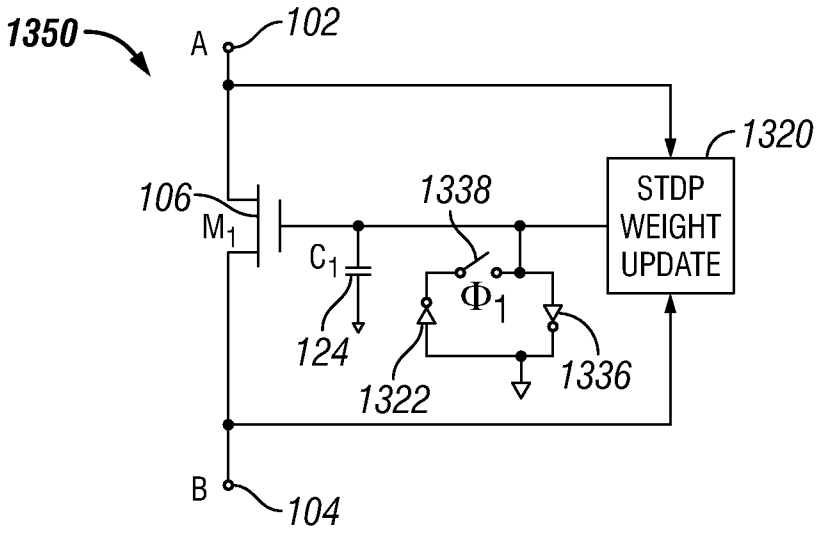


FIG. 13B

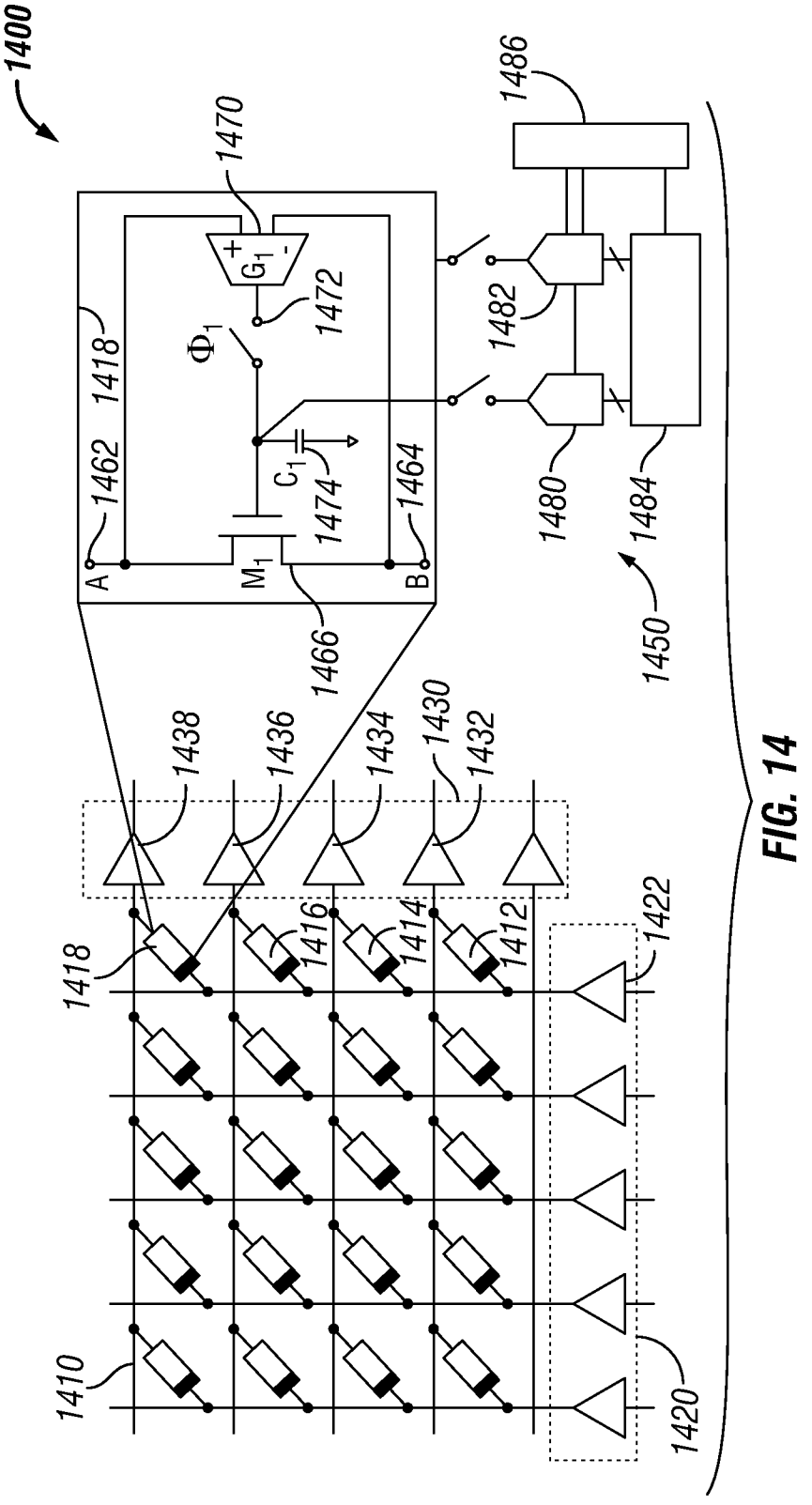

1400
1470
1486
1472
1482
1418
1462
1464
1474
1480
1484
1466
1450
1438
1436
1434
1430
1432
1416
1414
1412
1422
1418
1410
1420
A
B
M1
C1
G1
Φ1

FIG. 14

MEMORY CONTROLLED CIRCUIT SYSTEM AND APPARATUS

RELATED APPLICATIONS

[0001] This application, under 35 U.S.C. §119, claims the benefit of U.S. Provisional Patent Application Ser. No. 61/973,754 filed on Apr. 1, 2014, and entitled "DYNAMIC SYNAPSE CIRCUITS," which is hereby incorporated by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure generally relates to a memory controlled circuit and more particularly to a synapse-type memory controlled circuit.

BACKGROUND

[0003] Computing technology continues to advance by steadily scaling transistor size and by adding more complexity to processing devices while also lowering power consumption in the processing devices. However, as computing technology becomes smaller and more complex, it is increasingly difficult to maintain the current scaling rates. Traditional computer architectures, such as the von-Neumann architecture, require a large number of interconnects and other components. The von-Neumann architecture may be insufficient to keep up with the rapid pace of scaling associated with newer computing devices. For example, current difficulties associated with traditional computer architectures include device variability and interconnect bottlenecks. These difficulties become more pronounced as computing devices become smaller. In order to ensure continued advances in computing technology, new computer architectures are needed to overcome the scaling difficulties associated with traditional computer architectures.

SUMMARY

[0004] Disclosed is a memory controlled circuit that may at least partially emulate a synapse of a biological brain. The memory controlled circuit includes a transistor or another type of configurable circuit to generate a variable resistance or a variable capacitance between two terminals. The transistor or other type of configurable circuit may be controlled by a state of the memory controlled circuit. The memory controlled circuit may further include a capacitor or other dynamic analog memory to store the state.

[0005] In an embodiment, a memory controlled circuit includes a configurable circuit element electrically coupled to a first terminal and to a second terminal. The memory controlled circuit further includes a weight update circuit. A first input of the weight update circuit is electrically coupled to the first terminal and a second input of the weight update circuit is electrically coupled to the second terminal. The memory controlled circuit also includes a dynamic analog memory electrically coupled to the configurable circuit element and to the weight update circuit.

[0006] In an embodiment, the weight update circuit includes a first exponential decay circuit, an input of the first exponential decay circuit coupled to the first terminal. The weight update circuit may also include a first switch. An input of the first switch may be coupled to an output of the first exponential decay circuit and an output of the first switch may be coupled to the dynamic analog memory. A controller of the first switch may be coupled to the second terminal. The weight update circuit may also include a second exponential decay circuit, an input of the second exponential decay circuit coupled to the second terminal. The weight update circuit may include a second switch. An input of the second switch may be coupled to an output of the second exponential decay circuit and an output of the second switch may be coupled to the dynamic analog memory. A controller of the second switch may be coupled to the first terminal.

[0007] In an embodiment, the first exponential decay circuit includes a resistor. The first exponential decay circuit may further include a capacitor coupled to the resister. The first exponential circuit may also include an third switch coupled to a voltage source. A level of the voltage source may correspond to a peak spike level. A controller of the third switch may be coupled to the first terminal. The third switch may enable a voltage at the capacitor to charge to the peak spike level when activated. The voltage may dissipate through the resistor when the third switch is disabled. The resistor may include a transistor coupled with a biasing circuit. The biasing circuit may cause the transistor to generate a resistance.

[0008] In an embodiment, the second exponential decay circuit includes a second resistor. The second exponential decay circuit may also include a second capacitor coupled to the second resister. The second exponential circuit may further include a fourth switch coupled to a second voltage source. A level of the second voltage source may correspond to a second peak spike level. A controller of the fourth switch may be coupled to the second terminal. The fourth switch may enable a voltage at the capacitor to charge to the second peak spike level when activated. The voltage may dissipate through the second resistor when the fourth switch is disabled.

[0009] In an embodiment, the weight update circuit further includes a first transconductor coupled between an output of the first exponential decay circuit and an input of the first switch. The weight update circuit may also include a second transconductor coupled between an output of the second exponential decay circuit and an input of the second switch.

[0010] In an embodiment, the weight update circuit also includes a transconductor, a first input of the transconductor coupled to an output of the first switch and a second input of the transconductor coupled to an output of the second switch. An output of the first exponential decay circuit may be coupled to an input of the first switch and an output of the second exponential decay circuit may be coupled to an input of the second switch.

[0011] In an embodiment, the memory controlled circuit further includes a third switch coupled between the transconductor and the dynamic analog memory. A controller of the third switch may be coupled to a strobe signal source.

[0012] In an embodiment, the memory controlled circuit also includes a bi-stable memory element coupled to the dynamic analog memory. The bi-stable memory element may be configured to stabilize a state of the dynamic analog memory when activated. The bi-stable memory element may include a first inverter. The bi-stable memory element may further include a second inverter. The bi-stable memory element may also include a switch. The first inverter and the second inverter may hold a particular voltage at the capacitor when the switch is activated. The capacitor may discharge when the switch is deactivated.

[0013] In an embodiment, the memory controlled circuit is integrated into a system of memory controlled circuits. The system may include at least one input neuron device. The system may also include at least one output neuron device.

The at least one input neuron device may be coupled to the at least one output neuron device via the first terminal and the second terminal.

[0014] In an embodiment, a method includes receiving a first digital pulse at a first terminal. The method further includes receiving a second digital pulse at a second terminal. The method also includes, in response to the second digital pulse, changing a value of a dynamic analog memory to a modified value. A difference between the value and the modified value may be based on a duration between a first time of the first digital pulse and a second time of the second digital pulse.

[0015] In an embodiment, an electrical property of a configurable circuit element positioned between the first terminal and the second terminal changes based on the modified value of the dynamic analog memory.

[0016] In an embodiment, the method also includes in response to receiving the first digital pulse, generating an exponentially decaying voltage. The method may include generating a current proportionally related to the exponentially decaying voltage. The method may further include electrically coupling the current to the dynamic analog memory during the second digital pulse. The method may also include receiving a third digital pulse at the first terminal. The method may include, in response to the third digital pulse, changing a value of the dynamic analog memory to a second modified value. A difference between the modified value and the second modified value may be based on a duration between the second time of the second digital pulse and a third time of a third digital pulse.

[0017] In an embodiment, the method further includes, in response to receiving the second digital pulse, generating an exponentially decaying voltage. The method may also include generating a current proportionally related to the exponentially decaying voltage. The method may include electrically coupling the current to the dynamic analog memory during the third digital pulse. The method may further include holding a voltage level of the dynamic analog memory at a bi-stable memory element.

[0018] In an embodiment, a method includes receiving a first digital pulse from a first neuron device. The method further includes passing the first digital pulse to a second neuron device. The method also includes receiving a second digital pulse from the second neuron device. The method includes passing the second digital pulse to the first neuron device. The method further includes changing a value of a dynamic analog memory based on the first digital pulse and the second digital pulse.

[0019] In an embodiment, changing the value of the dynamic analog memory includes increasing the value when the first digital pulse is received before the second digital pulse and decreasing the value when the first digital pulse is received after the second digital pulse.

[0020] The method of claim **18**, wherein a magnitude of changing the value of the dynamic analog memory is based on a duration between the first digital pulse and the second digital pulse.

[0021] While the disclosure is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and will be described in detail herein. However, it should be understood that the disclosure is not intended to be limited to the particular forms disclosed. Rather, the intention is to cover all modifications, equivalents and alternatives, both structural and operational, falling within the spirit and scope of the disclosure as defined by the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. **1**A illustrates a conceptual block diagram for an embodiment of a synapse-type memory controlled circuit;

[0023] FIG. **1**B illustrates a circuit implementation of an embodiment of a synapse-type memory controlled circuit;

[0024] FIG. **2**A illustrates a current-voltage hysteresis curve for a simulated embodiment of a synapse-type memory controlled circuit;

[0025] FIG. **2**B illustrates a state trajectory for the simulated embodiment of the synapse-type memory controlled circuit when swept with a sine-wave input at 1 MHz frequency;

[0026] FIG. **3** illustrates a pulsed characterization response of the simulated embodiment of the synapse-type memory controlled circuit showing monotonic incremental state control;

[0027] FIG. **4** illustrates an embodiment of a synapse-type memory controlled circuit with asynchronous weight update, compatible with spike timing-dependent plasticity (STDP) learning mechanisms.

[0028] FIGS. **5**A-**5**B illustrate embodiments of a synapse-type memory controlled circuit with asynchronous weight update using an embodiment of an event detector, compatible with STDP learning mechanisms.

[0029] FIGS. **6**A-**6**B illustrate an example of an STDP learning mechanism in a bio-inspired synapse-type memory controlled circuit.

[0030] FIGS. **7**A-**7**B illustrate an example of STDP-type synaptic weight updates that depend on the relative timing of the pre- and post-synaptic action potentials.

[0031] FIG. **8**A illustrates a conceptual block diagram of an embodiment of a synapse-type memory controlled circuit.

[0032] FIG. **8**B illustrates a circuit implementation of an embodiment of a synapse-type memory controlled circuit.

[0033] FIGS. **9**A-**9**B illustrate embodiments of a synapse-type memory controlled circuit compatible with digital spikes.

[0034] FIG. **10**A illustrates characteristic timing and waveforms of an embodiment of a synapse-type memory controlled circuit using digital spikes.

[0035] FIG. **10**B illustrates an STDP learning function exhibited by an embodiment of a synapse-type memory controlled circuit using digital spikes.

[0036] FIG. **11** illustrates an embodiment of a synapse-type memory controlled circuit with an exponential decay circuit.

[0037] FIG. **12** illustrates an embodiment of a synapse-type memory controlled circuit with an exponential decay circuit.

[0038] FIGS. **13**A-**13**B illustrate embodiments of a bi-stable synapse-type memory controlled circuit.

[0039] FIG. **14** illustrates an embodiment of a system **800** memory controlled circuits with a store and refresh scheme using an ADC/DAC combination.

DETAILED DESCRIPTION

[0040] Referring to FIG. **1**A, a conceptual block diagram of an embodiment of a synapse-type memory controlled circuit **100** is depicted. The memory controlled circuit **100** includes a first terminal **102**, a second terminal **104**, and a configurable circuit element **106** coupled to the first terminal **102** and to the second terminal **104**. The functionality of the memory con-

trolled circuit **100** is depicted conceptually by a voltage difference sensing phase **108**, an integration phase **110**, and a gain control phase **112**, as described herein.

[0041] The configurable circuit element **106** may include a transistor. For example, as shown in FIG. **1**A, a transistor M**1** may be coupled between the first terminal **102** and the second terminal **104**. A drain of the transistor M**1** may be coupled to the first terminal and a source of the transistor M**1** may be coupled to the second terminal **104**. Alternatively, the source of the transistor M**1** may be coupled to the first terminal **102** and the drain of the transistor M**1** may be coupled to the second terminal **104**. The transistor M**1** may be configured to operate in a linear (e.g., triode) or near-linear operating mode. For example, the transistor M**1** may be a zero threshold voltage transistor to enable the transistor M**1** to operate in a linear or near linear mode for large signal excursions. Operating the transistor M**1** in a linear or near linear mode enables the memory controlled circuit **100** to exhibit variable resistance between the first terminal **102** and the second terminal **104**, as controlled by a gate voltage of the transistor M**1**.

[0042] Although FIG. **1**A depicts the configurable circuit element **106** as a type of field effect transistor (FET), in other embodiments, the configurable circuit element **106** may be any type of three-terminal switch. For example, the configurable circuit element **106** may be an N-channel field effect transistor (FET), a P-channel FET, an NPN bipolar junction transistor (BJT), a PNP BJT, a junction gate field-effect transistor (JFET), or another type of three-terminal switch. In one embodiment the three-terminal switch includes a variable capacitor, as described further with reference to FIGS. **7**A and **7**B.

[0043] During operation, a voltage difference V_{AB} between the first terminal **102** and the second terminal **104** may be sensed as represented by the voltage difference sensing phase **108**. During the integration phase **110**, the voltage difference may be integrated over time. To illustrate, a value (or a "state" in terms of a synapse) stored at a dynamic analog memory may be increased or decreased based on an integration operation performed on the voltage difference V_{AB} over time. For example, the dynamic analog memory may include a capacitor, and the value (or state) may include a charge stored at the capacitor, as described further with reference to FIG. **1**B. The charge may be increased when the voltage difference V_{AB} exceeds a positive threshold and decreased when the voltage difference falls below a negative threshold. A particular embodiment of the implementation of the integration phase **110** and the dynamic analog memory are further described with reference to FIG. **1**B.

[0044] At the gain control phase **112**, the value of the dynamic analog memory may be used to configure the configurable circuit element **106**. For example, an electrical property of the configurable circuit element **106** may be changed based on the value. To illustrate, in embodiments where the configurable circuit element **106** includes the transistor M**1**, the value of the dynamic analog memory may be used to generate a gate voltage at the transistor M**1**. A resistance between the drain and the source of the transistor M**1** (and also between the first terminal **102** and the second terminal **104**) may be changed based on changes to the gate voltage. For example, depending on the particular implementation, an increase in the gate voltage may result in a decrease in resistance between the drain and the source and a decrease in the gate voltage may result in an increase in resistance between the drain and the source.

[0045] The synapse-type memory controlled circuit **100** may provide a floating variable resistance between the first terminal **102** and the second terminal **104** controlled by a memory element (e.g., the dynamic analog memory). If a positive voltage is applied across the memory controlled circuit (if a voltage at the first terminal **102** is greater than a voltage at the second terminal **104**) then the gate voltage is increased. The increase in the gate voltage may result in a decrease of resistance between the first terminal **102** and the second terminal **104**. Hence, the synapse-type memory controlled circuit **100** is "programmed." Similarly, if a negative voltage is applied across the memory controlled circuit (if a voltage at the first terminal **102** is less than a voltage at the second terminal **104**) then the gate voltage is decreased. The decrease in gate voltage may result in an increase of resistance between the first terminal **102** and the second terminal **104**. Hence the synapse-type memory controlled circuit **100** is "erased." As such, the synapse-type memory controlled circuit **100** may exhibit the dynamic functionality of a fourth fundamental circuit element (i.e., in addition to a resistor, a capacitor, and an inductor) called a "memristor". The synapse-type memory controlled circuit **100** may further substantially mimic a wide variety of biological synapses found in animal brain and neuro-muscular system, and may be used in conjunction with biologically compatible plasticity learning rules including spike-timing dependent plasticity (STDP), anti-STDP, and Hebbian-type learning.

[0046] Referring to FIG. **1**B, a circuit implementation of an embodiment of the synapse-type memory controlled circuit **100** is depicted. The memory controlled circuit **100** may include a transconductor **120**, a switch **122**, and a dynamic analog memory, such as a capacitor **124**. The transconductor **120**, the switch **122**, and the capacitor **124** may realize the functionality described with reference to FIG. **1**A. For example, the transconductor **120**, the switch **122**, and the capacitor **124** may each perform portions of operations corresponding to the voltage difference sensing phase **108**, the integration control phase **110**, and the gain control phase **112**, of FIG. **1**A, as described herein.

[0047] In the embodiment depicted in FIG. **1**B, the transconductor **120** may be configured to sense a voltage difference between the first terminal **102** and the second terminal **104** and to generate a current based on the voltage difference. For example, the transconductor **120** may include a circuit that implements a voltage controlled current source (VCCS). The VCCS may include an operational transconductor amplifier (OTA), a differential amplifier, a single-ended transconductor, or another type of transconductor circuit. The transconductor **120** may be further configured to transmit the generated current to the switch **122**.

[0048] The switch **122** may be coupled to an output of the transconductor **120** and to the capacitor **124**. The position of the switch **122** within the synapse-type memory controlled circuit **100** may enable the switch **122** to electrically connect the transconductor **120** to the capacitor **124** and to electrically disconnect the transconductor **120** from the capacitor **124** based on an external strobe Φ**1** received at the switch **122**. For example, when the external strobe Φ**1** is a logical high, the switch **122** may be configured to electrically couple an output of the transconductor **120** to the capacitor **124**. When the external strobe Φ**1** is a logical low, the switch **122** may be configured to electrically uncouple the output of the transconductor **120** from the dynamic analog memory **124**.

[0049] The capacitor **124** may be coupled to an output of the switch **122** and to an input of the configurable circuit element **106**. The input of the configurable circuit element **106** may be a control input of the configurable circuit element **106**. For example, in embodiments where the configurable circuit element **106** includes the transistor M1, the control input may correspond to a gate of the transistor M1. The capacitor may also be coupled to a common voltage (e.g., a ground voltage) to enable the capacitor to store a charge at the input of the configurable circuit element **106**. The charge may be used to store a value (or state) of the synapse-type memory controlled circuit **100**. The value may control an electrical property of the configurable circuit element **106**. For example, in the embodiment shown in FIG. **1**B, the value may control a resistance of the configurable circuit element **106**.

[0050] The capacitor **124** may include any type of capacitive element. For example, the capacitor **124** may include an N-channel capacitor, a P-channel capacitor, a MOSCAP poly-poly capacitor, a reversed biased diode, or another type of capacitive element. In one embodiment, a capacitance value of the capacitor is between about 100 femtofarads to five picofarads when implemented on a complementary metallic oxide semiconductor (CMOS) chip. Although FIG. **1**B depicts the dynamic analog memory as being the capacitor **124**, in other embodiments, the dynamic analog memory may include other types of memory usable to store an analog value.

[0051] During operation, the transconductor **120** may sense a voltage difference between the first terminal **102** and the second terminal **104**. Based on the voltage difference, the transconductor **120** may generate a current at an output of the transconductor **120**. The switch **122** may receive the generated current.

[0052] As described above, the switch **122** may be controlled by the external strobe Φ**1**. When the strobe Φ**1** is a logical high, the switch **122** may electrically couple the output of the transconductor **120** to the capacitor **124**, thereby enabling the current generated by the transconductor **120** to be applied to the capacitor **124**. The generated current may change a charge at the capacitor **124**. For example, the value of a charge held at the capacitor **124** may be increased or decreased based on the current generated by the transconductor **120**. Applying the generated current to the capacitor **124**, and thereby generating a voltage at the capacitor **124**, may have the effect of integrating the voltage difference sensed by the transconductor **120** over time with an effective gain k. Hence, the current integration phase **108** described with reference to FIG. **1**A may be performed.

[0053] When the external strobe Φ**1** is a logical low, the capacitor **124** may be electrically disconnected from the transconductor **120** and may hold a value (or state) as a stored charge, thus exhibiting the characteristics of the dynamic analog memory.

[0054] For synchronous operations, the external strobe Φ**1** may be provided by a system clock. This configuration may be useful in machine learning applications that synchronously process data. Alternatively, in a bio-inspired spiking neural network (SNN), neurons may fire asynchronously based on sparse spiking input patterns. In an asynchronous application the strobe Φ**1** may be generated using spiking inputs (or "action potentials" in terms of a synapse) applied to the synapse-type memory controlled circuit as described further with reference to FIG. **4**.

[0055] The value of the dynamic analog memory (e.g., the value of the charge stored at the capacitor **124**) may control the configurable circuit element **106**. For example, in embodiments where the configurable circuit element **106** is the transistor M1, as illustrated by FIGS. **1**A and **1**B, a voltage stored at the capacitor **124** may control a gate voltage of the transistor M1. When the transistor M1 is operated in a linear or near-linear operating mode, the transistor M1 may perform the function of a memory controlled variable resistor between the first terminal **102** and the second terminal **104**. For example, the drain-source resistance of the transistor M1 may be altered by updating the gate voltage in response to voltage pulses applied across the first terminal **102** and the second terminal **104**. If square pulses are used, the incremental update in the gate voltage may be approximately given by

$$\Delta V_G = \frac{G_1}{C_1} V_{Pulse} \Delta T$$

[0056] where G1, C1, Vpulse and ΔT are the transconductance of the transconductor **120**, the capacitance of the capacitor **124**, the pulse height, and the pulse width, respectively. If the transistor M1 is in deep triode (e.g., within the linear operating mode), the current flowing through the synapse-type memory controlled circuit may be approximated by

$$I \approx KP \frac{W}{L} (V_{GS} - V_{THN}) V_{AB}$$

[0057] where V_{GS} and V_{THN} are the gate-to-source and threshold voltages, KP is the transconductance parameter, W is the width and L is the length of the gate of the transistor M1, and V_{AB} is the voltage difference between the first terminal **102** and the second terminal **104**. This results in a resistance between the first terminal **102** and the second terminal **104** that may be approximated by

$$R \approx \frac{1}{KP \frac{W}{L} (V_{GS} - V_{THN})}$$

[0058] If the source of the transistor M1 is pinned at a common-mode voltage VCM, then the conductance G (or the "weight" W in terms of synapses) between the first terminal **102** and the second terminal **104** may be approximated by

$$W \approx KP \frac{W}{L} (V_G - V_{CM} - V_{THN})$$

[0059] which shows a direct relation between the state VG and the synaptic weight W. Although, the transistor M1 is described with reference to FIGS. **1**A and **1**B as being in a linear operating mode, as CMOS technology scales, the saturation resistance for FET transistors may be lowered. Thus, the synapse-type memory controlled circuit **100** may exhibit the above described resistance even when the transistor M1 is in moderate saturation.

[0060] The synapse-type memory controlled circuit **100** of FIGS. **1**A and **1**B realizes a two-terminal variable resistor,

with incremental memory in a feedback loop, whose resistance is controlled by external electrical stimulus applied across the two terminals. The resistance of the synapse-type memory controlled circuit **100** can be altered by applying direct current (DC) or pulsed voltage or current across its terminals. The analog memory element (e.g., the capacitor **124**) stores the state unless changed by application of an external voltage or current, greater than a threshold. The synapse-type memory controlled circuit **100** may also act as a compact emulator for a fourth fundamental circuit element (i.e., in addition to a resistor, a capacitor, and an inductor) called a "memristor." The synapse-type memory controlled circuit **100** may have application in resistive memory devices (ReRAMs), and may substantially mimic spike-based learning and weight storage functionality of biological synapses found in an animal brain. The synapse-type memory controlled circuit **100** can be designed and fabricated using standard commercial CMOS technologies and may be used for realizing chip-scale circuits for implementing Machine learning algorithms and neurobiology-inspired electronic circuits that may emulate cognitive computing functionality of a biological brain.

[0061] While the transconductor **120**, the switch **122**, and the capacitor **124** may together perform operations corresponding to the voltage difference sensing phase **108**, the integration phase **110**, and the gain control phase **112** of FIG. **1**A, it should be understood that a single component of FIG. **1**B does not necessarily map to a single phase of FIG. **1**A. For example, a combination of multiple components (e.g., the capacitor **124** and the switch **122**) may perform at least a portion of a single phase (e.g., the current integration phase **110**).

[0062] FIGS. **2**A, **2**B, and **3** illustrate various simulation results of an embodiment of a synapse-type memory controlled circuit. The synapse-type memory controlled circuit of FIGS. **2**A, **2**B, and **3** may correspond to the synapse-type memory controlled circuit **100** of FIGS. **1**A and **1**B. For example, the synapse-type memory controlled circuit **100** of FIGS. **1**A and **1**B may exhibit the characteristics described with reference to FIGS. **2**A, **2**B, and **3**.

[0063] Referring to FIG. **2**A, a current-voltage hysteresis curve for a simulated embodiment of a synapse-type memory controlled circuit is depicted. For simulation purposes, the synapse-type memory controlled circuit was designed using a 130 nm CMOS process with a supply voltage of 1.2V, and simulated using foundry device models in Cadence Spectre. The synapse-type memory controlled circuit was swept with a sinusoidal input having a frequency of 1 MHz, an amplitude of 200 mV, and a common-mode DC offset (VCM) of 600 mV, while the strobe Φ**1** was held at a logical high (1.2 V). As shown by the current-voltage hysteresis curve, the circuit characteristics of the synapse-type memory controlled circuit exhibit a pinched hysteresis curve typical of a memristor.

[0064] Referring to FIG. **2**B, a state trajectory for the simulated embodiment of the synapse-type memory controlled circuit when swept with a sine-wave input at 1 MHz frequency is depicted. This waveform can be understood as successive voltage sweeps being applied to the synapse-type memory controlled circuit, to trace closely spaced analog memory states. As shown in FIG. **2**B, the circuit characteristics associated with the synapse-type memory controlled circuit exhibit memristor behavior. For example, FIG. **2** demonstrates that the synapse-type memory controlled circuit can hold analog memory states, which can be precisely controlled by external stimuli. Hence, the simulation corresponding to FIG. **2**B further confirms that the synapse-type memory controlled circuit may function as a memristor.

[0065] Referring to FIG. **3**, a pulsed characterization response of the simulated embodiment of the synapse-type memory controlled circuit showing monotonic incremental state control is depicted. The simulation results depicted in FIG. **3** show that the synapse-type memory controlled circuit exhibits a state retention property. The simulation was performed by applying a pseudorandom sequence with 100 mV pulses (Vpulse=100 mV) applied across the terminals of the synapse-type memory controlled circuit every 5 ns (ΔT=5 ns), where a drain of a transistor (corresponding to the transistor M**1** of FIGS. **1**A and **1**B) is tied to a common-mode voltage of 600 mV (VCM=600 mV) with 1 MHz clock rate. FIG. **3** shows that the gate voltage (or state), V_G, is incrementally updated based on a positive or negative pulse input. Since the weight updates of the synapses are monotonic with respect to the applied pulses (or spikes), the synapse-type memory controlled circuit may be used to store analog weights in a machine learning or spiking neural network circuit.

[0066] Referring to FIG. **4**, an embodiment of a synapse-type memory controlled circuit **400** with asynchronous weight update that is compatible with spike timing-dependent plasticity (STDP) learning mechanisms is depicted. The synapse-type memory controlled circuit **400** may correspond to the synapse-type memory controlled circuit **100** described herein. For example, the synapse-type memory controlled circuit **400** may include a first terminal **102**, a second terminal **104**, a configurable circuit element **106**, a transconductor **120**, a switch **122**, and a capacitor **124**. The synapse-type memory controlled circuit **400** may further include a strobe signal source, such as an event detector circuit **402**.

[0067] The event detector circuit **402** may be coupled to the first terminal **102** and the second terminal **104**. For example, a first input of the event detector circuit **402** may be coupled to the first terminal **102** and a second input of the event detector circuit **402** may be coupled to the second terminal **104**. An output of the event detector circuit **402** may be coupled to the switch **122**. The event detector circuit **402** may generate the strobe Φ**1**, and may be configured to provide the strobe Φ**1** to the switch **122**.

[0068] During operation, the event detector circuit **402** may asynchronously monitor a voltage difference between the first terminal **102** and the second terminal **104** and may generate the strobe Φ**1** when a particular condition occurs. For example, the strobe Φ**1** may have a logical high value when a voltage difference V_{AB} between the first terminal **102** and the second terminal **104** is greater than an upper threshold or is lower than a lower threshold.

[0069] The functioning of the hysteresis comparator **402** may be compatible with one or more spike dependent plasticity (STDP) learning rules observed in biological synapses, as described further with reference to FIGS. **6**A, **6**B, **7**A, and **7**B. The upper threshold and the lower threshold may be customized depending on a controlling hysteresis of the event detector **402**. Particular embodiments of a synapse-type memory controlled circuit with embodiments of event detectors are described further with reference to FIGS. **5**A and **5**B. Although, the synapse-type memory controlled circuit **400** is depicted in FIG. **4** as including the event detector **402** as the external strobe source, in other embodiments the synapse-

type memory controlled circuit **400** may include a system clock as the external strobe source.

[0070] Referring to FIG. **5**A, an embodiment of a synapse-type memory controlled circuit with an embodiment of an event detector is depicted and generally designated **500**. The circuit **500** may include a first terminal **102**, a second terminal **104**, a configurable circuit element **106**, a transconductor **120**, a switch **122**, and a capacitor **124**. The circuit **500** may also include an absolute difference circuit **530** and an asynchronous comparator **536**. In some embodiments, the absolute difference circuit **530** and the asynchronous comparator **536** may correspond to the event detector **402**.

[0071] The absolute difference circuit **530** may include a comparator **532** and an absolute value circuit **534**. A first input of the comparator **532** may be coupled to the first terminal **102** and a second input of the comparator **532** may be coupled to the second terminal **104**. An output of the comparator **532** may be coupled to the absolute value circuit **534**.

[0072] The asynchronous comparator **536** may be coupled to the absolute difference circuit **530** at a first input and to a threshold voltage at a second input. The threshold voltage may be determined based on a particular STDP implementation as may be known to persons of ordinary skill in the art having the benefit of this disclosure. An output of the asynchronous comparator **536** may be coupled to the switch **122**.

[0073] During operation, the absolute difference circuit **530** and the asynchronous comparator **536** may generate the strobe Φ**1** based on a voltage difference between the first terminal **102** and the second terminal **104**. For example, the comparator **532** may generate a positive signal or a negative signal related to the voltage difference between the terminals **102**, **104**. The absolute value circuit **534** may receive the positive or negative signal and may perform an absolute value function to generate a signal that represents a magnitude of the voltage difference. The asynchronous comparator **536** may compare the magnitude of the voltage difference to the threshold voltage. In response to the magnitude of the voltage difference exceeding the threshold voltage, the asynchronous comparator **536** may output a logical high signal as the strobe Φ**1**.

[0074] Referring to FIG. **5**B, an embodiment of a synapse-type memory controlled circuit with an embodiment of an event detector is depicted and generally designated **550**. The circuit **550** may include a first terminal **102**, a second terminal **104**, a configurable circuit element **106**, a transconductor **120**, a switch **122**, and a capacitor **124**. The circuit **550** may also include a comparator **540**, a first asynchronous comparator **542**, a second asynchronous comparator **544**, and a logical OR circuit **546**.

[0075] The comparator **540** may correspond to the comparator **532**. An output of the comparator **540** may be coupled to a first input of the first asynchronous comparator **542** and a first input of the second asynchronous comparator **544**. A first threshold voltage may be provided as an input to the first asynchronous comparator **542** and a second threshold voltage may be provided as an input to the second asynchronous comparator **544**. The first threshold voltage may correspond to a positive threshold voltage and the second threshold voltage may correspond to a negative threshold voltage. Outputs of the asynchronous comparators **542**, **544** may be coupled to the logical OR circuit **546**. The logical OR circuit **546** may be coupled to the switch **122**.

[0076] During operation, the comparator **540** may generate a positive signal or a negative signal related to the voltage difference between the terminals **102**, **104**. The first asynchronous comparator **542** may compare the voltage difference to the first threshold voltage. In response to the voltage difference exceeding the first threshold voltage, the first asynchronous comparator **542** may output a logical high signal. Likewise, the second asynchronous comparator **544** may compare the voltage difference to the second threshold voltage. In response to the voltage difference being less than the second threshold voltage, the second asynchronous comparator **544** may output a logical high signal. In response to a logical high signal from either of the asynchronous comparators **542**, **544**, the logical OR circuit **546** may generate a logical high signal as the strobe Φ**1**. It should be noted that in the embodiments depicted in FIGS. **5**A and **5**B, the voltage difference between the terminals **102**, **104** may be evaluated using either voltage or current mode differencing.

[0077] Referring to FIG. **6**A, an example of an STDP learning mechanism in a bio-inspired system **600** is depicted. The system **600** includes a pre-synaptic neuron **602**, a synapse-type memory controlled circuit **604**, and a post-synaptic neuron **606**. The synapse-type memory controlled circuit **604** may correspond to the synapse-type memory controlled circuit **400** of FIG. **4**. In particular, the synapse-type memory controlled circuit **604** may include the event detector **402** of FIG. **4**, which may be configured to function according to the STDP learning mechanism described herein.

[0078] The pre-synaptic neuron **602** may be coupled to a first terminal of the synapse-like memory controlled circuit **604** to enable a first signal (e.g., a first voltage spike **612**) to be received by the synapse-like memory controlled circuit **604** from the pre-synaptic neuron **602** at the first terminal. Similarly, the post-synaptic neuron **606** may be coupled to a second terminal of the synapse-like memory controlled circuit **604** to enable a second signal (e.g., a second voltage spike **614**) to be received by the synapse-like memory controlled circuit **604** from the post-synaptic neuron **606**.

[0079] During operation, the first voltage spike **612** may be generated by the pre-synaptic neuron and transmitted to the post-synaptic neuron **606** via the synapse-type memory controlled circuit **604**. In response to the first voltage spike **612**, the post-synaptic neuron **606** may generate the second voltage spike **614** and transmit the second voltage spike **614** to the pre-synaptic neuron **602** via the synapse-like memory controlled circuit **604**. Hence, the synapse-type memory controlled circuit **604** enables bi-directional communication between the pre-synaptic neuron **602** and the post-synaptic neuron **606**. The shape of the first voltage spike **612** and the second voltage spike **614** may be determined by a desired implementation of an STDP learning rule. In some embodiments, the second voltage spike **614** is comparable to Ca2+ mediated feedback signaling in biological neurons, which effectively update the efficiency (e.g., the weight) of synaptic receptors that bind with neurotransmitters released from synaptic vesicles of a pre-synaptic membrane.

[0080] A weight (e.g., a conductance between the first terminal and the second terminal) of the synapse-type memory controlled circuit **604** may be updated based on the first voltage spike **612** and the second voltage spike **614** as shown in FIG. **6**B. For example, an electrical property (e.g., a resistance/conductance) of a configurable circuit element of the synapse-type memory controlled circuit **604** may be changed based on a voltage difference between the first voltage spike **612** and the second voltage spike **614**, as described with reference to FIGS. **1**A and **1**B. In a particular STDP imple-

mentation, the weight may be updated based on the relative timing of the first voltage spike **612** and the second voltage spike **614**. For example, as depicted in FIG. **6**B, when the second voltage spike occurs before the first voltage spike ($\Delta t<0$), a weight change Δw may be negative. Further, when the first voltage spike occurs before the second voltage spike ($\Delta t>0$), the weight change Δw may be positive. In a particular embodiment, the weight is updated when Δt is within a threshold as described further with reference to FIGS. **7**A and **7**B.

[0081] Referring to FIGS. **7**A and **7**B, an example of STDP-type synaptic weight updates that depend on the relative timing of pre- and post-synaptic action potentials is depicted. FIG. **7**A illustrates a pre-synaptic action potential **702** being received after a post-synaptic action potential **704**, and FIG. **7**B illustrates a pre-synaptic action potential **752** being received before a post-synaptic action potential **754**. The pre-synaptic action potentials **704**, **752** may correspond to the first voltage spike **612** of FIG. **6**A and the post-synaptic action potentials **704**, **754** may correspond to the second voltage spike **614** of FIG. **6**.

[0082] Referring to FIG. **7**A, the relative timing of the pre- and post-synaptic action potentials **702**, **704** is converted to a potential difference ΔVm dropped across the synapse-type memory controlled circuit. When ΔVm exceeds a negative threshold, a weight of the synapse-type memory controlled circuit is decremented by an amount equal to Δw. If a time period between the pre-synaptic action potential **702** and the post-synaptic action potential **704** is too long, then ΔVm may not exceed the negative threshold and the weight will not be updated.

[0083] Referring to FIG. **7**B, the relative timing of the pre- and post-synaptic action potentials **752**, **754** is again converted to a potential difference ΔVm dropped across the synapse-type memory controlled circuit. When ΔVm exceeds a positive threshold a weight of the synapse-type memory controlled circuit is incremented by an amount equal to Δw. As in FIG. **7**A, if a time period between the pre-synaptic action potential **752** and the post-synaptic action potential **754** is too long, then ΔVm may not exceed the positive threshold and the weight will not be updated.

[0084] The STDP functionality described with reference to FIGS. **6**A, **6**B, **7**A, and **7**B may be performed by the synapse-type memory controlled circuit **400** of FIG. **4**. Further, the synapse-type memory controlled circuit **400** may be configurable to implement variants of STDP, which may be developed by the Computational Neuroscience community as will be apparent to persons of ordinary skill in the relevant art having the benefit of this disclosure.

[0085] Referring to FIG. **8**A, a conceptual block diagram for an embodiment of a synapse-type memory controlled circuit **800** is depicted. The memory controlled circuit **800** may include a first terminal **102** and a second terminal **104**. Further, the functionality of the memory controlled circuit **800** may be depicted conceptually by a voltage difference sensing phase **108**, an integration phase **110**, and a gain control phase **112**. The synapse-type memory controlled circuit **800** may include a variable capacitor **806** coupled between the first input **102** and the second input **104**. The conceptual operation of the synapse-type memory controlled circuit **800** may be similar to the conceptual operation of the synapse-type memory controlled circuit **100** described herein with the exception that a capacitance (instead of a resistance) between the first terminal **102** and the second terminal **104** may be controlled based on the voltage difference sensing phase **108**, the integration phase **110**, and the gain control phase **112**.

[0086] Referring to FIG. **8**B, a circuit implementation of an embodiment of the synapse-type memory controlled circuit **800** is depicted. The memory controlled circuit **800** may include the transconductor **120**, the switch **122**, and the dynamic analog memory, such as the capacitor **124**. The synapse-type memory controlled circuit **800** may further include the variable capacitor **806** of FIG. **8**A. The variable capacitor **806** may be a 3-terminal varactor (V_1), implemented using a MOS capacitor in accumulation or inversion mode. For example, the variable capacitor **806** may be implemented in CMOS technology, with a body or a source/drain of a transistor used as a controller.

[0087] The synapse-type memory controlled circuit **800** may operate in a similar manner as the synapse-type memory controlled circuit **100** described herein. For example, the transconductor **120** may sense a voltage difference between the first terminal **102** and the second terminal **104**. Based on the voltage difference, the transconductor **120** may generate a current at an output of the transconductor **120**. The switch **122** may receive the generated current. When a strobe $\Phi 1$ is a logical high, the switch **122** may electrically couple the output of the transconductor **120** to the capacitor **124**, thereby enabling the current generated by the transconductor **120** to be applied to the capacitor **124**. The generated current may change a charge at the capacitor **124**. When the strobe $\Phi 1$ is a logical low, the capacitor **124** may be electrically disconnected from the transconductor **120** and may hold a value (or state) as a stored charge, thus exhibiting the characteristics of the dynamic analog memory. The value of the dynamic analog memory (e.g., the value of the charge stored at the capacitor **124**) may control the variable capacitor **806**. For example, a voltage stored at the capacitor **124** may be used to increase or decrease a capacitance of the variable capacitor **806**.

[0088] The synapse-type memory controlled circuit **800** of FIGS. **8**A and **8**B may extend the memristor concept to a memcapacitor. The memcapacitor may be used as a capacitive synapse-type memory controlled circuit in a spiking neural network. When used in machine learning and neural network circuits, a capacitive synapse-type memory controlled circuit may result lower power consumption as compared to resistive synapse-type memory controlled circuits.

[0089] To realize large-scale neural inspired computing on silicon integrated circuits, the synaptic spikes described herein may include digital pulses instead of the analog-like action potentials with exponential tails as depicted in FIGS. **7**A and **7**B. Referring to FIG. **9**A, an embodiment of a synapse-type memory controlled circuit compatible with digital spikes is depicted and generally designated **900**. Like the embodiment described with reference to FIG. **1**B, the synapse-type memory controlled circuit **900** may include a first terminal **102**, a second terminal **104**, a configurable circuit element **106**, and a capacitor **124**. The circuit **500** may also include an STDP weight update circuit **930**.

[0090] The STDP weight update circuit **930** may sense digital pulses occurring at the terminals **102**, **104**, and may convert their relative timing into a change in a weight of the synapse-like memory controlled circuit **900**. For example, the STDP weight update circuit **930** may change a voltage across the capacitor **124** based on the relative timing.

[0091] Referring to FIG. **9**B, an embodiment of a synapse-type memory controlled circuit compatible with digital spikes is depicted and generally designated **950**. The synapse-type

memory controlled circuit **950** may include a first exponential decay circuit **932**, a first transconductor **933**, a first switch **934**, a second exponential decay circuit **935**, a second transconductor **936**, and a second switch **937**. The exponential decay circuits **932**, **935**, the transconductors **933**, **936**, and the switches **934**, **937** may correspond to the STDP weight update circuit **930**.

[0092] The first exponential decay circuit **932** may be electrically coupled between the first terminal **102** and the first transconductor **933**. An input of the first transconductor **933** may be coupled to the first exponential decay circuit **932** and an output of the first transconductor **933** may be coupled to the first switch **934**. Likewise, the second exponential decay circuit **935** may be coupled between the second terminal **104** and the second transconductor **936**. An input of the second transconductor **936** may be coupled to the second exponential decay circuit **935** and an output of the second transconductor **936** may be coupled to the second switch **937**. The first switch **934** may be controlled by a voltage at the second terminal **104** and the second switch **937** may be controlled by a voltage at the first terminal **102**. For example, a digital voltage pulse at the second terminal **104** may cause the first switch **934** to electrically couple an output of the first transconductor **933** to the capacitor **124** and the configurable circuit element **106**. Similarly, a digital voltage pulse at the first terminal **102** may cause the second switch **937** to electrically couple an output of the second transconductor **936** to the capacitor **124** and the configurable circuit element **106**.

[0093] During operation, a first digital pulse **940** (e.g., corresponding to a pre-synaptic spike) may be received at the first terminal **102**. The first digital pulse may be shortly followed by a second digital pulse **942** (e.g., corresponding to a post-synaptic spike). In response to the first digital pulse **940**, the first exponential decay circuit **932** may generate an exponentially decaying response voltage that gradually decays over a period of time. The first transconductor **933** may generate a current based on the exponentially decaying response voltage. When the second digital pulse **942** is received at the second terminal **104**, the first switch **934** may connect the generated current to the capacitor **124**, thereby changing a voltage level at the capacitor **124**. In an embodiment, the first transconductor **933** generates a positive current that increases a voltage across the capacitor **124**, thereby updating a weight of the synapse-type memory controlled circuit **950**.

[0094] In response to the second digital pulse **942**, the second exponential decay circuit **935** may generate a second exponentially decaying response voltage that gradually decays over a period of time. The second transconductor **936** may generate a second current based on the second exponentially decaying response voltage. When another digital pulse is received at the first terminal **102**, the second switch **937** may connect the generated current to the capacitor **124**, thereby changing a voltage of the capacitor and updating the weight of the synapse-type memory controlled circuit **950**. In an embodiment, the second transconductor **937** generates a negative current that decreases a voltage across the capacitor **124**.

[0095] A benefit of the embodiment of FIGS. **9**A and **9**B, is that STDP weight updates may be performed in response to digital pulses as opposed to systems that do not include the exponential decay circuits **932**, **935**. Hence, the synapse-type memory circuits **900**, **950** may be incorporated into digital integrated circuits. Other advantages and benefits of the circuits **900** and **950** will be apparent to persons of ordinary skill in the related art having the benefit of this disclosure.

[0096] Referring to FIG. **10**A, characteristic timing and waveforms of an embodiment of a synapse-type memory controlled circuit using digital spikes, as described herein, are depicted. The characteristic timing and waveforms may correspond to the embodiments of FIGS. **9**A and **9**B. As depicted in FIG. **10**A, a first waveform may correspond to a voltage V_A at a first terminal (e.g., the terminal **102**). A second waveform may correspond to a voltage Vp,exp corresponding to an exponentially decaying voltage generated by a first exponential decay circuit (e.g., the first exponential decay circuit **932**). A third waveform may correspond to a voltage V_B at a second terminal (e.g., the second terminal **104**). A fourth waveform may correspond to a voltage Vm,exp corresponding to an exponentially decaying voltage generated by a second exponential decay circuit (e.g., the second exponential decay circuit **935**). A fifth waveform V_G may correspond to a charge held by a capacitor (e.g., the capacitor **124**) and applied to a controller (e.g., a gate) of the configurable circuit element **106**.

[0097] The first waveform may include a voltage pulse **1002** (corresponding to a pre-synaptic pulse) at a time tpre. In response to the voltage pulse **1002**, the second waveform may include a voltage spike **1012** followed by an exponentially decaying voltage response with an amplitude of Ap and a time constant τp. The exponentially decaying spike may be sampled (e.g., by actuating the switch **934**) during a voltage pulse **1016** of the third waveform. In response to the sampling, a voltage increase **1024** may occur at the fifth waveform. For example, the exponentially decaying voltage response may be converted to a positive current by a transconductor (e.g., the transconductor **933**) and integrated onto a capacitor (e.g., the capacitor **124**) via a switch (e.g. the switch **934**). The voltage increase **1024** may be proportional to the voltage level Vp,exp integrated over the duration of the voltage pulse **1002** (e.g., the area **1018** under the curve Vp,exp).

[0098] In a similar manner, the voltage pulse **1016** may cause a voltage spike **1020** followed by an exponentially decaying voltage response in the fourth waveform with an amplitude Am and a time constant τp. The exponentially decaying voltage response may be sampled (e.g., by actuating the switch **937**) during a voltage pulse **1004** in the first waveform. In response to the sampling, a voltage decrease **1026** may occur at the fifth waveform. For example, the exponentially decaying voltage response may be converted to a negative current by a transconductor (e.g., the transconductor **935**) and integrated onto the capacitor (e.g., the capacitor **124**) via a switch (e.g., the switch **937**). The voltage decrease **1026** may be proportional to the voltage level Vm,exp integrated over the duration of the voltage pulse **1004** (e.g., the area **1022** under the curve Vm,exp). Thus, the weight corresponding to the synapse-type memory controlled circuit is updated by the relative timing of pre and post digital pulses. Further, in response to the pulse **1004**, the second waveform may include a second voltage spike **1014** followed by a second exponentially decaying voltage response. Hence, the operations described herein may be repeated as additional voltage pulses are received at terminals of a synapse-type memory controlled circuit.

[0099] Referring to FIG. **10**B, an STDP learning function exhibited by the embodiment of FIG. **11**A of a synapse-type memory controlled circuit using digital spikes is depicted. The sampling of exponential decay implements an exponen-

tial STDP learning function to enable fast convergence of spiking neural network learning algorithms. Further, the synaptic potentiation may be given by:

$$\Delta w_p \approx \frac{G_m}{C_1} A_p T_{pulse}$$

[0100] Where Gm is the transconductance of the transconductor **933**, C1 is the capacitance of the capacitor **124**, Ap is the amplitude of the decaying voltage spike **1012** and Tpulse is the width of the pulse **1002**. The synaptic depression may be given by:

$$\Delta w_m \approx -\frac{G_m}{C_1} A_m T_{pulse}$$

[0101] Where Gm is the transconductance of the transconductor **936**, C1 is the capacitance of the capacitor **124**, Am is the amplitude of the decaying voltage spike **1020** and Tpulse is the width of the pulse **1016**.

[0102] Referring to FIG. **11**, an embodiment of a synapse-type memory controlled circuit with an exponential decay circuit is depicted and generally designated **1100**. The synapse-type memory controlled circuit **1100** may correspond to the synapse-type memory controlled circuit **9**B. For example, the circuit **1100** may include terminals **102**, **104**, a configurable circuit element **106**, a capacitor **124**, a first switch **1112**, a second switch **1132**, a first transconductor **1110**, and a second transconductor **1130**. The first switch **1112** may correspond to the switch **934** and the second switch **1132** may correspond to the switch **937**. Also, the first transconductor **1110** may correspond to the first transconductor **933** and the second transconductor **1130** may correspond to the second transconductor **936**.

[0103] The circuit **1100** may further include a first voltage source **1102**, third switch **1104**, a first resistor **1106**, and a capacitor **1108**. The first voltage source **1102**, the third switch **1104**, the first resistor **1106**, and the capacitor **1108** may correspond to the first exponential decay circuit **932**. The circuit **1100** may further include a second voltage source **1122**, a fourth switch **1124**, a second resistor **1126**, and a capacitor **1128**. The fourth switch **1124**, the second resistor **1126**, and the capacitor **1128** may correspond to the second exponential decay circuit **935**. Hence, the exponential decaying responses may be implemented using capacitor charge and discharge circuits.

[0104] The first voltage source **1102** may correspond to a voltage level of a peak spike level. For example, referring to FIG. **10**A, the peak spike voltage level may correspond to the voltage A_P at time tpre. Likewise, the second voltage source **1122** may correspond to a second peak spike level such as the voltage A_B at time tpost.

[0105] The third switch **1104** may be controlled by a voltage at the first terminal **102**. For example, a controller of the third switch **1104** may be coupled to the first terminal **102**. The third switch **1104** may enable voltage at the capacitor **1108** to charge to the peak spike level when activated. To illustrate, when activated, the third switch **1104** may couple the capacitor **1108** to the first voltage source **1102**, thereby charging the capacitor **1108**. When the third switch **1104** is disabled or deactivated, the voltage at the capacitor **1108** may dissipate through the resistor **1106**. Similarly, the fourth switch **1124** may be controlled by a voltage at the second terminal **104**. The fourth switch **1124** may enable voltage at the capacitor **1128** to charge to the second peak spike level when activated and may enable the capacitor **1128** to discharge through the second resistor **1126** when deactivated.

[0106] In an embodiment, the first and second resistors **1106**, **1126** include transistors coupled with biasing circuits. The transistors may be biased to function in the triode region using voltage references Vrbiasp and Vrbiasm. Because the transistors are biased to place them in the triode region, the biasing circuit may causes the transistors to generate a resistance, thereby forming a first resistor **1106** and a second resistor **1126**.

[0107] During operation, the terminal **102** may receive a first digital pulse (e.g., a pre-synaptic pulse). In response to the first digital pulse, the third switch **1104** may activate, causing the capacitor **1108** to charge to a voltage level corresponding to the voltage Ap. When the first digital pulse terminates, the capacitor **1108** may discharge through the resistor **1106** with a time constant $\tau p = Rp\ Cp$, thereby generating a first exponentially decaying voltage Vp,exp. The exponentially decaying voltage Vp,exp may be converted to an exponentially decaying current proportional to the exponentially decaying voltage Vp,exp at the transconductor **1110**. Thereafter, the terminal **104** may receive a second digital pulse (e.g., a post-synaptic pulse). In response to the second digital pulse, the first switch **1112** may be activated, causing a connection between the transconductor **1110** and the capacitor **124** to be established, thereby altering a charge of the capacitor **124**. For example, if the transconductor **1110** generates a positive current, a voltage level of the capacitor **124** may be increased. If the transconductor **1110** generates a negative current, then a voltage level of the capacitor **124** may be decreased. When the second digital pulse terminates, the first switch **1112** may be deactivated.

[0108] Further in response to the second digital pulse, the third switch **1124** may be activated, causing the capacitor **1128** to charge to a voltage level corresponding to the voltage A_M. When the second digital pulse terminates, the capacitor **1128** may discharge through the resistor **1126** with a time constant $\tau m = Rm\ Cm$, thereby generating a second exponentially decaying voltage Vm,exp. The second exponentially decaying voltage Vm,exp may be converted to a second exponentially decaying current proportional to the second exponentially decaying voltage Vm,exp at the second transconductor **1130**. Thereafter, the terminal **102** may receive a third digital pulse. In response to the third digital pulse, the second switch **1132** may be activated, causing a connection between the transconductor **1130** and the capacitor **124** to be established, thereby altering a charge of the capacitor **124**. For example, if the transconductor **1130** generates a negative current, a voltage level of the capacitor **124** may be decreased. If the transconductor **1130** generates a positive current, then a voltage level of the capacitor **124** may be increased. When the third digital pulse terminates, the second switch **1132** may be deactivated. Thus, a value of a dynamic analog memory (e.g., the capacitor **124**) may be modified. Because the modification of the value of the voltage at the capacitor **124** is based on an exponentially decaying voltage, a difference between an original value of the capacitor **124** and the modified value may be based on a duration between a first time of the first digital pulse and a second time of the second digital pulse or

based on a duration between the second time of the second digital pulse and a third time of the third digital pulse.

[0109] Referring to FIG. **12**, an embodiment of a synapse-type memory controlled circuit with an exponential decay circuit is depicted and general designated **1200**. The circuit **1200** may include terminals **102**, **104**, a configurable circuit element **106**, a capacitor **124**, a first switch **1210**, a second switch **1230**, a first voltage source **1202**, a third switch **1204**, a first resistor **1206**, a capacitor **1208**, a second voltage source **1222**, a fourth switch **1224**, a second resistor **1226**, and a capacitor **1228**. The embodiment of FIG. **12** may further include a transconductor **120** and a fifth switch **122**.

[0110] An input of the first switch **1210** may be connected to the resistor **1206** and the capacitor **1208**. An output of the first switch **1210** may be coupled to a first input of the transconductor **120**. When activated, the first switch may connect the resistor **1206** and the capacitor **1208** to the transconductor **120**. Likewise, an input of the second switch **1230** may be connected to an output of the resistor **1226** and the capacitor **1228**. An output of the second switch **1230** may be connected to a second input of the transconductor **120**. When activated, the second switch **1230** may connect the resistor **1226** and the capacitor **1228** to the transconductor **120**. An output of the transconductor **120** may be coupled to the fifth switch **122**. The fifth switch **122** may be controlled by a strobe signal Φ**1**.

[0111] Hence, FIG. **12** depicts an embodiment of a STDP synapse-type memory controlled circuit where two transconductors (e.g., the transconductors **1110**, **1130** of FIG. **11**) are merged into the transconductor **120**. The transconductor **120** may sample the exponentially decaying response voltage Vp,exp when the second voltage pulse (e.g., a post-synaptic pulse V_B) is present at the terminal **104**. Similarly, the exponentially decaying response Vm,exp may be sampled when the first voltage pulse (e.g., a pre-synaptic pulse V_A) is present at the terminal **102**. An output current of the transconductor **120** may be integrated into the capacitor **124** in response to the strobe signal Φ**1**. In an embodiment, the strobe signal Φ**1** is configured to activate the fifth switch **122** when either the first or second digital pulse are present (e.g., Φ**1**=(V_A OR V_B)). In an alternative embodiment, the STDP synapse may not include the fifth switch **122** and alternative means may be used to integrate the current onto the capacitor **124**.

[0112] The STDP synapse-type memory controlled circuits disclosed thus far may realize short-term potentiation (e.g., an increase in weight) and depression (e.g., a decrease in weight) where the weights are stored in a capacitive memory that may be subject to leaks. The duration of storage at the dynamic analog memory may depend on the size of the capacitor and leakage associated with the configurable circuit element (e.g., the transistor), and may range from a few seconds to minutes. In some machine learning applications it may be desirable to hold the learned weights for a longer period of time. This can be realized by employing bi-stability in synapses where after short-term STDP learning, the weight is quantized to either a high or low binary state.

[0113] Referring to FIGS. **13**A and **13**B, embodiments of bi-stable synapse-type memory controlled circuits are depicted. FIG. **13**A depicts an embodiment of a bi-stable synapse-type memory controlled circuit **1300** as including terminals **102**, **104**, a configurable circuit element **106**, a capacitor **124**, and an STDP weight update circuit **1320**. The circuit **1300** also includes a bi-stable memory element **1322** coupled to the capacitor **124**.

[0114] The bi-stable memory element **1322** may include a weak bi-stable latch. For example, the bi-stable latch may be designed for large regeneration time-constants such that it doesn't interfere in the short-term STDP learning. Between digital or analog pulses (e.g., STDP pulses) the bi-stable memory element **1322** may steer the state of the synapse-type memory controlled circuit to either increase a voltage (e.g., a high conductance state) or decrease the voltage (e.g., a low conductance state).

[0115] The bi-stable memory element **1322** may be configured to stabilize a state of the capacitor **124** when activated. For example, the bi-stable memory element **1322** may hold a particular voltage (or draw the particular voltage a high or low value) at the capacitor **124** when activated. When deactivated, the bi-stable memory element **1322** may enable the capacitor **124** to discharge.

[0116] FIG. **13**B, depicts an embodiment of a bi-stable synapse-type memory controlled circuit **1350** where a first inverter **1332** and a second inverter **1336** are cross-coupled as a binary latch. The inverters **1332**, **1336** may include large time-constants resulting in delay times that may prevent the inverters **1332**, **1336** from interfering with short term STDP learning (e.g., updating the voltage at the capacitor **124** based on STDP pulses). The large time-constants or inverter delay can be realized by sizing transistors of the inverters **1332**, **1336** with large lengths and small widths, and/or starving the current available in the inverters. In an embodiment, a switch **1338** may deactivate the bi-stable memory element **1322** when either pre- or post-synaptic pulses are applied. For example, the bi-stable memory element **1322** may be deactivated in response to a strobe Φ**1**. The strobe may be set to a logical high in response to a pulse (e.g., V_A or V_B).

[0117] Referring to FIG. **14**, an embodiment of a system **1400** of synapse-type memory controlled circuits with a store and refresh scheme using an ADC/DAC combination is depicted. The system **1400** includes a cross-point array **1410**, an array of input neuron devices **1420**, an array of output neuron devices **1430**, and a store and refresh scheme **1450**.

[0118] The cross-point array **1410** may include a plurality of synapse-type memory controlled circuits organized in a cross-point configuration (using rows and columns) to form a dense neural network (ANN or SNN) layer or a machine learning data structure. Each synapse-type memory controlled circuit of cross-point array **1410** may correspond to a synapse-type memory controlled circuit such as the synapse-type memory controlled circuit **100** of FIGS. **1**A and **1**B, the synapse-type memory controlled circuit **400** of FIG. **4**, the synapse-type memory controlled circuit **500** of FIG. **5**A, the synapse-type memory controlled circuit **550** of FIG. **5**B, the synapse-type memory controlled circuit **900** of FIG. **9**A, the synapse-type memory controlled circuit **950** of FIG. **9**B, the synapse-type memory controlled circuit **1100** of FIG. **11**, the synapse-type memory controlled circuit **1200** of FIG. **12**, the synapse-type memory controlled circuit **1300** of FIG. **13**A, and/or the synapse-type memory controlled circuit **1350** of FIG. **13**B. As a non-limiting example, each synapse-type memory controlled circuit may include a first input **1462**, a second input **1464**, a configurable circuit element **1466**, a transconductor **1470**, a switch **1472**, and a capacitor **1474**. The plurality of synapse-type memory controlled circuits of the cross-point array **1410** may connect the array of input neuron devices **1420** to the array of output neuron devices **1430**.

[0119] To illustrate, the array of input neuron devices **1420** may include a first representative input neuron device **1422** and the array of output neuron devices may include a first representative output neuron device **1432**, a second representative output neuron device **1434**, a third representative output neuron device **1436**, and a fourth representative output neuron device **1438**. Further, the cross-point array **1410** may include a first representative synapse-type memory controlled circuit **1412**, a second representative synapse-type memory controlled circuit **1414**, a third representative synapse-type memory controlled circuit **1416**, and a fourth representative synapse-type memory controlled circuit **1418**. The first representative input neuron device **1422** may be connected to each of the representative output neuron devices **1432-1438** via a corresponding synapse-type memory controlled circuit of the representative synapse-type memory controlled circuits **1412-1418**. The number and/or configuration of the input neuron devices, output neuron devices, and synapse-type memory controlled circuits is for illustrative purposes only and may be varied within the scope of the present disclosure as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0120] The store and refresh scheme **1450** may include an analog-to-digital converter (ADC) **1480**, a digital-to-analog converter (DAC) **1482**, a memory array **1484**, and a controller **1486**. Each synapse-type memory controlled circuit of the cross-point array **1410** may be coupled to the store and refresh scheme **1450**. For example, the ADC **1480** and the DAC **1482** may be coupled to the capacitor **1474** and may enable reading from and writing to the capacitor **1474**. The memory array **1484** may include a long-term memory usable to store states associated with each of the synapse-type memory controlled circuits of the cross-point array **1410**. The controller **1486** may be configured to control the read and write processes of the ADC **1480** and the DAC **1482**.

[0121] During operation, a charge at the capacitor **1474**, if not continually updated, may leak away due to sub-threshold leakage at the switch **1472** as it is controlled by a strobe Φ1. In order to hold a value (or state) of the synapse-type memory controlled circuit, the value may be periodically read via the ADC **1480** and stored at the memory array **1484**. When needed, the value may be recalled from the memory array **1484** and stored at the capacitor **1474** via the DAC **1482**.

[0122] The system **1400** may operate at very high speeds (up to several GHz), which is beneficial for applications involving big data analytics. Since the system **1400** may be designed using CMOS technology, complicated fabrication steps are not needed to design large neural inspired computing chips. Hence, the system **1400** enables prototype applications targeted for conceptual memristor devices and/or elements. The system **1400** may also synergistically work with memristor devices for fast data processing and non-volatile storage of learned weights in a non-volatile device such as a conducting bridge type memristor, ReRAM, flash memory, and/or phase change memory.

[0123] Although, FIG. **14** depicts the cross-point array **1410** as including 20 synapse-type memory controlled circuits, in other embodiments, the cross-point array **1410** may include more or fewer than 20 synapse-type memory controlled circuits. Further, although FIG. **14** depicts the array of input neuron devices **1420** as including 5 input neuron devices, the array of input neuron devices **1420** may include more or fewer than five input neuron devices. Also, although FIG. **14** depicts the array of output neuron devices **1430** as including 5 output neuron devices, the array of output neuron devices **1430** may include more or fewer than five output neuron devices. It should be generally understood that the system depicted in FIG. **14** is for purposes of example only and that in other embodiments, the system may include many more input neuron device, output neuron devices, and synapse-type memory controlled circuits than depicted in FIG. **14**.

[0124] Although FIG. **14** depicts each synapse-type memory controlled circuit as including the transconductor **1470** and the switch **1472**, in one or more other embodiments the synapse-type memory controlled circuits may correspond to embodiments of the synapse-type memory controlled circuits that do not include the transconductor **1470**, and the switch **1472** as described with reference to FIGS. **9A-13B**. Further, in an embodiment, each synapse-type memory controlled circuit is configured to respond to analog STDP pulses as described herein. Alternatively, each synapse-type memory controlled circuit may be configured to respond to digital STDP pulses as described herein. To illustrate, one or more of the embodiments of synapse-type memory controlled circuits (such as the circuit **900**) may be coupled to one or more of the input neuron devices **1420** and to one or more of the output neuron devices **1430**. The synapse-type memory controlled circuit **900** may be configured to receive a first digital pulse from one of the input neuron devices **1420** and to pass the first digital pulse to one of the output neuron devices **1430**. The synapse-type memory controlled circuit **900** may also receive a second digital pulse from one of the output neuron devices **1430** and pass the second digital pulse to one of the input neuron devices **1420**. The synapse-type memory controlled circuit **900** may further change a value of the capacitor **124** based on the first digital pulse and the second digital pulse as described herein. Hence, either an analog synapse-type memory controlled circuit or a digital synapse-type memory controlled circuit may be used in conjunction with the cross-point array **1410**.

[0125] Although various embodiments have been shown and described, the present disclosure is not so limited and will be understood to include all such modifications and variations, both structural and operational, as would be apparent to one skilled in the art.

What is claimed is:

1. A memory controlled circuit comprising:

a configurable circuit element electrically coupled to a first terminal and to a second terminal;

a weight update circuit, wherein a first input of the weight update circuit is electrically coupled to the first terminal and a second input of the weight update circuit is electrically coupled to the second terminal; and

a dynamic analog memory electrically coupled to the configurable circuit element and to the weight update circuit.

2. The memory controlled circuit of claim **1**, wherein the weight update circuit comprises:

a first exponential decay circuit, an input of the first exponential decay circuit coupled to the first terminal;

a first switch, an input of the first switch coupled to an output of the first exponential decay circuit and an output of the first switch coupled to the dynamic analog memory, a controller of the first switch coupled to the second terminal;

a second exponential decay circuit, an input of the second exponential decay circuit coupled to the second terminal; and

a second switch, an input of the second switch coupled to an output of the second exponential decay circuit and an output of the second switch coupled to the dynamic analog memory, a controller of the second switch coupled to the first terminal.

3. The memory controlled circuit of claim **2**, wherein the first exponential decay circuit comprises:

a resistor;

a capacitor coupled to the resister; and

an third switch coupled to a voltage source, wherein a level of the voltage source corresponds to a peak spike level, wherein a controller of the third switch is coupled to the first terminal, wherein the third switch enables a voltage at the capacitor to charge to the peak spike level when activated, and wherein the voltage dissipates through the resistor when the third switch is disabled.

4. The memory controlled circuit of claim **3**, wherein the resistor includes a transistor coupled with a biasing circuit, wherein the biasing circuit causes the transistor to generate a resistance.

5. The memory controlled circuit of claim **2**, wherein the second exponential decay circuit comprises:

a second resistor;

a second capacitor coupled to the second resister; and

a fourth switch coupled to a second voltage source, wherein a level of the second voltage source corresponds to a second peak spike level, wherein a controller of the fourth switch is coupled to the second terminal, wherein the fourth switch enables a voltage at the capacitor to charge to the second peak spike level when activated, and wherein the voltage dissipates through the second resistor when the fourth switch is disabled.

6. The memory controlled circuit of claim **2**, wherein the weight update circuit further comprises:

a first transconductor coupled between an output of the first exponential decay circuit and an input of the first switch; and

a second transconductor coupled between an output of the second exponential decay circuit and an input of the second switch.

7. The memory controlled circuit of claim **2**, wherein the weight update circuit further comprises:

a transconductor, a first input of the transconductor coupled to an output of the first switch and a second input of the transconductor coupled to an output of the second switch,

wherein an output of the first exponential decay circuit is coupled to an input of the first switch and an output of the second exponential decay circuit is coupled to an input of the second switch.

8. The memory controlled circuit of claim **7**, further comprising:

a third switch coupled between the transconductor and the dynamic analog memory, a controller of the third switch coupled to a strobe signal source.

9. The memory controlled circuit of claim **1**, further comprising:

a bi-stable memory element coupled to the dynamic analog memory, the bi-stable memory element configured to stabilize a state of the dynamic analog memory when activated.

10. The memory controlled circuit of claim **9**, wherein the bi-stable memory element comprises:

a first inverter;

a second inverter; and

a switch, wherein the first inverter and the second inverter hold a particular voltage at the capacitor when the switch is activated, and wherein the capacitor discharges when the switch is deactivated.

11. The memory controlled circuit of claim **1**, integrated into a system of memory controlled circuits, the system including:

at least one input neuron device;

at least one output neuron device;

wherein the at least one input neuron device is coupled to the at least one output neuron device via the first terminal and the second terminal.

12. A method comprising:

receiving a first digital pulse at a first terminal;

receiving a second digital pulse at a second terminal;

in response to the second digital pulse, changing a value of a dynamic analog memory to a modified value, wherein a difference between the value and the modified value is based on a duration between a first time of the first digital pulse and a second time of the second digital pulse.

13. The method of claim **12**, wherein an electrical property of a configurable circuit element positioned between the first terminal and the second terminal changes based on the modified value of the dynamic analog memory.

14. The method of claim **12**, further comprising:

in response to receiving the first digital pulse, generating an exponentially decaying voltage; and

generating a current proportionally related to the exponentially decaying voltage; and

electrically coupling the current to the dynamic analog memory during the second digital pulse.

15. The method of claim **12**, further comprising:

receiving a third digital pulse at the first terminal; and

in response to the third digital pulse, changing a value of the dynamic analog memory to a second modified value, wherein a difference between the modified value and the second modified value is based on a duration between the second time of the second digital pulse and a third time of a third digital pulse.

16. The method of claim **15**, further comprising:

in response to receiving the second digital pulse, generating an exponentially decaying voltage;

generating a current proportionally related to the exponentially decaying voltage; and

electrically coupling the current to the dynamic analog memory during the third digital pulse.

17. The method of claim **12**, further comprising holding a voltage level of the dynamic analog memory at a bi-stable memory element.

18. A method comprising:

receiving a first digital pulse from a first neuron device;

passing the first digital pulse to a second neuron device;

receiving a second digital pulse from the second neuron device;

passing the second digital pulse to the first neuron device;

changing a value of a dynamic analog memory based on the first digital pulse and the second digital pulse.

19. The method of claim **18**, wherein changing the value of the dynamic analog memory comprises increasing the value when the first digital pulse is received before the second

digital pulse and decreasing the value when the first digital pulse is received after the second digital pulse.

20. The method of claim **18**, wherein a magnitude of changing the value of the dynamic analog memory is based on a duration between the first digital pulse and the second digital pulse.

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