ECE 309: Electronic Circuit Analysis I

Spring 2020

ECE Department, University of Delaware

Instructor : Dr. Vishal Saxena (Website)
Email : vsaxena@udel.edu
Class Schedule : Tu & Thu 11:00 AM - 12:15 PM
Class dates : Feb 11 – May 14, 2020
Final Exam : May 20, 2020 (2 hours duration)
Location : Kirkbride Hall #204
Office Hours : Tue & Thu, 2-3 PM or by appointment at DuPont 110B
Course Homepage : https://www.canvas.udel.edu
Piazza Site : https://piazza.com/udel/spring2020/20S-ELEG309/home

Prerequisites: ELEG205: Circuit analysis techniques (KVL and KCL, superposition, circuit transformation, Thévenin and Norton equivalents).

Textbook: Fundamentals of Microelectronics – Behzad Razavi, **2nd** Edition, Wiley, 2013.

Teaching Assistants:

Name	Email Address	Office Hours	Location
Abhishek Iyer	jeetshek@udel.edu	Tue 3:30-4:30 PM	I-Suite
Russell Stump	rstump@udel.edu	Thu 5:30-6:30PM	
Qi Cheng	qicheng@udel.edu	Wed 2:30-3:30 PM	

Course Outline: This course focuses on design and analysis of microelectronic circuits. At the end of the course, students will be able to design, analyze, and simulate analog microelectronic circuits comprised of a few transistors.

Course content:

- Basics of Semiconductor Physics (Chapter 2)
- Diode Models and Circuits (Chapter 3)
- MOS Transistors (Chapter 6)
- CMOS Amplifiers and Mirrors (Chapter 17)
- Bipolar Junction Transistors (Chapter 4)
- Bipolar Amplifiers and Mirrors (Chapter 5)
- Operational Amplifiers (Chapter 8)

Grading Scheme:
The overall course grade is derived as follows:

15% Homework/Participation
25% Laboratory Reports
40% Midterm Exams (2)
20% Final Exam

The **tentative** grading scale is as below.

		A	93 – 100%	A-	90 – 92.99%
B+	87 – 89.99%	B	83 – 86.99%	B-	80 – 82.99%
C+	77 – 79.99%	C	73 – 76.99%	C-	70 – 72.99%
D+	67 – 69.99%	D	63 – 66.99%	D-	60 – 62.99%
		F	0 – 59.99%		

Lab Requirements:
Lab experiments **must** be performed in groups of 3 (2 or 4 in exceptions) with a single report submission per group electronically through Canvas. **Each lab group must submit their own circuit data and unique report.**

Course Policies:

1. The course will include two midterm exams and a final exam, weekly homework assignments, and 6 labs with reports. The exams are individual and closed books and notes. The final exam will be comprehensive.
2. Requests for make-up exams will be subjected to the University policy.
3. Homework is collected in class and due at the beginning of class on the submission date. Homework and labs that are not submitted on time will not be accepted, and will be assigned a grade of zero.
4. You may consult with others on assignments, provided you only submit your attempt at the work. Identical assignments will receive a grade of zero and be considered as academic dishonesty.
5. Homework and exam scores become final one week after they are returned to the class.
6. Final exam will not be returned at the end of the semester.

Learning Outcomes: After completing this course, students can do the following:

a) Understand the difference between analog and digital signals
b) Understand the basics of semiconductor devices, carrier density, doping, drift and diffusion.
c) Understand p-n junction, depletion region, junction capacitance, forward bias operation, current equation.
d) Comprehend diode circuits such as rectifier, clipping/clamping circuits, and references.
e) Understand MOSFET construction and operation, I-V curves, cutoff, triode and saturation regions of operation.
f) Understand the FET CS, CG and SF amplifier topologies and their relative strengths.
g) Understand BJT device structure and operation, I-V curves, saturation and forward active regions of operation.
h) Understand the BJT CE, CB and EF amplifier topologies and their relative strengths.
i) Able to bias transistors using current mirrors or a resistor network, and understand the effect of base current.
j) Understand small-signal transistor models and is able to perform small-signal analysis of amplifiers to estimate low-frequency gain, input and output impedances.
k) Understand source (emitter) degeneration and effect on gain/linearity
l) Understand the relative strengths and weaknesses of FET and BJT circuits
m) Design and analyze Opamp based circuits.
n) Understand the effect of opamp non-idealities, gain-bandwidth product and settling time of feedback amplifiers.

o) Ability to use SPICE to analyze and analog circuit including DC operating point, parametric sweeps, and transient analysis.
p) Capable of breadboarding, troubleshooting, and characterizing analog circuits using Digilent hardware.
q) Able to generate concise and informative lab reports.

Student Responsibility:

1. You are expected to attend class regularly, to conduct yourself in a professional manner, and to always act with integrity.
2. You are responsible for all readings and lecture content unless otherwise specified by the instructor. If you miss class, it is your responsibility to obtain assignments and other information given on the days that you missed.
3. Please turn off/silent your phones in the class and don't sleep, text, web surf, or listen to music during the class.
4. Participate in discussions and in-class problem solving – Ask questions
5. Exams are individual effort – eyes stay on your answer sheet.
6. This is an important course and opens door to many exciting and rewarding career possibilities. Utilize this opportunity to learn and enjoy the material.

Honors Section

Honors students have additional assignments designed to deepen their understanding of the course material. For one assignment, students design and simulate an amplifier circuit. For another assignment, students read and write a brief summary on an article from the professional literature that aligns with the course learning objectives.

Academic Honesty:

Any evidence of copied lab reports, homework or dishonesty during tests will result in an academic dishonesty report in your record and the corresponding academic penalty as per the University policy. **NO EXCEPTIONS.**

Disability Support:

Any student who thinks he/she may need an accommodation based on a disability should contact the Office of Disability Support Services (DSS) office as soon as possible. The DSS office is located at 240 Academy Street, Alison Hall Suite 130, Phone: 302-831-4643, fax: 302-831-3261, DSS Website. You may contact DSS at dssoffice@udel.edu.

TENTATIVE COURSE OUTLINE

This is **tentative** schedule. The Canvas course page will supersede these dates.

Week	Day	Date	Topics	Readings
1	T	2/11	Course Introduction, Semiconductor Physics	Ch. 1
	R	2/13	Semiconductor Physics	Ch. 2
2	T	2/18	Semiconductor Physics	
	R	2/20	Diode Models and Circuits	Ch. 3
3	T	2/25	Diode Models and Circuits	
	R	2/27	Diode Models and Circuits	
4	T	3/3	Diode Models and Circuits	
	R	3/5	MOS Transistors Physics	Ch. 6
5	T	3/10	MOS Transistors Physics	
	R	3/12	MOS Transistors Physics	
6	T	3/17	CMOS Amplifiers	Ch. 7
	R	3/19	CMOS Amplifiers	
7	T	3/24	**Exam #1**	
	R	3/26	CMOS Amplifiers	
8	T	3/31	**Spring Break**	
	R	4/2	**Spring Break**	
9	T	4/7	CMOS Amplifiers	
	R	4/9	Bipolar Transistors Physics	Ch. 4
10	T	4/14	Bipolar Transistors Physics	
	R	4/16	Bipolar Transistors Physics	
11	T	4/21	Bipolar Amplifiers	Ch. 5
	R	4/23	**Exam #2**	
12	T	4/28	Bipolar Amplifiers	
	R	4/30	Bipolar Amplifiers	Ch. 9
13	T	5/5	Operational Amplifiers	Ch. 8
	R	5/7	Operational Amplifiers	
14	T	5/12	Operational Amplifiers	
	R	5/14	Operational Amplifiers	
5/20			**Final Exam**	

LAB SCHEDULE

This is **tentative** schedule. The Canvas course page will supersede these dates.

Week	Laboratory	Dates	Report Due
1,2	1-Introduction to Spice and the Experimental Setup	Feb 11- Feb 23	Feb 24, 11:55PM
3,4	2-Diode Characterization	Feb 24-Mar 8	Mar 9, 11:55PM
5,6	3-Rectifier and Regulator Circuits	Mar 9- Mar 22	Mar 23, 11:55PM
7,9	4-MOSFET Characterization and Amplifier Design	Mar 23-Apr 12	Apr 13, 11:55PM
8	Spring Break		
10,11	5-BJT Characterization and Amplifier Design	Apr 14- Apr 28	Apr 27, 11:55PM
12,13	6-Opamp Circuits and Non-idealities	Apr 27-May 13	May 14, 11:55PM

Lab Instructions:

- Lab experiments **must** be performed in groups of 3 (2 or 4 in exceptions with the permission of the instructor) with a **single report** submission per group **electronically** through Canvas. The lab grade will be based on the lab report.
- You can work on the labs on you own schedule using your Digilent Board. However, the TAs will be available in the I-Suite during their office hours should you need assistance.
- Use the sample report posted on course site. **Each lab group must submit their own circuit data and unique report.** Each member of the group will receive the same grade for the report.
- Labs are due on the date specified in the table above. Lab reports that are not submitted on time will not be accepted, and will be assigned a grade of zero.
- The group must divide their work so that all students contribute equally and not copy data, writeup, or results from another group.
- Check out the Digilent Electronics Explorer Board from Tom Lum in the ECE storeroom (Evans 128/130). We have sufficient number of boards for each student to check out his own. All components needed for the labs are available in Evans 128.