Project 1

ECE 697 – Delta-Sigma Data Converter Design (Spring 2010)

Due on Tuesday, April 6, 2010.

1 Problem Statement

Design of a High-Fidelity Audio ADC: Commercial audio recording systems require very high resolution analog-to-digital conversion for stereo or quad audio input with a frequency range up to 200 KHz and over 100 dB dynamic range [1]. In this project, we will explore the design issues involved in the design of a $\triangle\Sigma$ modulator used in a commercial grade ADC with 24 KHz input. The modulator is to be implemented using TSMC 180-nm mixed-mode CMOS process (CM018) with a VDD=1.8 V supply voltage. [2]. The target specifications for the single-loop multi-bit audio $\triangle\Sigma$ modulator are as follows:

Table 1: $\triangle\Sigma$ ADC design specifications.

Parameter	Specified Value
Supply voltage, V_{DD}	1.8 V
Input signal bandwidth (f_B)	24 KHz, single channel
Resolution	24 bits
Dynamic range (after decimation)	$>$ 104 dB
-1 dB Total Harmonic Distortion + Noise[1] -20 dB -60 dB	-94 dB -78 dB -38 dB
Minimum Full-Scale (FS) input voltage	$0.6 \cdot V_{DD}$
Output sample rate (after decimation)	48 KHz
Maximum clock speed (f_{CLK})	12.288 MHz
Quantizer Range (fully-differential)	3 $V_{pp,diff}$

[1]Referred to the typical full-scale input voltage. For details on noise calculations in audio conversion systems refer to [3].

2 $\triangle\Sigma$ Modulator Design

It is understood that the design choices made in the decimation filter chain will affect the DR and resolution available from the ADC. However, your modulator should have enough design margin (10-20 dB excess SNR) to be able to meet the design requirements set for the overall ADC. The following steps will guide you through the design process:

1. **Design Space Selection:** Determine the order (L), OSR, the number of quantizer levels (nLev) and the out-of-band gain (OBG). The OSR is set by the maximum clock speed (12.288 MHz), but using the maximum clock rate will result in stringent power penalty in the loop-filter op-amps, quantizer and the DEM logic. Also a quantizer resolution larger than 5-bits is

impractical. A large OBG will result in a lower MSA and higher design sensitivity. Provide reasons for your choice of design space (L, OSR, nLev, OBG) and argue why is your choice is optimal.

2. **NTF Design:** Determine the NTF for your design while ensuring that it is a realizable transfer function. Describe the NTF optimized zero and pole placement.

   (a) Plot the impulse response $h[n]$ and show that $h[0] = 1$.

   (b) Plot the NTF magnitude response along with their pole-zero plots.

   (c) Estimate the MSA for your NTF and show the simulation result.

   (d) Plot the theoretical SNR, SNDR (in dB) vs amplitude (in dBFS), and mark peak-SNR, peak-SNDR, DR and SFDR on the plot.

3. **Loop-Filter Design:** Select a loop-filter architecture to implement the design NTF.

   (a) Since the audio ADCs have stringent harmonic distortion (THD) requirements and thus the architecture should be inherently a low-distortion topology.

   (b) The loop-filter is to be implemented using fully-differential switched capacitor circuits. Knowing that the op-amps in the integrators are linear only for roughly 50% of the V_{DD}, limit the integrator output range to 1.5 $V_{pp,diff}$ (peak to peak differential). Apply Dynamic Range Scaling (DRS) to ensure that the loop-filter states are bounded and the op-amps don't saturate.

   (c) Find the effective quantizer gain (k) using simulations and use this value to ensure that the STF is distortionless (e.g. $b_{N+1} = 1/k$). Also show that the modulator is stable with the quantizer gain variation (Hint: NTF root locus).

   (d) Find the loop-filter coefficients and quantize them to a realizable capacitor ratio. To quantify the degradation due to coefficient quantization, compare the original NTF response with the final one. Neatly tabulate the original and final loop-filter coefficients, and the required capacitor ratios.

   (e) Show the poles and zeros and magnitude response for $L_0(z)$, $L_1(z)$, $NTF(z)$ and $STF(z)$ with the selected loop-filter topology.

   (f) Simulate the resulting modulator topology in MATLAB showing its performance. Show that the modulator states lie in the linear range when the input is within the stable input range.

4. **Switched-Capacitor Design:** Map the designed loop-filter to a fully-differential switched capacitor topology.

   (a) Determine the required clock timing for the switches from the loop-filter difference equations.

   (b) Perform thermal noise analysis for the modulator and obtain the base capacitor value set by the kT/C noise with appropriate noise budgeting (show pie-chart) [4]. Determine all the capacitor values required to implement the range-scaled loop-filter. What is the total capacitance used in the design?

(c) Select optimal switch sizing to minimize thermal noise. At this point you may want to do preliminary noise simulations for basic transistor-level op-amp to find its input referred noise for the given settling requirements.

(d) Devise a Verilog-A behavioral model for the op-amp, emulating the non-ideal behavior due to the transistor level implementation. Your Verilog-A model should have op-amp f_{un}, A_{OL}, SR and other parameters as a function of the basic op-amp sizing. The op-amp outputs should be limited to the supply rails. You should be able to predict the power penalty in the op-amp depending upon the sizing. Also, initially model the quantizer with a Verilog-A code with a realistic delay. The idea is to let the Verilog-A models imitate the realistic transistor-level limitations set by the CMOS process in use.

(e) Neatly draw the loop-filter schematic in Cadence Virtuoso using the Verilog-A models. Make use of the config view to select pertinent schematic cell views. You may use ideal non-overlapping clock phases (ϕ_1 and ϕ_2) with realistic rise and fall times. Initially assume that the feedback DAC capacitors have no mismatch. If you employ double-sampling, use a fully-floating switched-capacitor integrator to avoid noise folding due to the sampling capacitor mismatch [5].

(f) Realizing that the input to the modulator is single-ended, use a single-ended to fully differential S/H stage in the front end. You may also want to explore bottom-plate sampling front-end to minimize switch non-idealities.

(g) **Extra work:** Design a non-overlapping clock generation circuit to drive the total load offered by the switches and quantizer employed in the modulator. Discuss if bootstrapped clock will be beneficial to drive the switches in this process.

5. **Ideal Schematic Simulation:**

(a) Simulate the ideal switched-capacitor loop-filter and compare its impulse response with the one simulated using MATLAB. Use PSS analysis in SpectreRF to simulate the frequency domain characteristics of the loop-filter [6, 7]. Ensure that the simulated loop-filter impulse response behaves as expected.

(b) Next, close the loop on the loop-filter and the quantizer and thus forming the modulator. Link your Spectre output to MATLAB in the Linux environment. Find the MSA using the slow-ramp input method and plot the results.

(c) By appropriately choosing an sinusoidal input frequency (i.e. $f_{in} = \frac{m}{N_{FFT}} f_s$), simulate the modulator schematic with an amplitude of $0.9\,MSA$. Plot the resulting modulator PSD with a 1024-point Hann window and compare the in-band SQNR with the results in part (3).

(d) Plot the waveforms at the output of each integrator (loop-filter states) and show that they don't go beyond the linear range (i.e. 1.5 $V_{\text{pp,diff}}$).

(e) Find the THD of the modulator for an input amplitude of -1 dB below MSA (i.e. 0.9 MSA).

6. **Schematic Simulation with circuit non-idealities:**

(a) Discuss how will you optimize the overall power consumption of the designed modulator when implemented in the selected CMOS process. Select appropriate sizing for each of the integrator stages depending upon your architecture. Set the appropriate values for f_{un} and A_{OL} in your op-amp models but use infinite slew rate. Make sure the 'golden' integrator in the loop-filter is appropriately sized. Also, the first integrator in the loop-filter should be sized to minimize the input referred noise and distortion. Repeat step (5) with this design model.

(b) Set finite slew-rate in the op-amp models (obtained from the transistor sizing information) and repeat step (5). What is the effect of the non-linear setting of the op-amps on the modulator performance and stability ?

(c) **Extra work:** Implement the most critical integrator and the front-end sample-and-hold (they may be the same depending upon your design choice) in your modulator using transistor-level circuitry. Characterize the modulator SNDR and THD limited by the non-idealities in this circuit block.

(d) **Extra work:** Replace the Verilog-A model for the quantizer (Flash ADC architecture) with a transistor level implementation. Using the transistor mismatch information from the process, estimate the offset variance in the comparator latch [8]. Study the effects of this offset on the overall modulator SNDR and argue if offset cancellation and a pre-amp are required in the quantizer. Simulate the performance of the modulator with this transistor-level quantizer (you may use ideal model of the loop-filter integrators to reduce simulation time).

You may additionally model other circuit non-idealities like switch non-linearity, clock jitter, quantizer non-idealities etc.

7. **DEM logic:** Explore the **simulateESL** function in the $\triangle\Sigma$ toolbox used for simulating element mismatch shaping algorithms.

(a) Find the typical capacitor mismatch in the process used for this design. Design an appropriate DEM logic to mitigate the errors due to feedback DAC non-linearity.

(b) Simulate your modulator with the capacitor mismatch, with and without element mismatch noise shaping. What is the resulting in-band SQNR?

(c) Comment on how would you implement this DEM logic in silicon.

(d) **Extra work:** Modify the feedback DAC model to include capacitor mismatch. Demonstrate the effectiveness of your DEM logic in the Cadence schematic using Verilog-A modeling.

3 Decimation Filter Design

Design a decimation filtering scheme involving a cascade of Sincs and/or IIR/FIR filters with a sharp roll-off. An example digital filter specification is shown in page 8 of reference [1]. Show the decimation filter schematic diagram. Filter the modulator output (in MATLAB) with the designed decimation filter and show the relevant spectra. Comment on the effects of filter coefficient

quantization. Estimate the resulting dynamic measurements (SNR, SNDR, etc.) of the overall ADC and see if you meet the specifications. Comment on how would you implement the decimated filter in silicon.

4 Simulink Modeling

Extra work: You may (optionally) model the designed $\triangle\Sigma$ modulator using the Simulink Delta-Sigma Toolbox [9] and plot relevant simulation results with circuit non-idealities and noise.

5 Final Report

Submit your neatly typed report in a two-column IEEE transactions format [10]. Lyx has the IEEE transactions template (IEEEtran) built-in. Show crisply drawn schematics and block diagrams drafted using a professional tool like Visio, besides your Cadence schematics. You may download the Visio schematic symbols from the course website [11]. Provide relevant references in your report. Show the modulator, decimation filter and the overall ADC performance in a neatly tabulated manner along with the conclusion. If possible, show the pie-chart for the estimated power consumption for each of the modulator circuit blocks.

References

[1] A 24-bit, 192 kHz Multi-bit Audio ADC: CS5430 Datasheet, Wesbite, Cirrus Logic, 2008.

[2] TSMC CM018 Mixed-Mode CMOS Process available through MOSIS. Models available online.

[3] Audio Conversion Systems Noise Calculations and Requirements, App. note AN263, Cirrus Logic, 2008.

[4] R. Schreier, J. Silva, J. Steensgaard, G. C. Temes,"Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits," *IEEE TCAS-I*, vol. 52, no. 11, pp. 2358-2368, Nov. 2005.

[5] K. Lee, J. Chae, G. C. Temes, "Efficient Fully-Floating Double-Sampling Integrator for $\Delta\Sigma$ ADCs," *Proc. IEEE Int. Symp. Circuits and Syst.(ISCAS)*, 2008.

[6] K. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," *Designer's Guide Community* [Online].

[7] K. Kundert, "Device Noise Simulation of Delta-Sigma Modulators," *Designer's Guide Community* [Online].

[8] Pelgrom et. Al., "Matching Properties of MOS Transistors," IEEE JSSC, vol. 24, no. 5, Oct. 1989 [Online].

[9] P. Malcovati, "Simulink Delta-Sigma Toolbox 2," Mathworks. Available [Online].

[10] IEEE Transactions Templates. Available [Online].

[11] Visio Schematic Symbols. Available [Online].