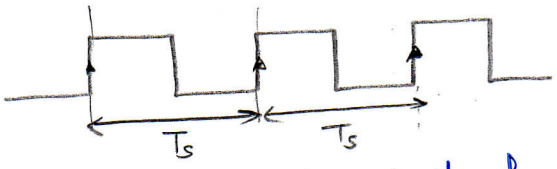
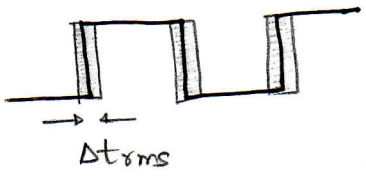
# Clock Jitter and its effect in ΔΣ modulators

So far we assumed that the sampling clock is ideal.
↳ i.e. every rising edge of the clock occurs exactly at the multiples of time $T_s$ = clock period.



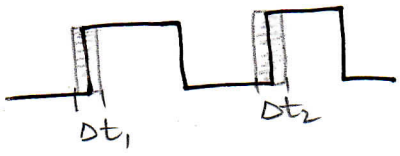

- Real oscillator → $T_s$ is not constant from cycle to cycle
  on the average, time period = $T_s$ with random variation around it.

- chop and superpose the clock on the same graph (like eye diagram)
  ↳ edges will coincide




→ mean = 0
variance → characterized by $\Delta t_{rms}$, i.e $\sigma = \Delta t_{rms}$

- $\Delta t_{rms}$ can be derived from the device noise in the clock generation circuit.

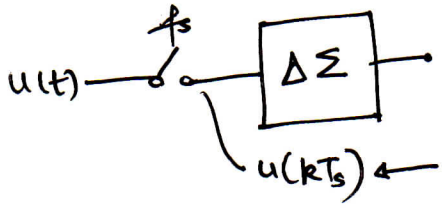



we assume that $\Delta t_1$ and $\Delta t_2$, etc. are uncorrelated with each other
⇒ PSD of the sequence of random variables is white ⇒ "white jitter" model.

- What happens to the behavior of the ΔΣ modulator when the clock is "jittery"?

# D-T ΔΣ Modulator

Sampling is done upfront




jittery sampled input = $u(kT_s + \Delta t_k) \simeq u(kT_s) + \boxed{\Delta t_k \cdot \left.\frac{du}{dt}\right|_{t=kT_s}}$ ← error due to jitter

Using Taylor's expansion and neglecting higher-order terms

Large error when the input is changing fast

## Sinusoidal input:

$$u = A\sin(\omega_{in} t)$$

$$\frac{du}{dt} = A\omega_{in}\cos(\omega_{in} t)$$

Mean square value of the error due to jitter $= E\left[\left\{\Delta t_k \cdot A\omega_{in}\cos(\omega_{in} t)\Big|_{kT_s}\right\}^2\right]$

$$= E[\Delta t_k^2] \cdot E[A^2\omega_{in}^2 \cdot \cos^2(\omega_{in} t)]$$

$$= E[\Delta t_k^2] \cdot \frac{A^2\omega_{in}^2}{2}$$

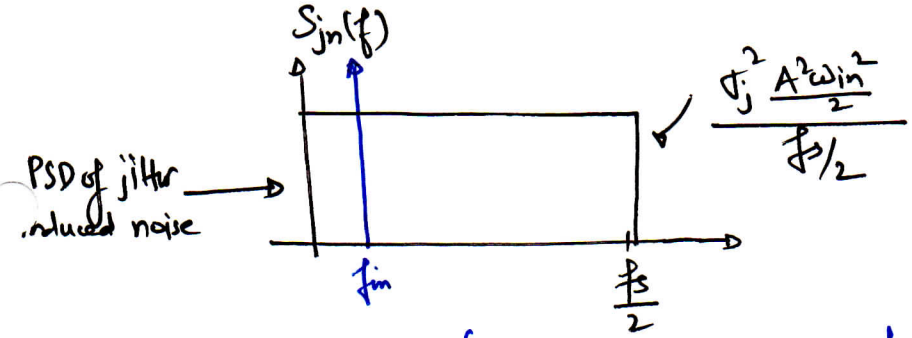
$$= \sigma_j^2 \cdot \frac{A^2\omega_{in}^2}{2}$$

Jitter limited SNR $= SNR_j = \dfrac{A^2/2}{\sigma_j^2 \cdot \frac{A^2\omega_{in}^2}{2}} = \dfrac{1}{\sigma_j^2 \cdot \omega_{in}^2}$ ($A^2/2 = P_S$)

$$\Rightarrow \boxed{SNR_j = -20\log_{10}(2\pi f_{in}\sigma_j) \text{ dB}}$$

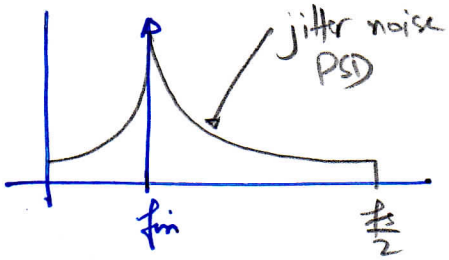
As the input frequency increase $\Rightarrow$ $SNR_j$ decreases.

$\Rightarrow$ fundamental limit on SNR in a sampling system.




- We model the 'white-jitter' noise to be uniformly spread from $f = [0, \frac{f_s}{2}]$.

- The jitter in a real clock generated on chip (using a Vco) is not white. see accumulated noise model in the Cherry's paper on jitter in CT ΔΣ modulators.



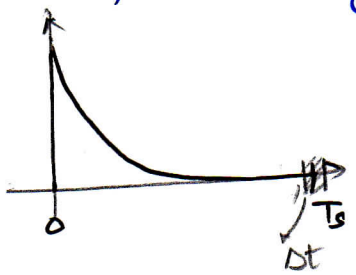

- For the oversampling case:

$$\text{In-band SNR due to jitter limitations} = \frac{1}{\sigma_j^2 \cdot \omega_{in}^2 \cdot OSR}$$

$$\Rightarrow SNR_j = -20 \log_{10}(2\pi f_{in} \sigma_j \cdot OSR)$$

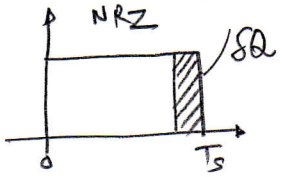
- In DT ΔΣ implemented using switched-capacitor circuits, the settling is exponential.

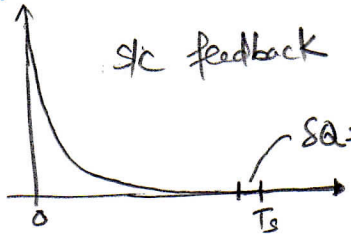
  ⇒ The feedback current (DAC) look like a fast exponentially decaying pulse.




  ⇒ The error in the amount of charge feedback due to the variation in DAC pulse-width ($T_s$) is negligible.

  ⇒ Effect of pulse width variation is ignored in DT DSM



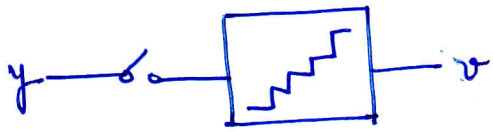

⇒ Straightforward in DT-DSM
↳ only sampling jitter.

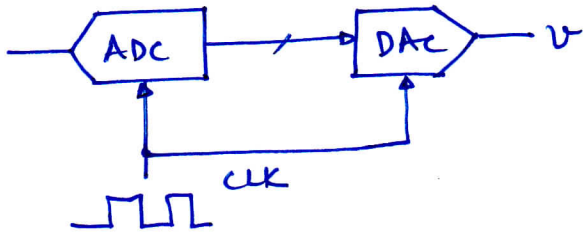
## CT ΔΣ Jitter:

- In a CT ΔΣ where does sampling occur?
  - The input is sampled inside the modulator after the loop-filter L(s), within the ADC.

**Digression:**

① The ideal sampler/quantizer is shown as:

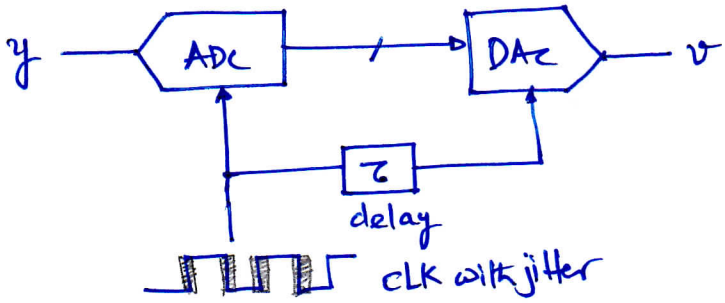



- same clock defines the sampling instances of the ADC as well as the DAC.

- Input is sampled in the ADC
  - ADC output is "sampled" by the DAC
    - the DAC puts out a pulse equivalent to the ADC output code.

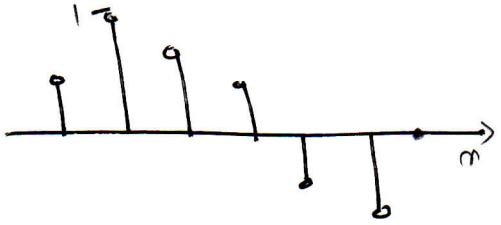
② The Real Sampler/Quantizer:

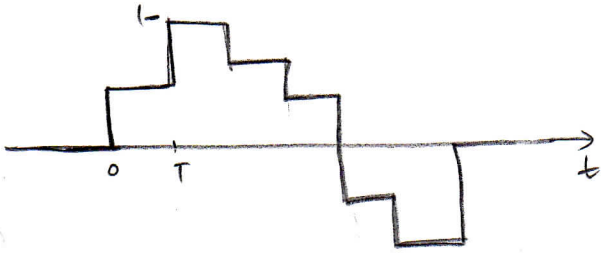



- ADC needs finite time for conversion
- DAC is clocked 'τ' delay later
- The clock is jittery.
- Also, to reduce the effect of DAC element mismatch DEM/DWA logic is used which introduces additional delay.

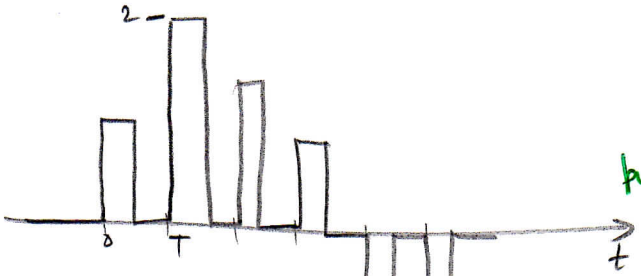
# Types of DACs

DAC input $v[n]$



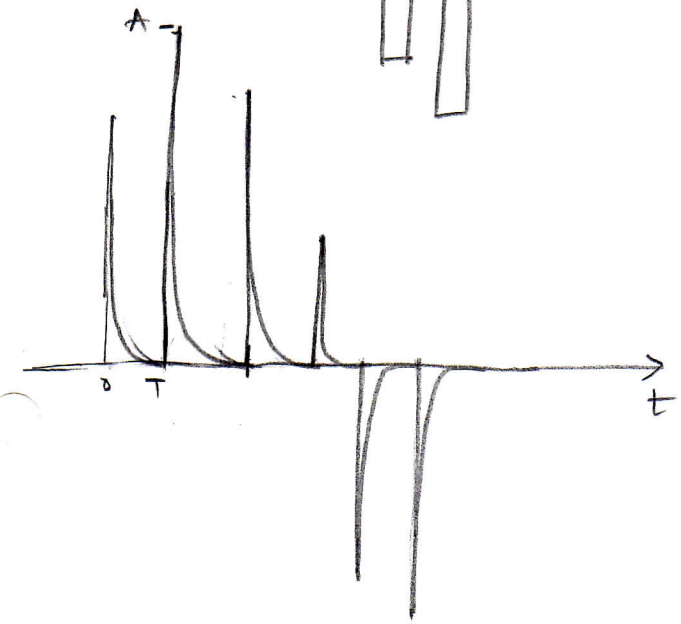




NRZ DAC output




RZ DAC output

pulse height is 2x than in NRZ

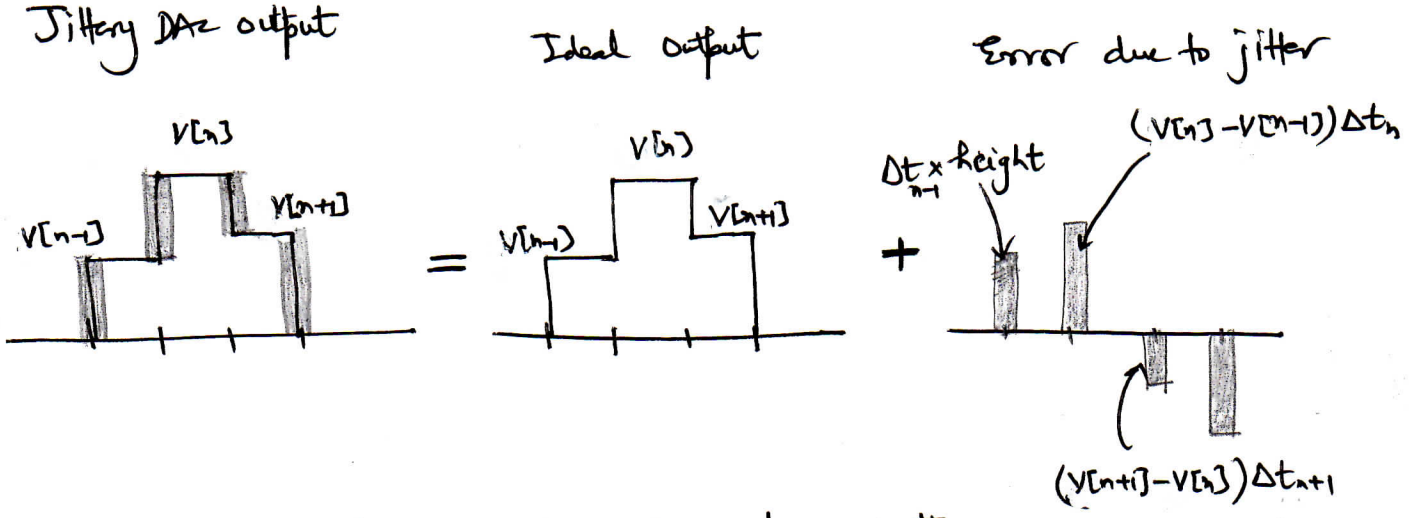



Switched-Capacitor DAC output

pulse height is much larger than NRZ DAC.

* There are many other DAC waveforms possible.

# Clock jitter in NRZ DACs

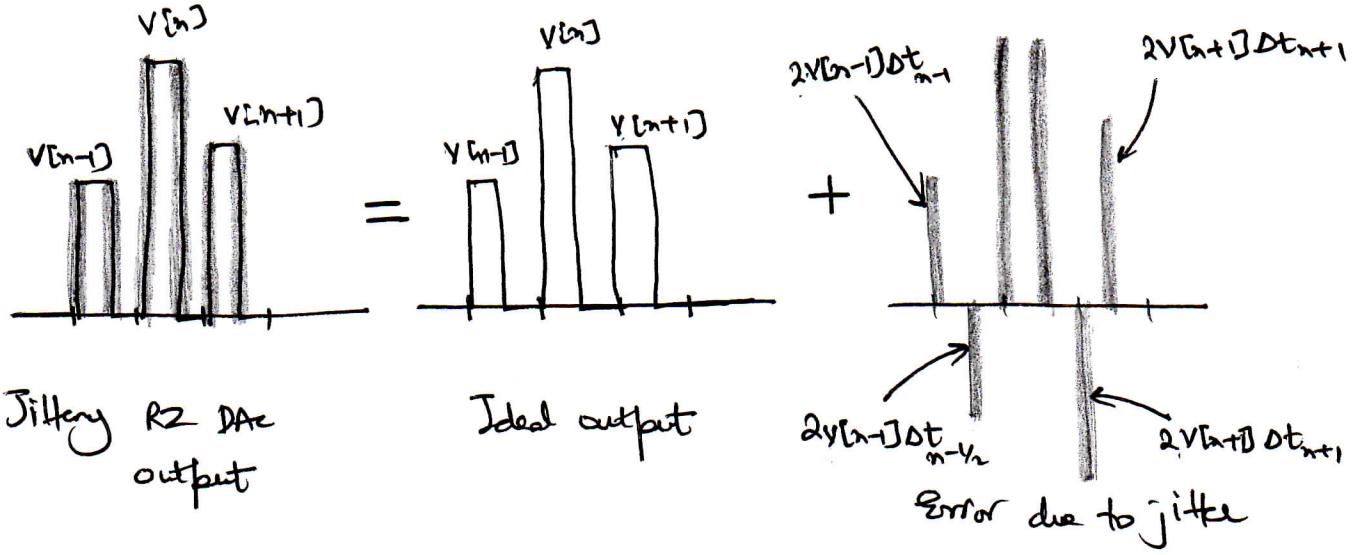



* Error waveform depends only on the change in the height
  - ↳ depends upon the jumps in the adjacent modulator output codes V[n]

* With multibit quantizer, the LSB jumps are smaller
  - ↳ error due to jitter is smaller

* Large OBG ⇒ larger jumps in the outputs
  - ↳ more error due to jitter.

Clock jitter in RZ DACs:




Jittery RZ DAC output

Ideal output

Error due to jitter

Comparison:

* Error depends upon the height and number of transitions in the DAC output waveform

* NRZ DACs have a transition height $(y[n]-y[n-1])$, one transition every $T_s$

* RZ DACs have a transition height $2y[n]$, two transitions every $T_s$.

* RZ DACs are Much more sensitive to clock jitter
  - ↳ 4x times worse than NRZ DACs
  - ↳ height is always fixed ⇒ no $\Delta y[n]$ benefit

* Multibit NRZ DACs have good jitter performance

* Switched-capacitor DACs have very small DAC reconstruction error but their pulse height is much larger ⇒ opamp slewing issues.

Effect of Jitter on SNR : Assuming NRZ DAC pulse

$$e_j[n] \triangleq \underbrace{(v[n] - v[n-1])}_{dv} \frac{\Delta t[n]}{T_s}$$

$\Rightarrow$ Noise variance

$$\sigma_{e_j}^2 = \sigma_{dv}^2 \cdot \frac{\sigma_{\Delta t}^2}{T_s^2}$$ → white noise process

$\Rightarrow$

$$v[n] = u[n] + e_q[n] \circledast h[n]$$ ← NTF's impulse response

↳ shaped quantization noise

$\Rightarrow$

$$V[n] - V[n-1] = U[n] - U[n-1] + (e_q[n] - e_q[n-1]) \circledast h[n]$$

Assuming slowly varying input, due to oversampling

$$U[n] \simeq U[n-1]$$

$$dv[n] = V[n] - V[n-1] \simeq (e_q[n] - e_q[n-1]) \circledast h[n]$$

$\Rightarrow$

$$\sigma_{dv}^2 \simeq \left(\frac{\sigma_{LSB}^2}{\pi}\right) \int_0^{\pi} |(1 - e^{-j\omega}) NTF(e^{j\omega})|^2 \cdot d\omega$$

$e_q[n]$ is a white sequence with mean square value $\sigma_{LSB}^2$

→ Parseval's theorem

$\Rightarrow$ The in-band noise due to jitter (J) is

$$J \simeq \frac{\sigma_{\Delta T_s}^2}{T_s^2} \cdot \frac{\sigma_{LSB}^2}{\pi \, OSR} \int_0^{\pi} |(1 - e^{-j\omega}) NTF(e^{j\omega})|^2 \cdot d\omega$$

$$J = \frac{\sigma^2_{\Delta T_s}}{T_s^2} \cdot \frac{\sigma_{LSB}^2}{\pi OSR} \int_0^{\pi} |(1-e^{j\omega}) NTF(e^{j\omega})|^2 \cdot d\omega$$

Observations:

* The NTF at high frequencies ($\omega = \pi$) contributes most to J

  $\Rightarrow$ NTFs with high OBG result in more jitter noise

* Smaller LSB, leads to less jitter noise $\Rightarrow$ multibit NRZ modulators are less sensitive to jitter.

* $\left(\frac{\sigma^2_{\Delta T_s}}{T_s^2}\right)$ is more significant at higher sampling frequencies when $T_s$ is small and $\sigma^2_{\Delta T_s}$ is nearly fixed.
  ↳ depends upon the clock source.

## Example Calculations:

Assume audio CTΔΣ modulator, BW = 24 kHz

* OSR = 64, $\Rightarrow f_s = 3.072$ MHz, N = 4 bit quantizer

* Maximum input range of quantizer = 2V

$\Rightarrow$ LSB size $= \frac{2}{16} \Rightarrow \sigma^2_{LSB} = \frac{\Delta^2}{12} = \frac{(2/16)^2}{12}$

* Assume a clock source with 100 ps RMS jitter

$\Rightarrow \sigma_{\Delta T_s} = 100$ ps

Solving the integral we get

$$J = (1.28\,\mu V)^2$$

$$MSA = 0.83\ V_{pk}$$

$\Rightarrow$ Signal to jitter noise ratio

$$SJNR = 20 \log \left( \frac{0.83/\sqrt{2}}{1.28\,\mu V} \right) = 113.13$$

$\Rightarrow$ 100 ps rms jitter is not an issue for 15-bit resolution.

Reference: Reddy [2007]