Final Exam

ECE 697 – Delta-Sigma Data Converter Design (Spring 2010)

Due on Thursday, May 15, 2010

Instructions:

1. State all assumptions clearly and attach all the MATLAB code used. List all the references used in your solutions.
2. Work out all the algebra and present in a neat manner. All the figures and graphs should be annotated and properly labeled.

Problem 1 DT $\Delta\Sigma$ **Modulator** Design:

1. Design NTF of a single-bit, second-order $\Delta\Sigma$ modulator with OSR=16, and OBG=1.5. Plot the magnitude response and pole-zero plot for both the NTF.
2. Map the synthesized NTF to a **CRFB** topology. Simulate the modulator and estimate the in-band SQNR and the MSA.
3. Implement the above single-bit modulator using switched-capacitor topology. Assume that TSMC 180-nm process is used with V_{DD}=1.8 V, and the clock frequency is 100 MHz.
   (a) The integrators outputs should be range scaled to less than 50% of the supply rails (i.e. $x_{max} = 0.9$). For this single-bit design, you may select the quantizer reference voltage $V_{ref} = x_{max}$.
   (b) Determine the value of the capacitances used in the topology after appropriate noise budgeting. You may ignore the input referred noise of the op-amps.
   (c) Show the schematic and the timing diagram. The timing should satisfy the modulator design equations.
4. What changes would you make to the schematic and the timing diagram if the modulator topology is changed to **CIFB**?
5. List at least five reasons to convince your Manager that a multi-bit DSM design offers substantial improvement over its single-bit counterpart.
   (a) Using plots, show improvement in the SNR and stability for the design in this problem as the quantizer resolution is gradually increased to 5-bits.
   (b) How would you mitigate the errors arising due to the non-linearity in the multi-bit feedback DAC?

Extra Credits: Simulate the modulator using Cadence Spectre and verify its operation.

Problem 2 CT $\Delta\Sigma$ Modulator Design:

1. In this problem, a second-order CT $\Delta\Sigma$ modulator will be designed using the NTF designed in problem (1). Initially, assume that the design is normalized to a clock frequency (f_s) of 1 Hz.
   (a) Assuming an **NRZ** DAC pulse-shape and a **CIFF** architecture, determine the loop-filter coefficients $\{k_1, k_2, \gamma_1\}$ for the continuous-time loop-filter $\hat{L}(s)$. Here, γ_1 is the local feedback coefficient used to realize the resonator. Can you do this mapping using the impulse-invariant transform (IIT) tables?
   (b) Initially assume that the excess loop delay (τ) is zero. Sketch the loop-filter block diagram.
   (c) Plot the CT and sampled loop-responses $l(t)$ and $l[n]$ respectively for the CT-DSM.
2. Determine the $STF(e^{j\omega})$ for your design and plot the spectrum. Can you explain the out of band peaking in the STF?
3. Now, due to design considerations an excess loop delay (ELD) of 60% of the clock-period is introduced (i.e. $\tau = 0.6$).
   (a) Find the equivalent $NTF(z)$ and plots its response and the pole-zero plot. What do you observe?
   (b) Plot $l(t)$ and $l[n]$ for the CT-DSM with the excess loop-delay.
4. Find a method to compensate for the ELD so that the NTF is restored to the response seen in part (1).
   (a) Show that the direct path in the loop-filter arising due to the ELD compensation, can be realized as a direct feedback path around the quantizer. Find the resulting loop-filter coefficients $\{k_0, k_1, k_2, \gamma_1\}$. Can you do this mapping using the impulse-invariant transform (IIT) tables or using the direct computation method discussed in class?
   (b) Plot $l(t)$ and $l[n]$ for the CT-DSM, and demonstrate that the effect of the ELD is fixed.
5. Implement the above single-bit modulator using active-RC filter topology. Assume that TSMC 180-nm process is used with V_{DD}=1.8 V, and the clock frequency is 100 MHz.
   (a) Time-scale the CT DSM to operate it at a clock frequency (f_s) of 100 MHz.
   (b) The integrators outputs should be range scaled to less than 50% of the supply rails (i.e. $x_{max} = 0.9$). For this single-bit design, you may select the quantizer reference voltage $V_{ref} = x_{max}$.
6. Assuming a 30% variation in the RC time-constant variation across different die, plot the worst case equivalent $\left|NTF(e^{j\omega})\right|$ and compare it with the nominal NTF magnitude response. Suggest a method to tune the CT DSM in the presence of these RC variation.

Extra Credits: Simulate the modulator using Cadence Spectre and verify its operation.

Problem 3 MASH Simulation: Study section 9.3 in the text-book [Schreier 2005] and go through the MATLAB simulation of a 2-0 MASH.

1. Synthesize a low-distortion, second-order DSM as seen in Figure 4.23 in the text-book to be used as the first stage of the MASH.

2. Implement a 2-2 MASH using the above low-distortion topology and thus avoiding an analog subtraction block. The design specifications as same as in the book example and are listed in Table 1.

   (a) Judiciously select the quantizer resolution in each stage and present reasoning. Discuss if you would require DEM logic to mitigate the effects of feedback DAC non-linearity in any of the stages?

   (b) Employ an inter-stage coupling coefficient to ensure that the output of the first stage lies within the MSA range of the second stage.

3. What are the possible sources of error resulting in the first-stage noise leakage into the output? Simulate and plot the degradation in the SQNR due to finite op-amp gain.

Parameter	Symbol	Value	Units
Signal Bandwidth	f_B	1.25	MHz
Sampling Frequency	f_s	20	MHz
Signal-to-Noise Ratio	SNR	90	dB
Supply voltage	VDD	5	V
Input voltage range		[-2,2]	V

Table 1: Specifications for the 2-2 MASH design.

Problem 4 CT $\Delta\Sigma$ Modulator AAF and Jitter Analysis

1. For a generalized CT $\Delta\Sigma$ modulator illustrated in Figure 1, show that the overall CT signal transfer function ($STF_C(j\omega)$) is given by

$$STF_C(j\omega) = L_0(j\omega) \cdot NTF(e^{j\omega}) \tag{1}$$

   where $L_0(s)$ is the CT loop transfer function seen by the input CT. Here, the quantizer gain (k_q) is assumed to be unity.

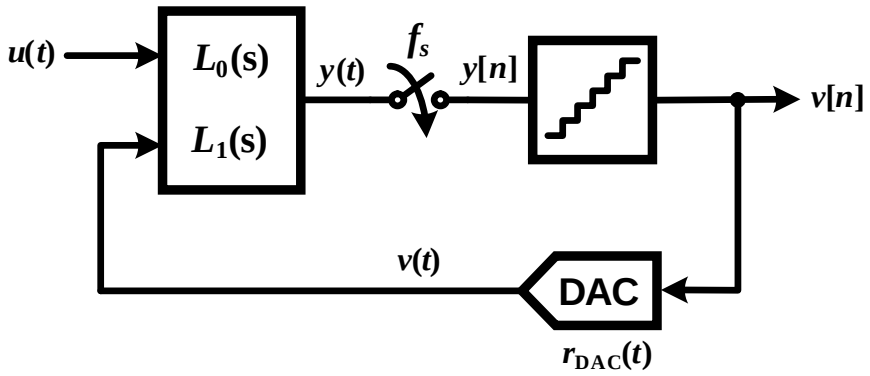

Figure 1: Block diagram of the CT DSM.

2. Recall that the STF for the corresponding discrete-time DSM was given as

$$STF_D(e^{j\omega}) = \frac{L_0(e^{j\omega})}{1 - L_1(e^{j\omega})} \tag{2}$$

Now, in order to find an expression for the implicit anti-alias filtering (AAF) of the CT-DSM, we define the frequency response of the AAF as

$$F_{AAF}(j\omega) = \frac{STF_C(j\omega)|_{CT}}{STF_D(e^{j\omega})|_{DT}} \tag{3}$$

(a) Show that the implicit AAF response can be simplified as

$$F_{AAF}(j\omega) = \frac{L_0(j\omega)|_{CT}}{L_0(e^{j\omega})|_{DT}} \tag{4}$$

(b) For a **CIFB,** third-order, CT DSM defined by the loop-filter coefficients $\{k_1, k_2, k_3\}$, show that the AAF filter is of the form

$$|F_{AAF}(j\omega)| \approx sinc^3\left(\frac{f}{f_s}\right) \tag{5}$$

(c) What can you conclude about the AAF, if the above CT DSM is implemented using a **CIFF** topology?

3. **Extra Credits:** From the class notes, the effect of the clock jitter is categorized as (i) the sampling jitter, and (ii) the feedback DAC reconstruction error.

(a) Write an expression for the error in the output, $e_{vj_s}[n]$, introduced due to the sampling jitter. Show that this error is shaped by the NTF of the modulator, exactly the same way as the quantization noise.

(b) Show that the error in the modulator output, $e_{vj_d}[n]$, due to the **NRZ** DAC reconstruction jitter is of the form:

$$\begin{aligned} e_{vj_d}[n] &\approx g[n] \otimes [(v[n] - v[n-1]) \cdot \Delta t[n]] \\ &= g[n] \otimes [\delta v[n] \cdot \Delta t[n]] \end{aligned} \tag{6}$$

where $g_1[n] \leftrightarrow STF_1(e^{j\omega})$ is the impulse response of the signal transfer function seen by the DAC feedback, and $\Delta t[n]$ is the normalized jitter process.

(c) Show that the in-band jitter noise, when using an NRZ DAC, can be given by the expression

$$J \approx \frac{\sigma^2_{\Delta T_s}}{T_s^2} \cdot \frac{\sigma^2_{LSB}}{\pi OSR} \int_0^{\pi} \left| \left(1 - e^{-j\omega}\right) \cdot STF_1(e^{j\omega}) \cdot NTF(e^{j\omega}) \cdot d\omega \right| \tag{7}$$

where the notations are same as in the class notes.