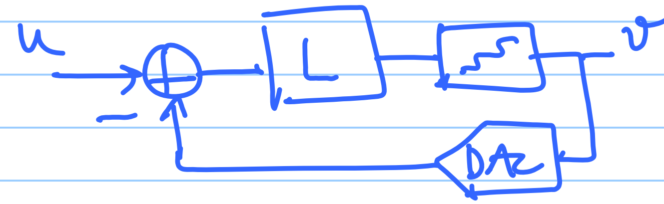
ECE 615 - Lecture 21

Note Title 3/29/2016

Multistage Modulators:

So far → Single-loop ΔΣ modulator



* OSR ↑ → SQNR ↑ (ENOB ↑)

Eg. BW = 80 MHz (802.11ac)

Can't increase OSR much further : f_s = 640 MHz in 65-nm CMOS

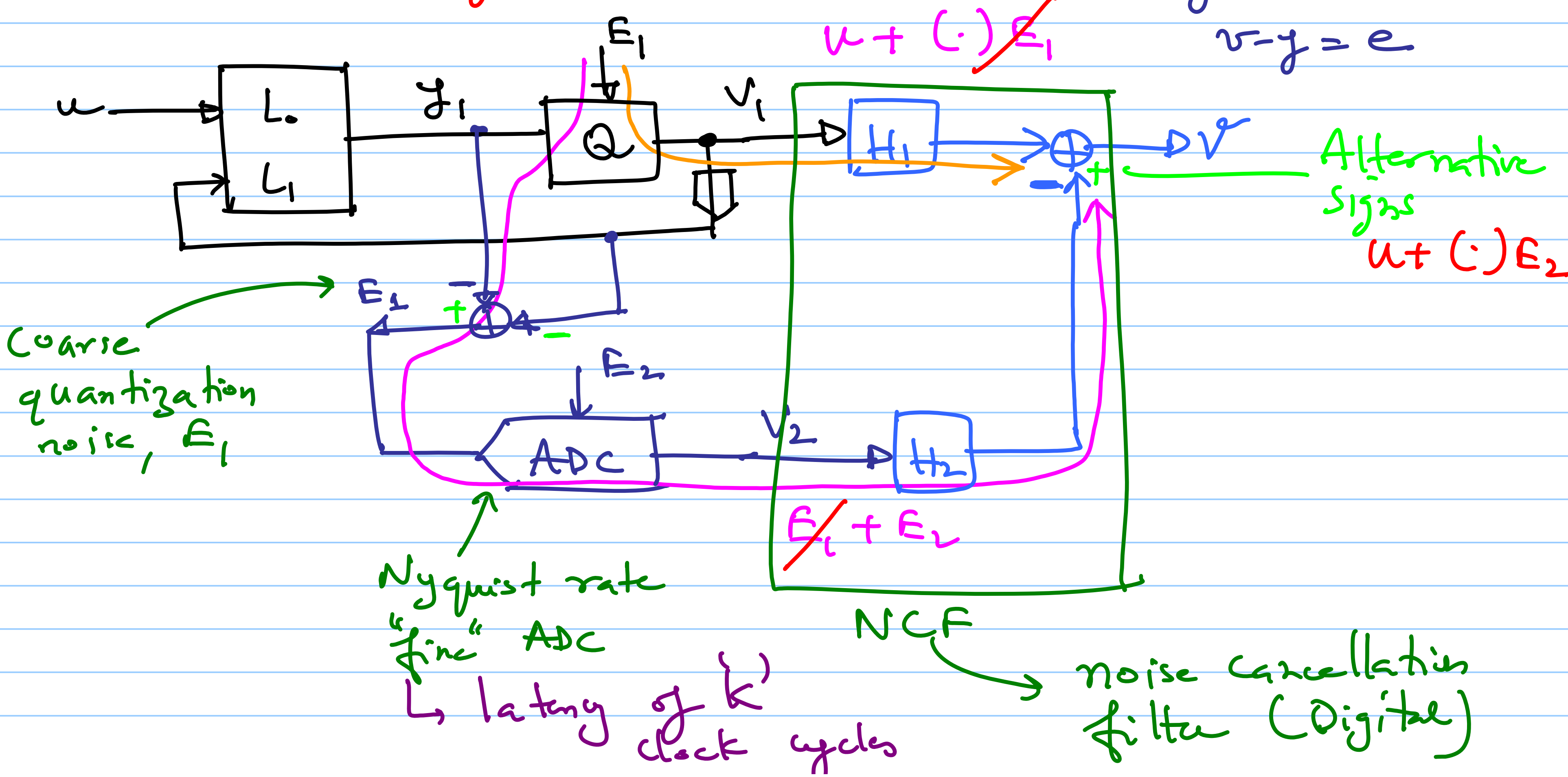
OSR = 4

what if order ↑ MSA ↓ due to stability issues.

L-0 Cascade of ΔΣ Modulator

$y - v = -e$

$v - y = e$



* L^{th}-order $\Delta\Sigma M$ in the 1^{st} stage followed by (0^{th}-order) ADC as the 2^{nd} stage ⇒ Nyquist rate ADC
  e.g. pipelined or SAR ADC

↳ L-0 cascade

⇒ combine V_1 & V_2 to cancel out E_1

⇒ $H_1(z) = z^{-k}$ ⇒ matches the latency of the 2^{nd}-stage

⇒ $H_2(z)$ ⇒ ??

$$V(z) = H_1(z)\,V_1(z) - H_2(z)\,V_2(z)$$

$$= \underbrace{z^{-k}}_{H_1}\left(STF_1 \cdot U + NTF_1(z) \cdot E_1\right) - H_2(z) \cdot \overbrace{z^{-k}}^{\text{delay of } ADC_2}\left(E_1 + E_2\right)$$

$\because U_2 = E_1$

$$= z^{-k} STF_1 \cdot U + \underbrace{\left(z^{-k} NTF_1(z) - z^{-k} H_2(z)\right)}_{=0} E_1 - H_2(z) \cdot z^{-k} \cdot E_2$$

$$H_2(z) \triangleq NTF_1(z)$$

$$\Rightarrow \quad V(z) = \underbrace{z^{-k} \cdot STF_1(z)}\cdot U(z) - \underbrace{z^{-k} NTF_1(z)} \cdot E_2(z)$$

$$NTF(z) = NTF_1(z) \cdot z^{-k}$$

↳ PSD of $E_2(z)$ is much smaller than that of $E_1(z)$

↳ significant gain in SQNR (ideally)

for perfect "noise cancelation"

$$H_{2d}(z) = NTF_{1a}(z)$$

digital → H_{2d}

$NTF_{1a}(z)$ ← switched capacitor analog

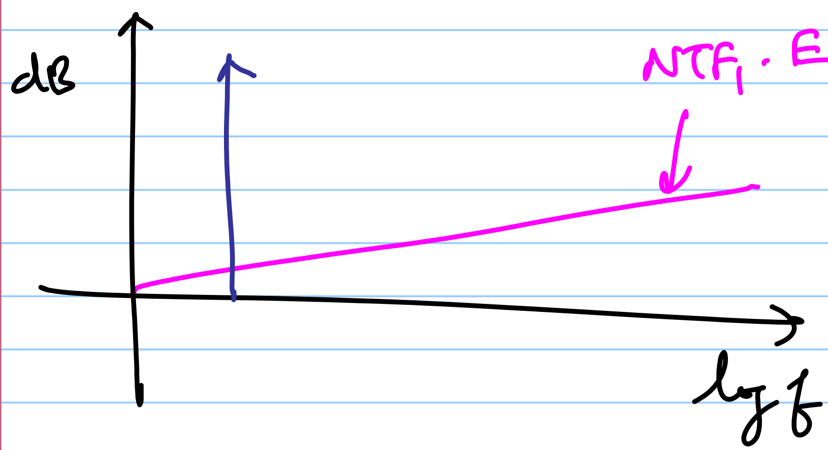
⇑ changes b'coz of opamp non-ideal-ities

end up with

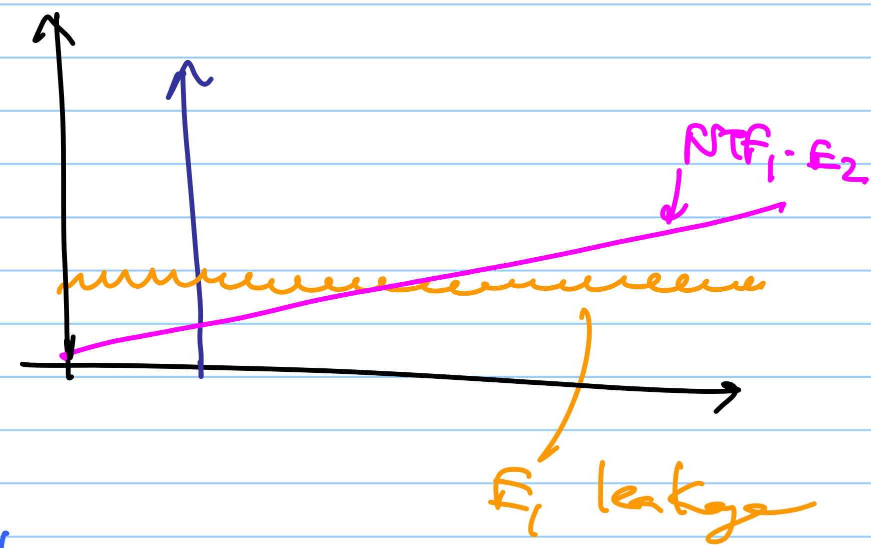
$$E_1 \left(NTF_{1a} - H_{2d} \right)$$

↳ coarse quantization noise leakage

Ideal



Realistic

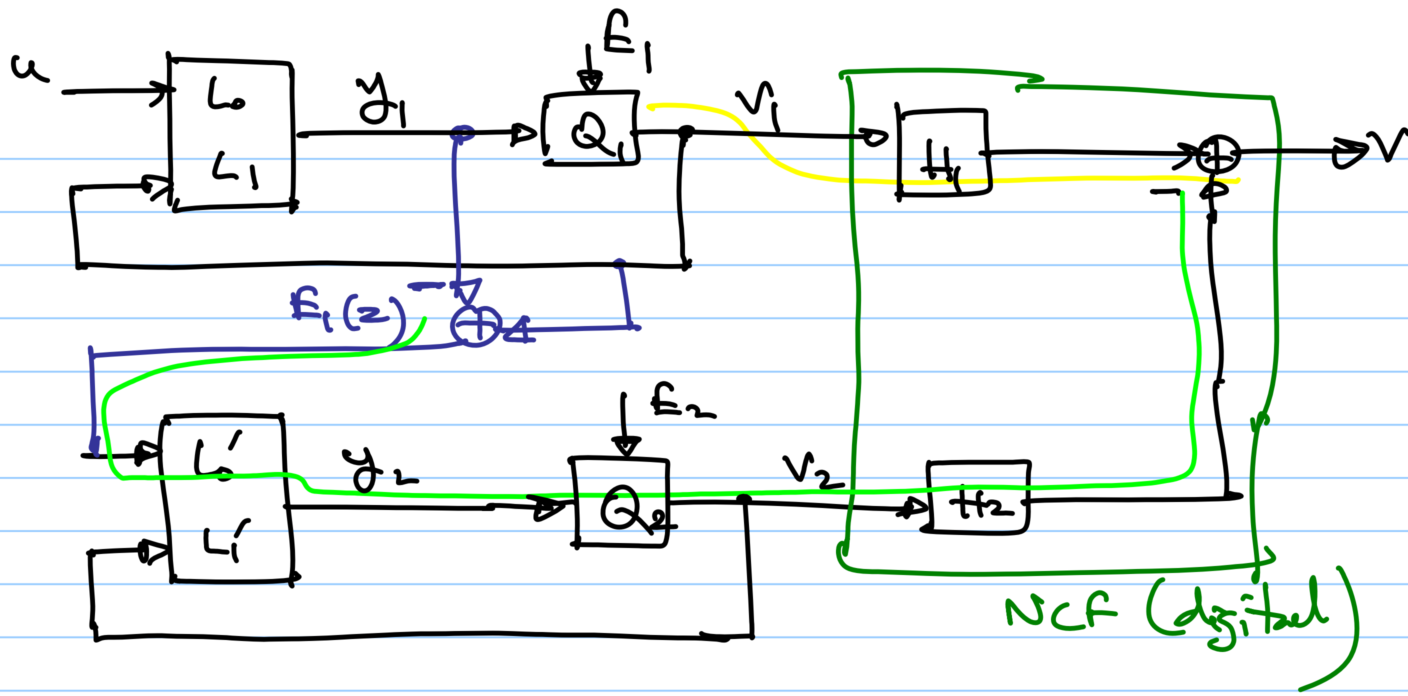


Eventually a trade-off between
power consumption & quantization noise leakage

Cascaded ΔΣ Modulator (MASH)

"MultistAge Noise SHaping" modulator = MASH

- second stage in the cascade is another ΔΣ Modulator



$$V(z) = H_1 V_1 - H_2 V_2$$

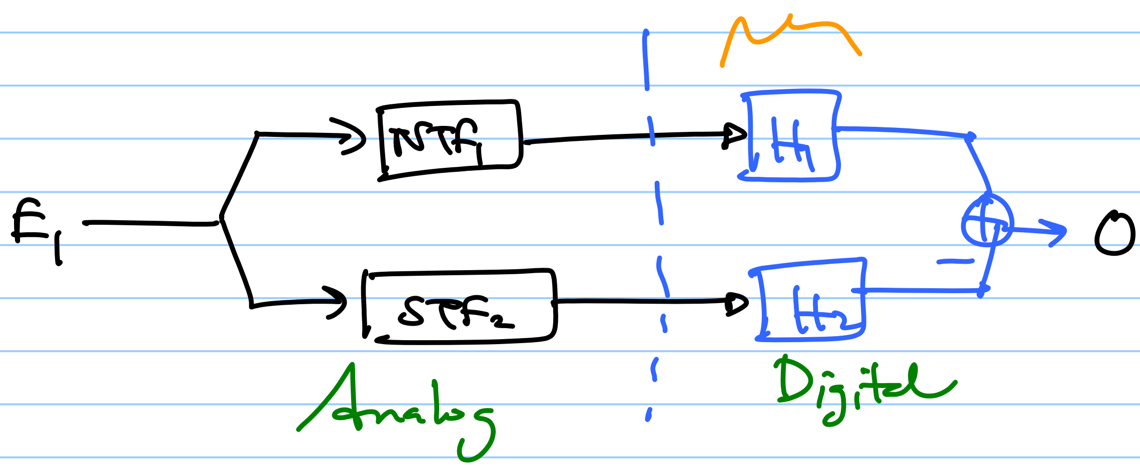
$$= H_1 \left(STF_1 \cdot u + NTF_1 \cdot E_1 \right) - H_2 \left(STF_2 \cdot E_1 + NTF_2 \cdot E_2 \right)$$

$$= \left(H_1 \cdot STF_1 \cdot U - H_2 \cdot NTF_2 \cdot E_2\right) + \left(H_1 \cdot NTF_1 - H_2 \cdot STF_2\right) \cdot E_1 \rightarrow 0$$

Cancel $E_1(z)$

for E_1 cancellation

$$H_1 \cdot NTF_1 \overset{\Delta}{=} H_2 \cdot STF_2$$



$$H_1 \overset{\Delta}{=} STF_2$$

$$H_2 \overset{\Delta}{=} NTF_1$$

$$NTF_{MASH} = NTF_1 \cdot NTF_2$$

2-1 → 3rd order noise shaping MASH

2-2 → 4

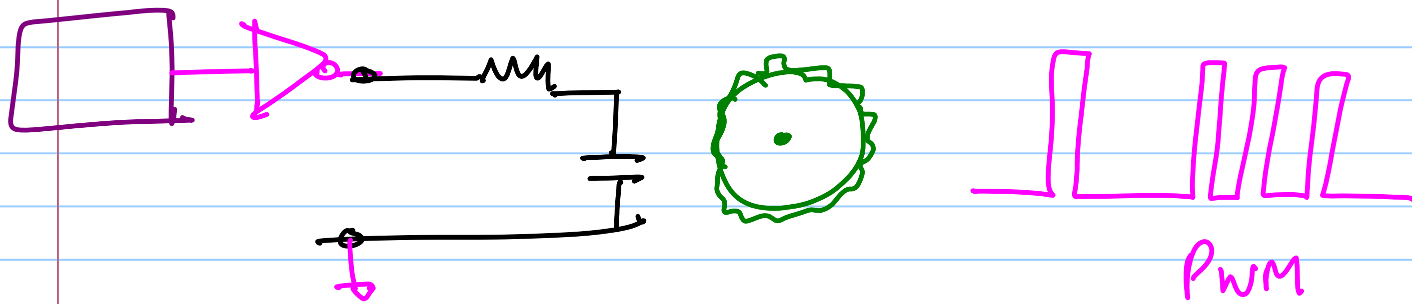
2-2-1 → 5

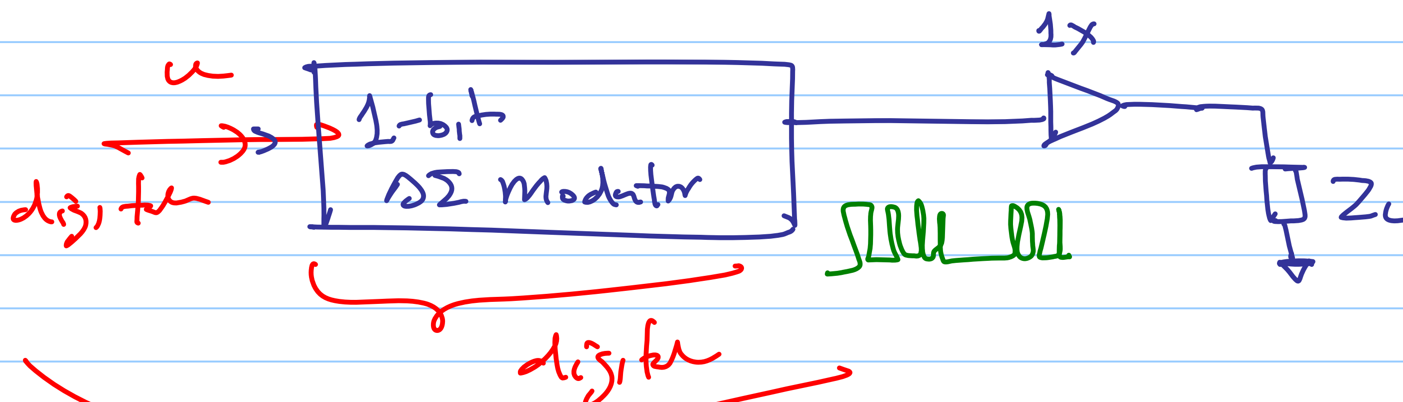
2-~~2~~-2 → diminishing returns

1-1 → first stage → avoid 1st order Modulator

1-bit ΔΣ modulator

6-bit resolution





FPGA

ΔΣ DAC