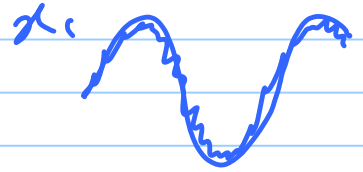
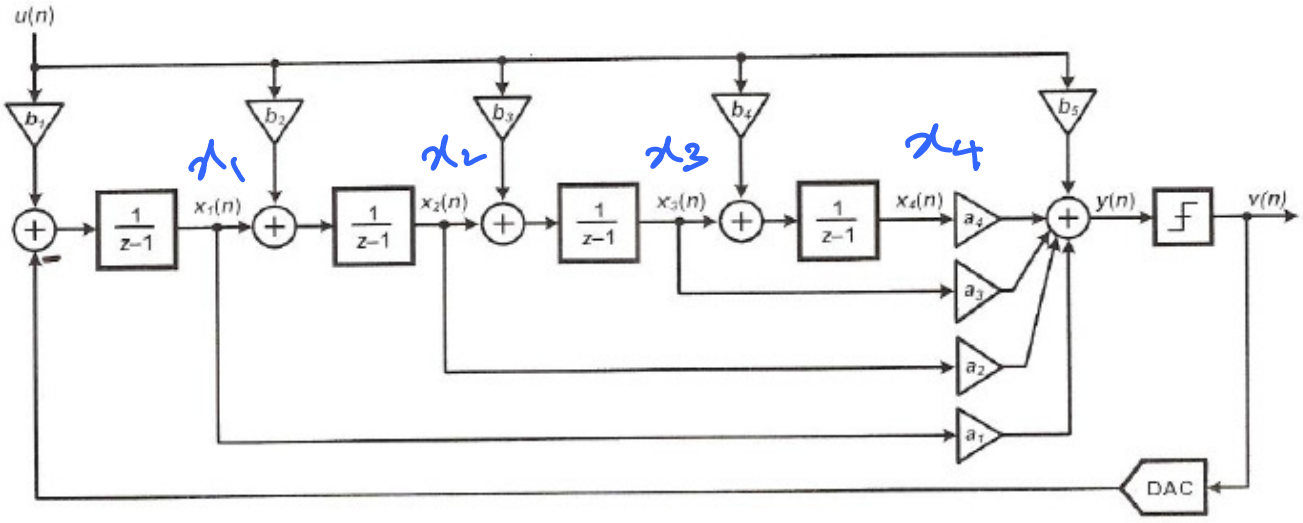
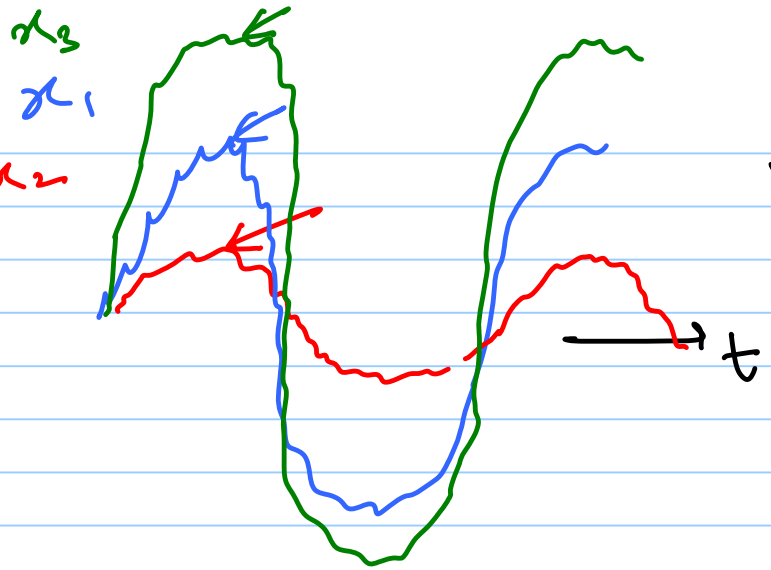
ECE 615 – Lecture 20

Note Title 3/17/2016

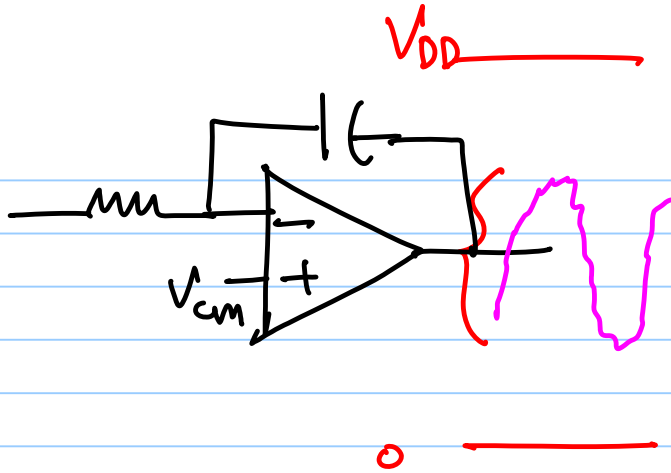
Dynamic Range Scaling







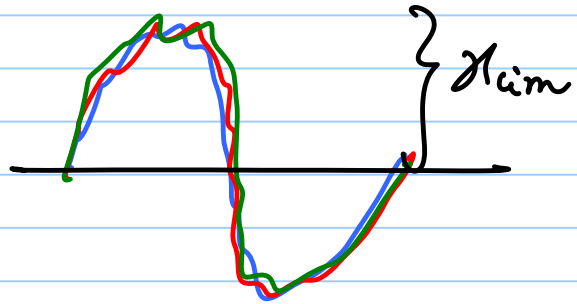
$$X = \begin{bmatrix} x_{1max} \\ x_{2max} \\ x_{3max} \end{bmatrix}$$



$$x_{lim} = \frac{1}{3} V_{DD}$$

$\Longrightarrow$ scale ABCD ( ) in the Toolbox

$\uparrow x_{max}$



$$x' = Sx$$

$$= \begin{bmatrix} \gamma_{r_1} & 0 & \\ 0 & \gamma_{r_2} & \\ & & \ddots \frac{1}{\gamma_N} \end{bmatrix} \begin{bmatrix} x_{1max} \\ x_{2max} \\ \vdots \\ x_{N,max} \end{bmatrix} \triangleq x_{lim} \begin{bmatrix} \vdots \\ \vdots \end{bmatrix}$$

$$\gamma_i = \frac{x_{max,i}}{x_{lim}}$$

DT ABCD matrix ⇒ state-space representation

$$x[n+1] = A\,x[n] + B\begin{bmatrix} u[n] \\ v[n] \end{bmatrix}$$

$$y[n] = C\,x[n] + D\begin{bmatrix} u[n] \\ v[n] \end{bmatrix}.$$

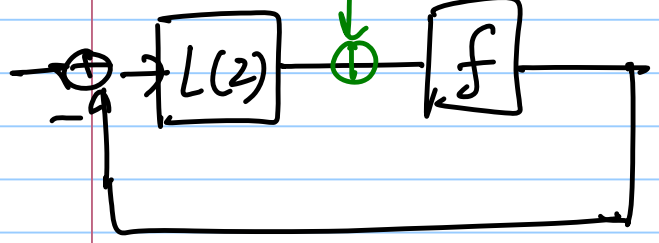
$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]$$

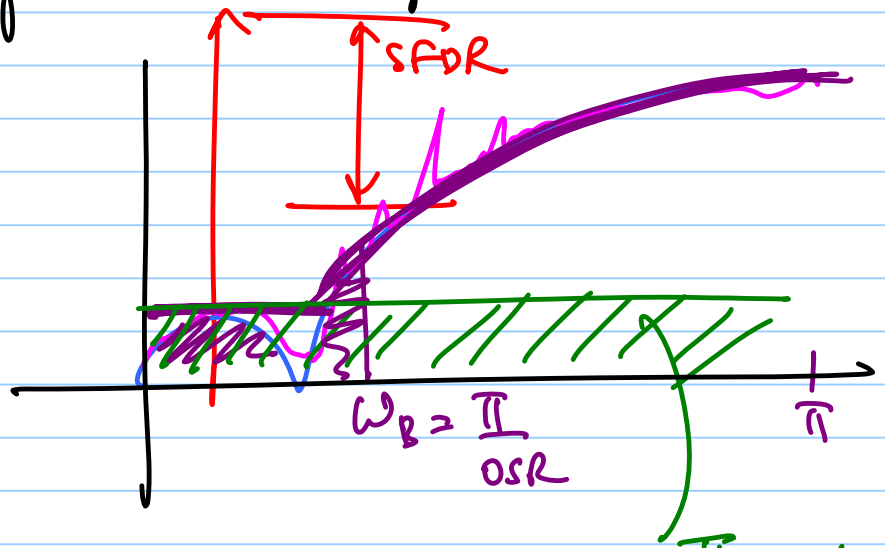
$$x_s = Sx$$

$$ABCD_s = \left[\begin{array}{c|c} SAS^{-1} & SB \\ \hline CS^{-1} & D \end{array}\right] \Rightarrow$$

new a, b, c, g's

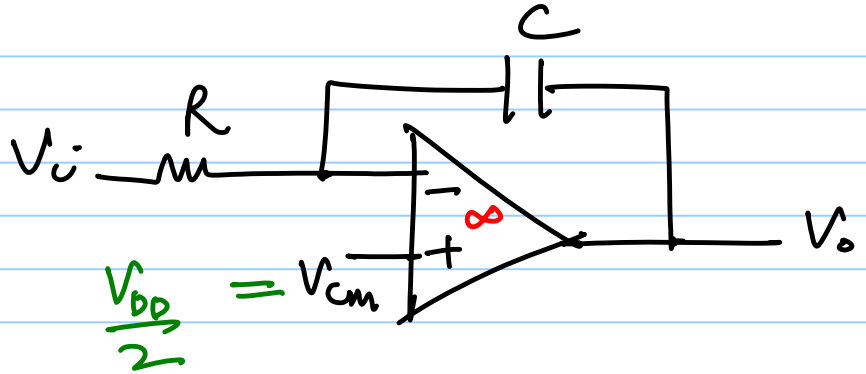
SQNR from system-level design





Overdesign the modulator for 8-10 dB extra SNR

→ Use thermal noise from the circuit for Dithering

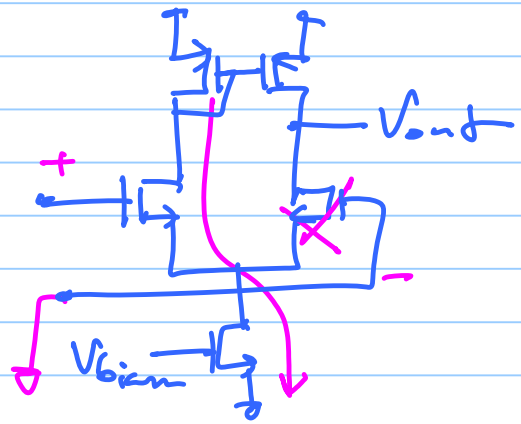


$$\frac{V_o}{V_i}(s) = \frac{1}{sRC}$$

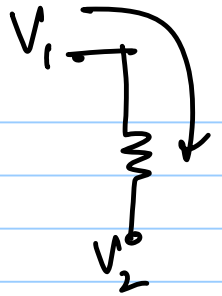
$R, C \pm 20\%$

$\frac{R_1}{R_2}$ $\frac{C_1}{C_2} \rightarrow < 0.1\%$

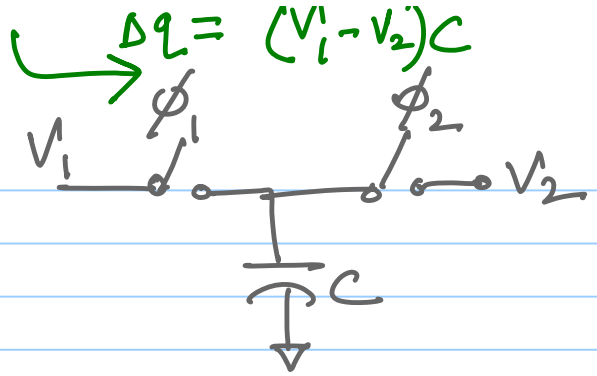
Cap ratios are tightly controlled on a chip



LM741 → ±15V

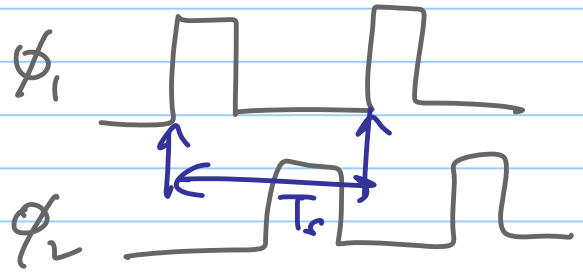


$$I = \frac{V_1 - V_2}{R}$$



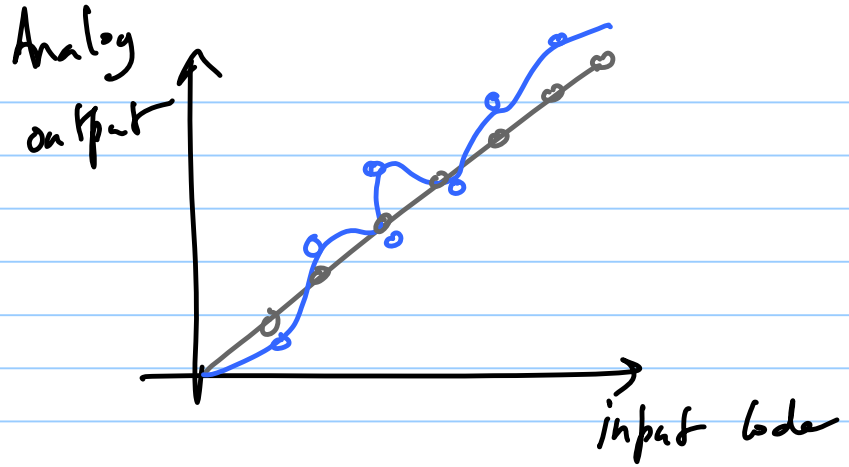
$$I = \frac{\Delta q}{T_s} = \frac{C}{T_s}(V_1 - V_2)$$

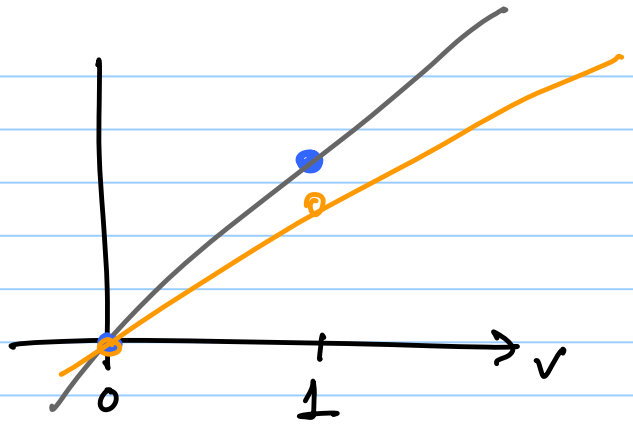
$$= f_s C (V_1 - V_2)$$



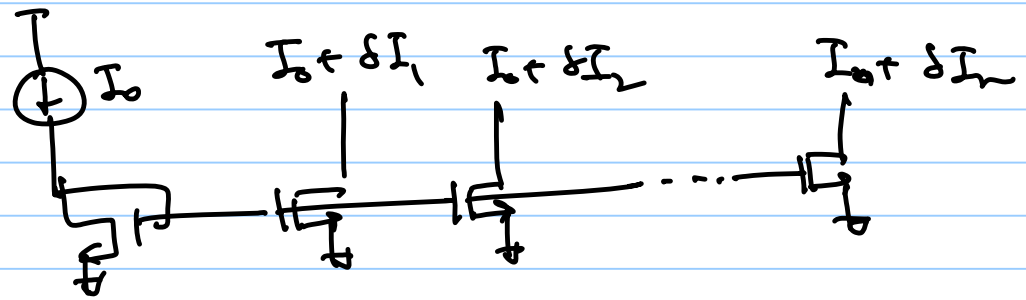
$$R = \frac{1}{f_s C}$$

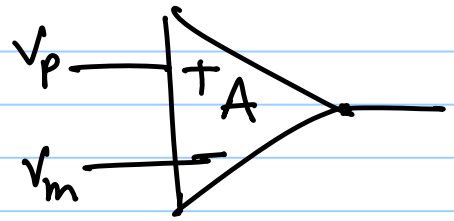
Switched-Cap Circuits
$\Rightarrow$ DT





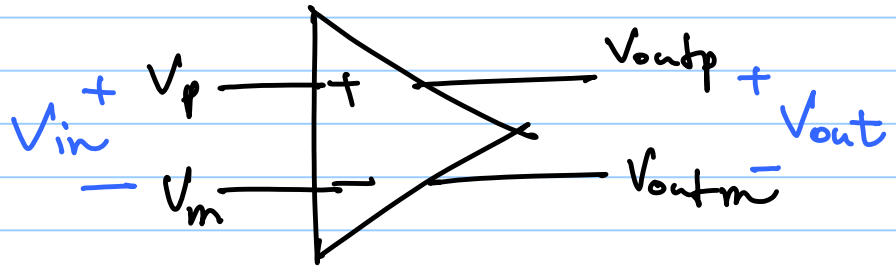
1-bit DAC is always "linear"





$V_{out} = A \cdot (V_p - V_m)$

single-ended



$(V_{outp} - V_{outm}) = A\,(V_p - V_m)$