

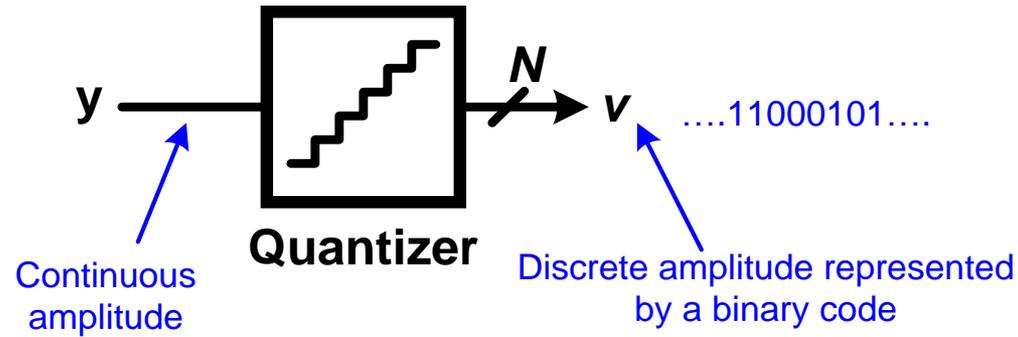
ECE615 Mixed-Signal IC Design

Lecture 4 Slides: Quantization

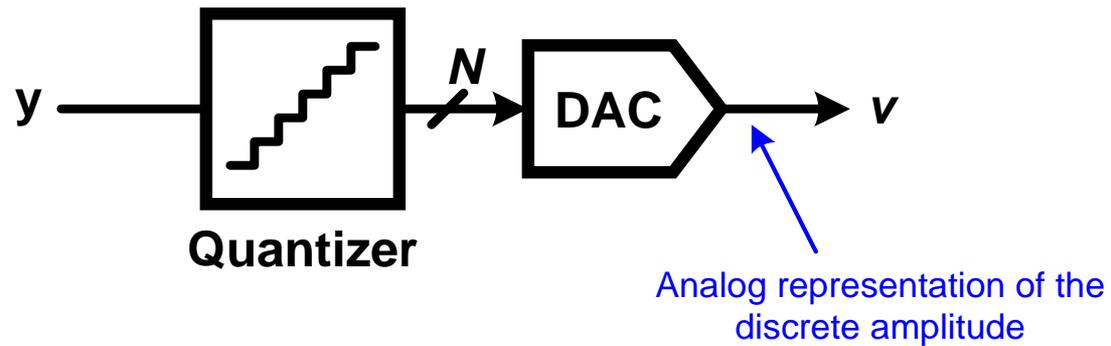
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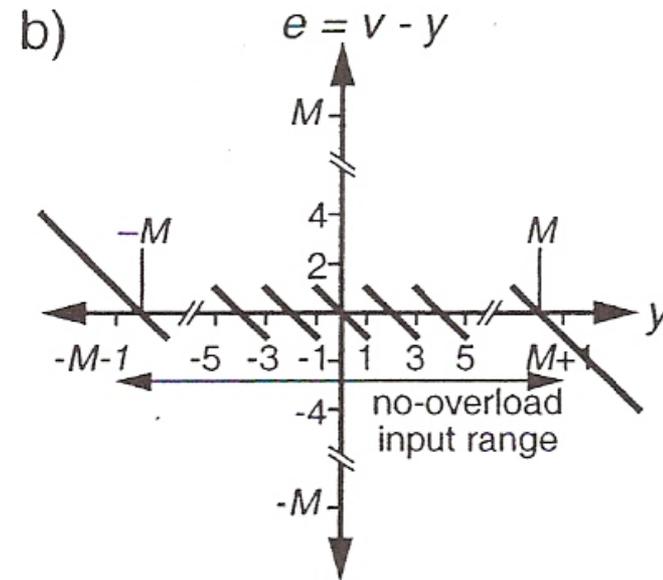
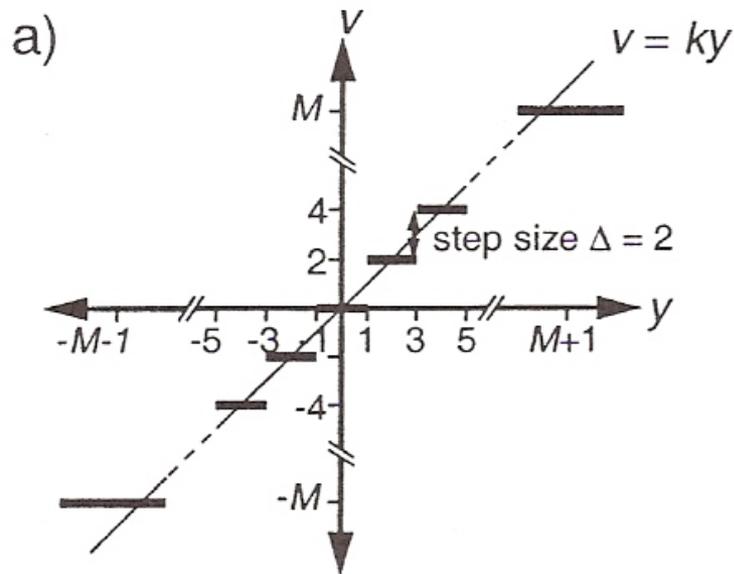
Quantizer



Modeling

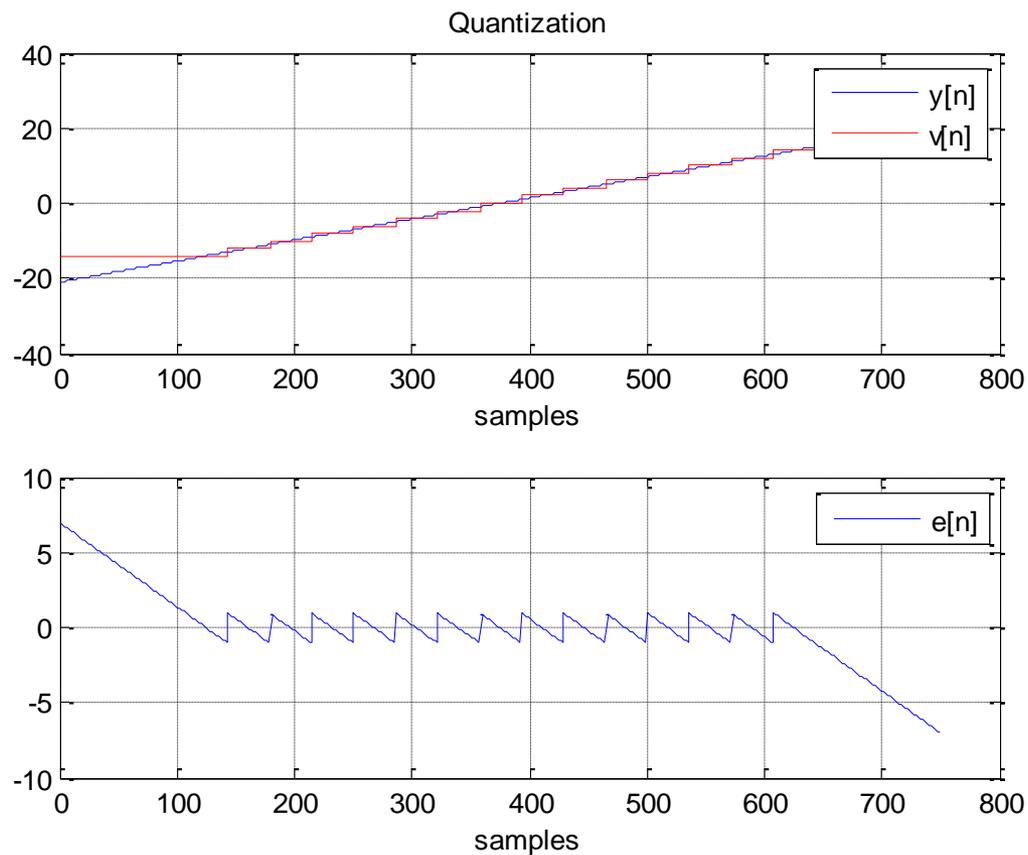


Mid-Tread Quantizer (odd number of levels)



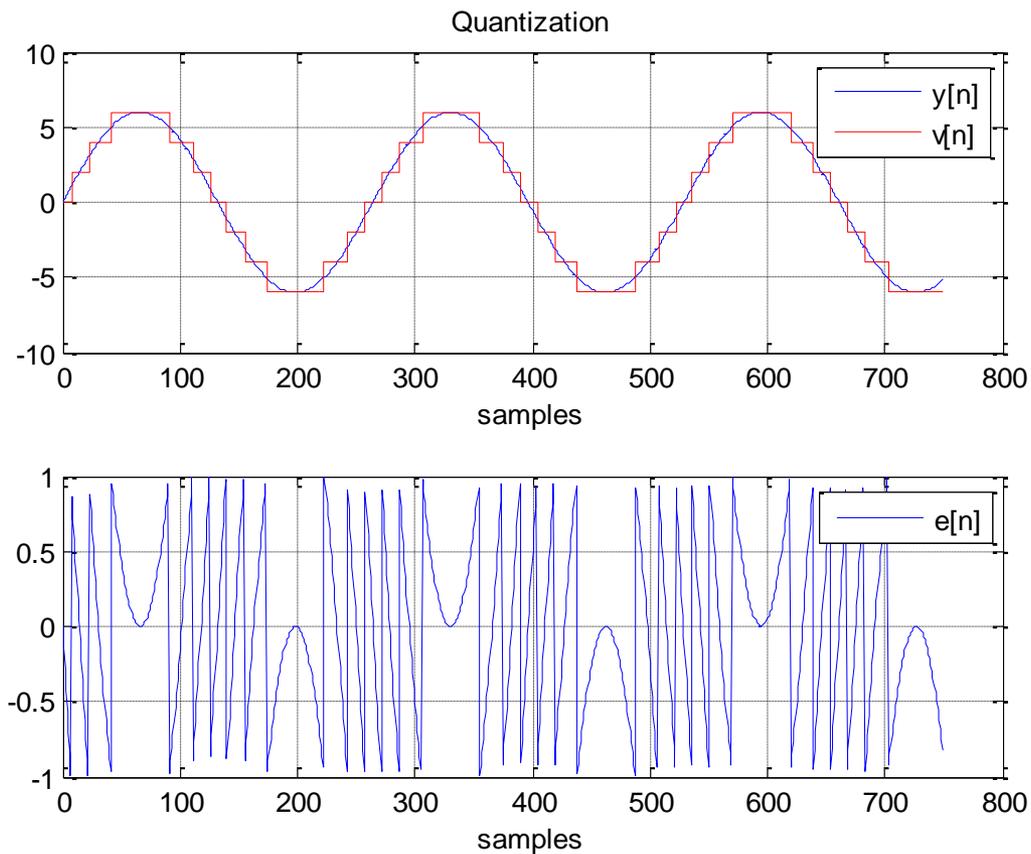
- ❑ Flat part of the step at $y=0$ (mid-tread).
- ❑ Here, $\text{LSB} = \Delta = 2$
- ❑ $M = \text{Number of steps}$, (M is even here)
 - ✓ Number of levels ($n\text{Lev}$) = $M+1$, (odd)
- ❑ Input thresholds: $0, \pm 2, \dots, \pm(M-1)$.
- ❑ Output levels: $0, \pm 2, \pm 4, \dots, \pm M$.

Quantizer characteristics : Slow ramp input



File: Quantizer_ramp_input.m

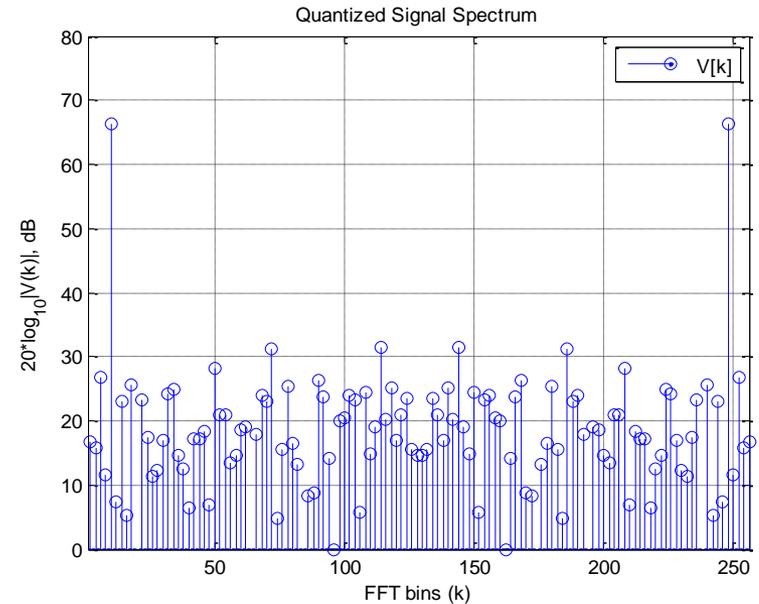
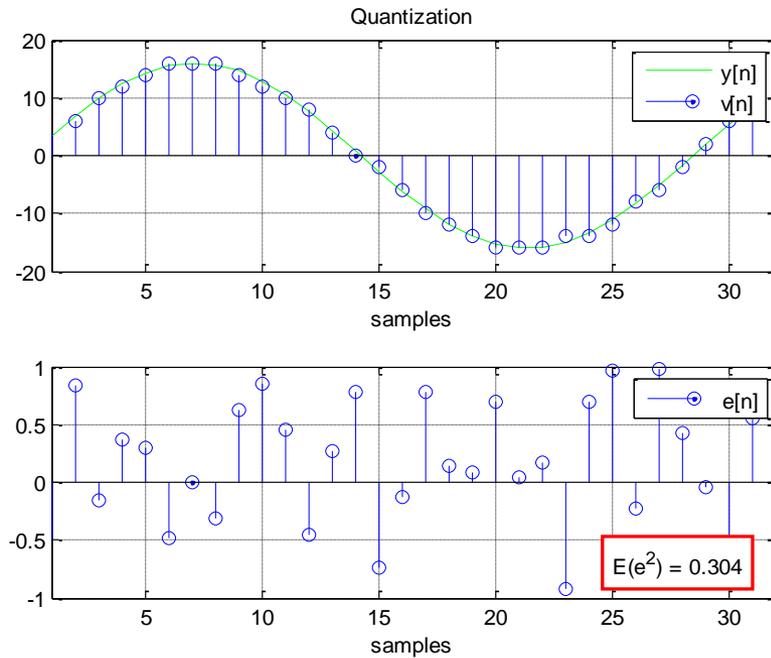
Quantizer characteristics : Sine input



File: Quantizer_sine_input.m

Quantization Noise Spectrum

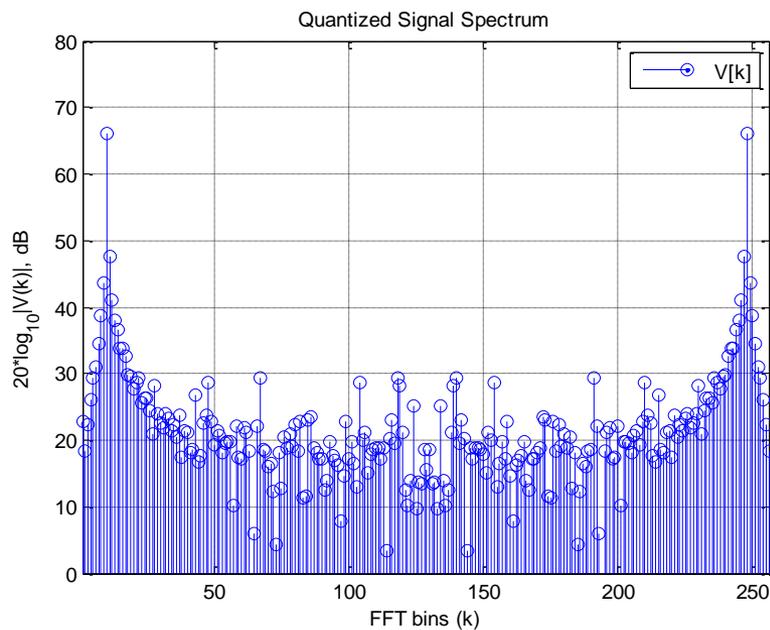
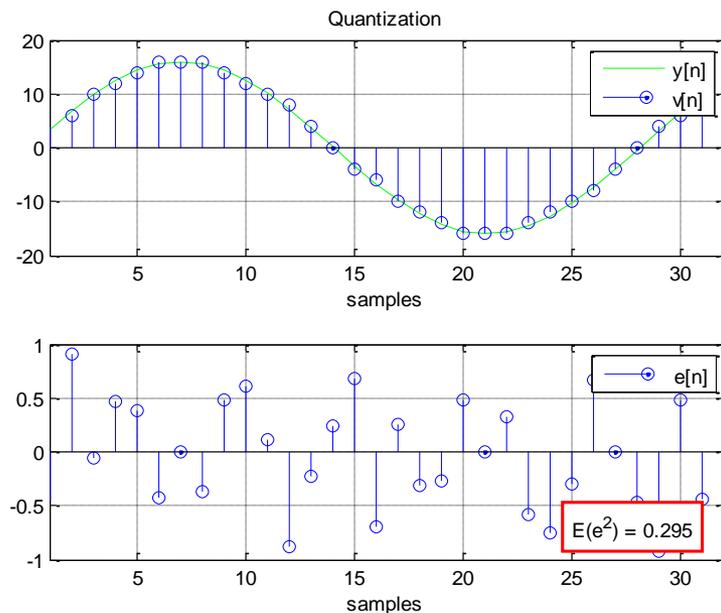
Quantization Noise : Example 1



$n\text{Lev}=17, \Delta=2, f_{\text{in}}/f_s = 9/256 :$
• $E(e^2) = 0.304 \approx \Delta^2/12$

file:Quantization_Noise1.m

Quantization Noise : Example 1 contd.



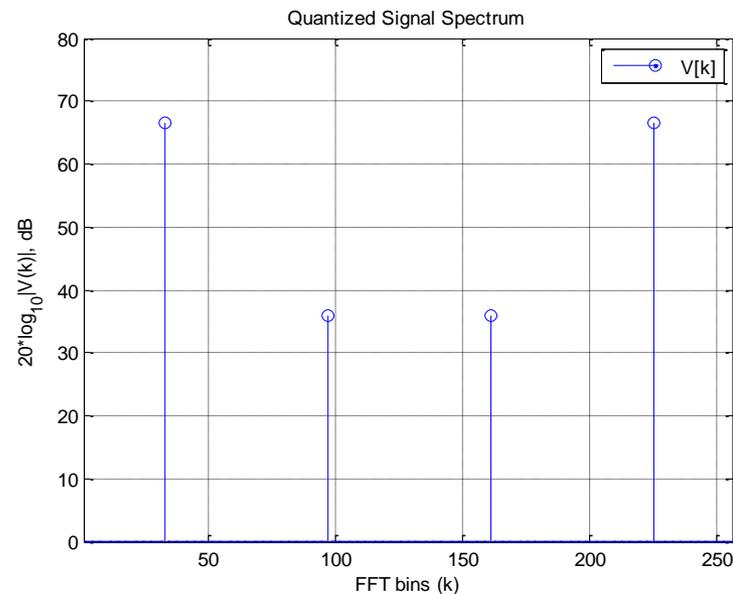
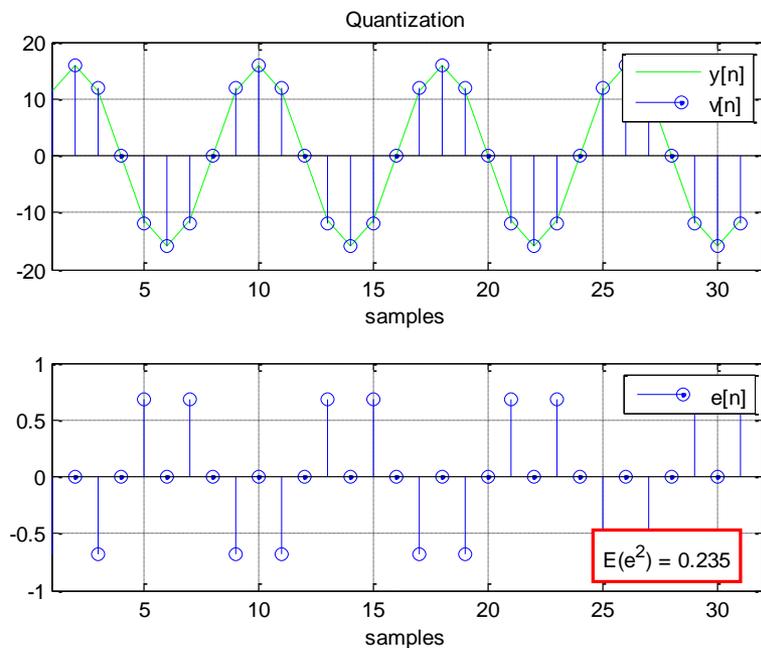
$nLev=17$, $\Delta=2$, $f_{in}/f_s = 9.1/256$:

• $E(e^2) = 0.295 \approx \Delta^2/12$

• Notice the FFT leakage.

file:Quantization_Noise1.m

Quantization Noise : Example 1 contd.



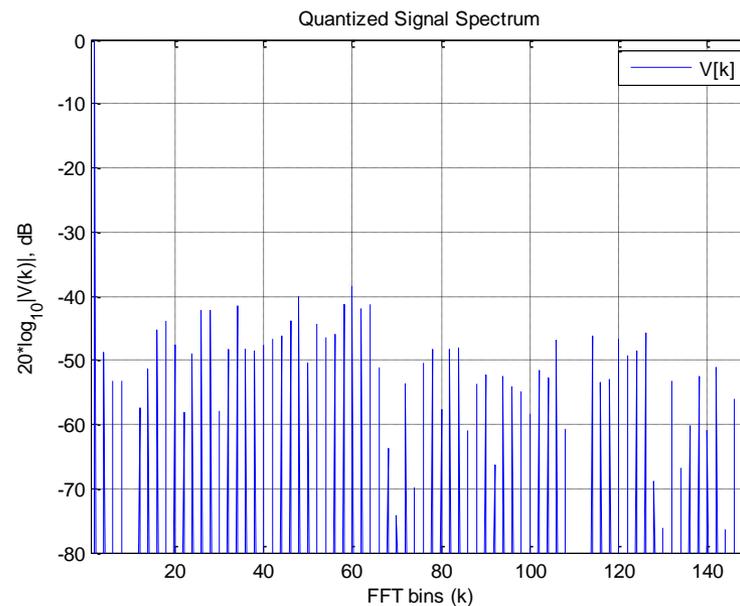
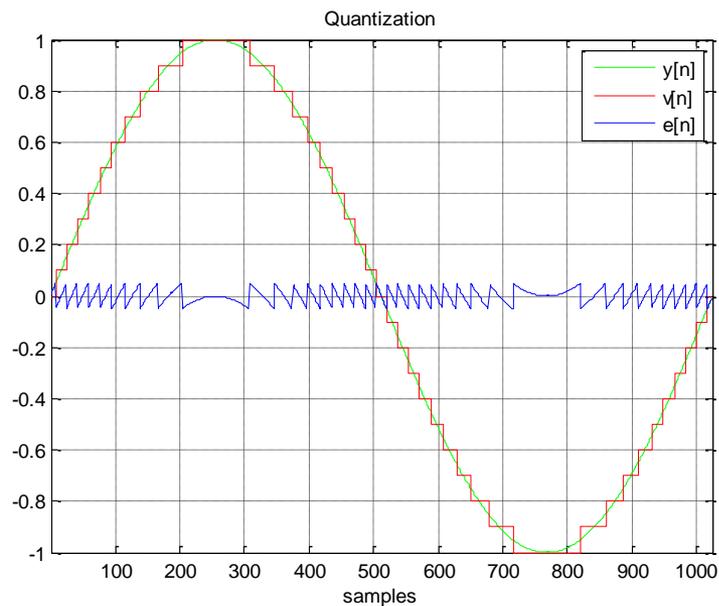
$nLev=17$, $\Delta=2$, $f_{in}/f_s = 32/256 = 1/8$:

• $E(e^2) = 0.235 < \Delta^2/12$

• Quantization *noise* approximation not valid

file:Quantization_Noise1.m

Quantization Noise : Example 2

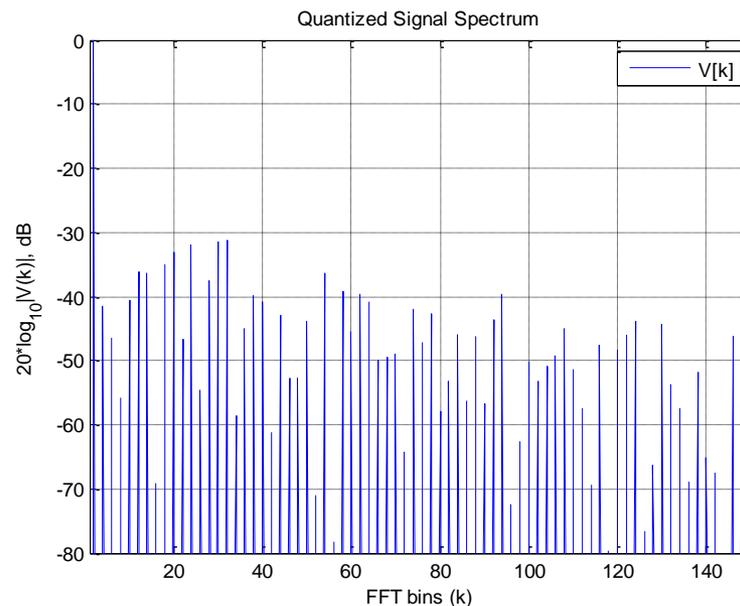
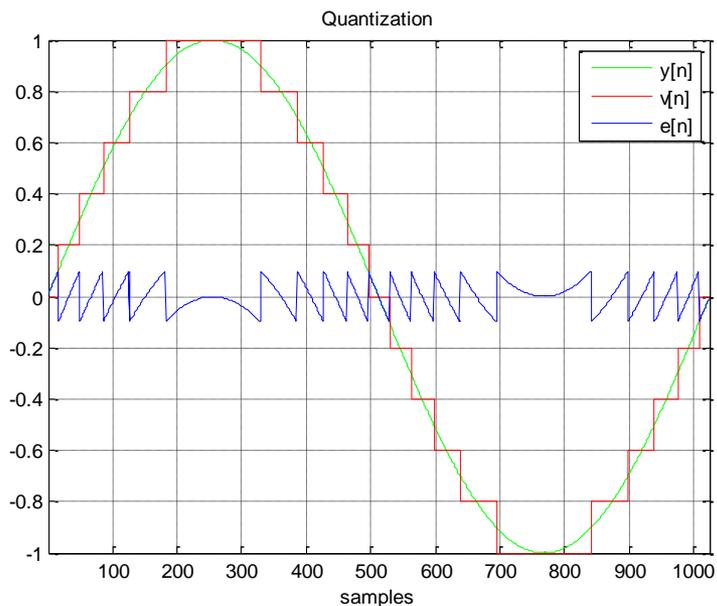


$A=1, \Delta=0.1, f_{in}/f_s = 1/1024 :$

- Most of the tones around the 44th bin
- Average quantization noise floor lowers by 6 dB
- SFDR = -39 dB (SFDR increases by 9 dB if LSB size is halved)

file:Quantization_Noise2a.m

Quantization Noise : Example 2 contd.

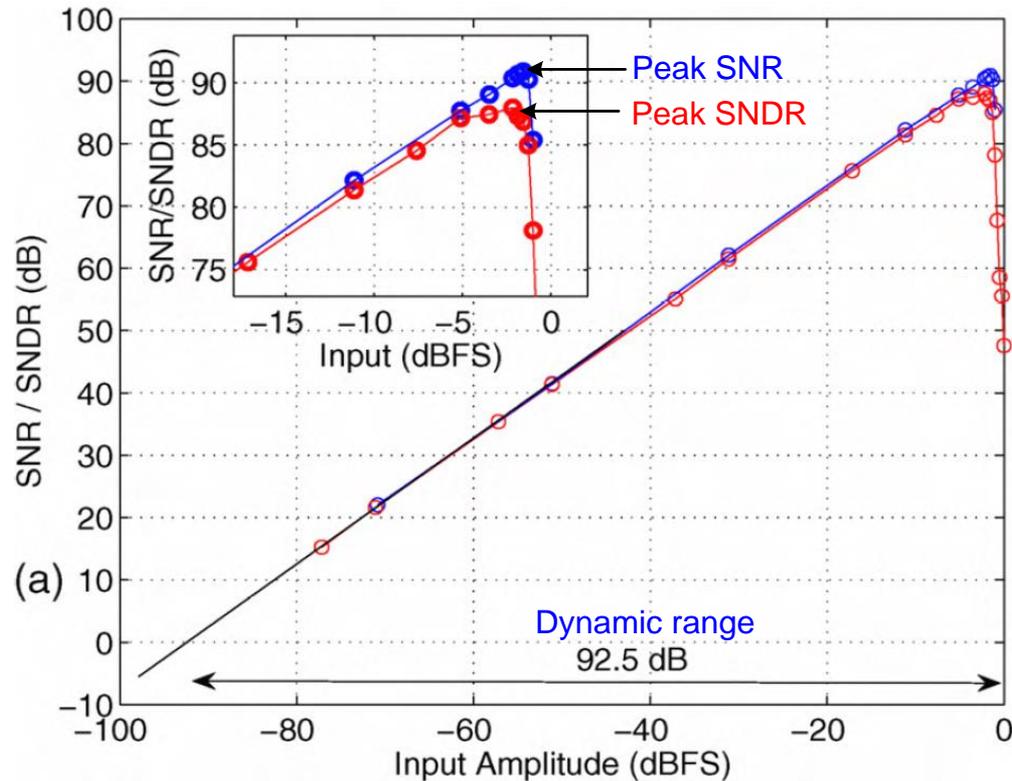


$A=1, \Delta=0.2, f_{in}/f_s = 1/1024 :$

- Most of the tones around the 20th bin
- SFDR = -30 dB
- Quantizer spectrum not white and the error (e) is correlated with the input (y).

file:Quantization_Noise2b.m

Frequency Domain Measurements

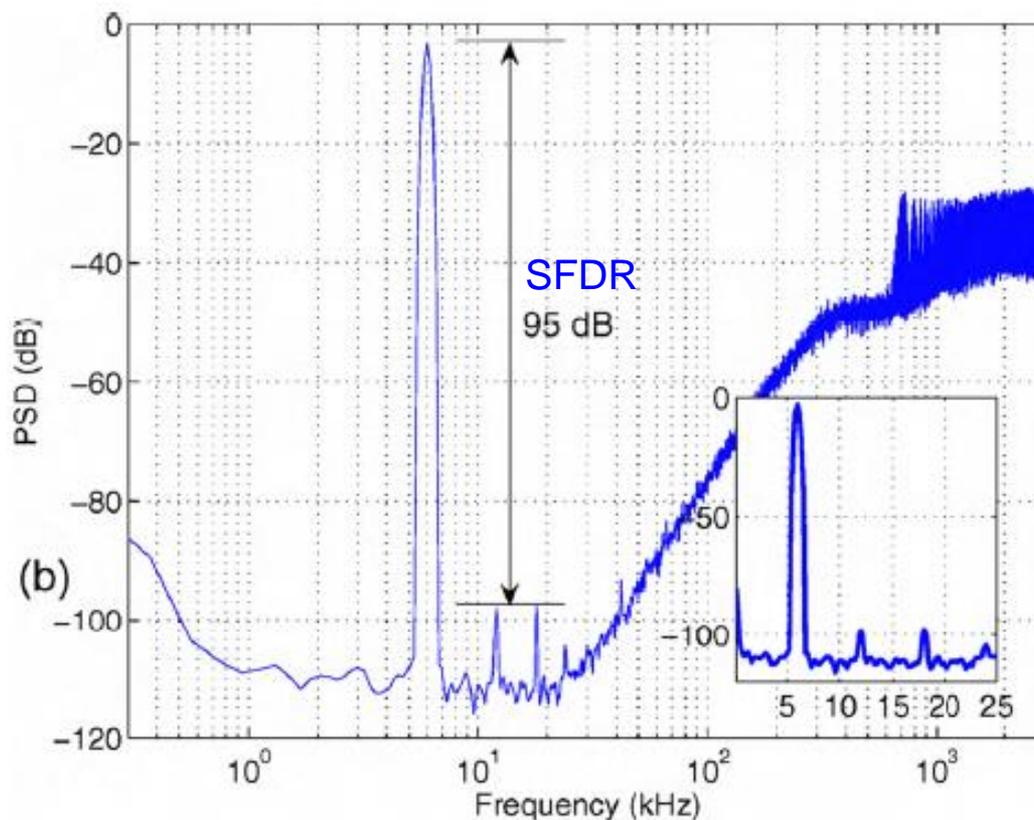


SUMMARY OF MEASURED ADC PERFORMANCE.

Signal Bandwidth/Clock Rate	24 kHz / 6.144 MHz
Quantizer Range	3.6 V _{pp,diff}
Input Swing for peak SNR	-1.6 dBFS
Dynamic Range/SNR/SNDR	92.5 dB/91 dB/88 dB
Active Area	0.24 mm ²
Process/Supply Voltage	0.18 μm CMOS/1.8 V
Power Dissipation (Modulator + References)	110 μW
Figure of Merit	0.0665 pJ/level

Reference [2]

Spurious (tone) Free Dynamic Range (SFDR)



Reference [2]

References

- [1] M. Gustavsson, J. Wikner, N. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, 2000.
- [2] S.Pavan and P.Sankar, “A 110 μ W Single Bit Audio Continuous-time Oversampled Converter with 92.5 dB Dynamic Range”, *Proceedings of the European Solid State Circuits Conference (ESSCIRC), Athens, Greece, September 2009*.
- [3] S. Pavan, N. Krishnapura, “EE658 VLSI Data Conversion Circuits Course,” 2008, [Online]: <http://www.ee.iitm.ac.in/~nagendra/videolectures/doku.php?id=start>