ECE615 Mixed-Signal IC Design

Lecture 20: Discrete-Time ΔΣ Modulator Implementation

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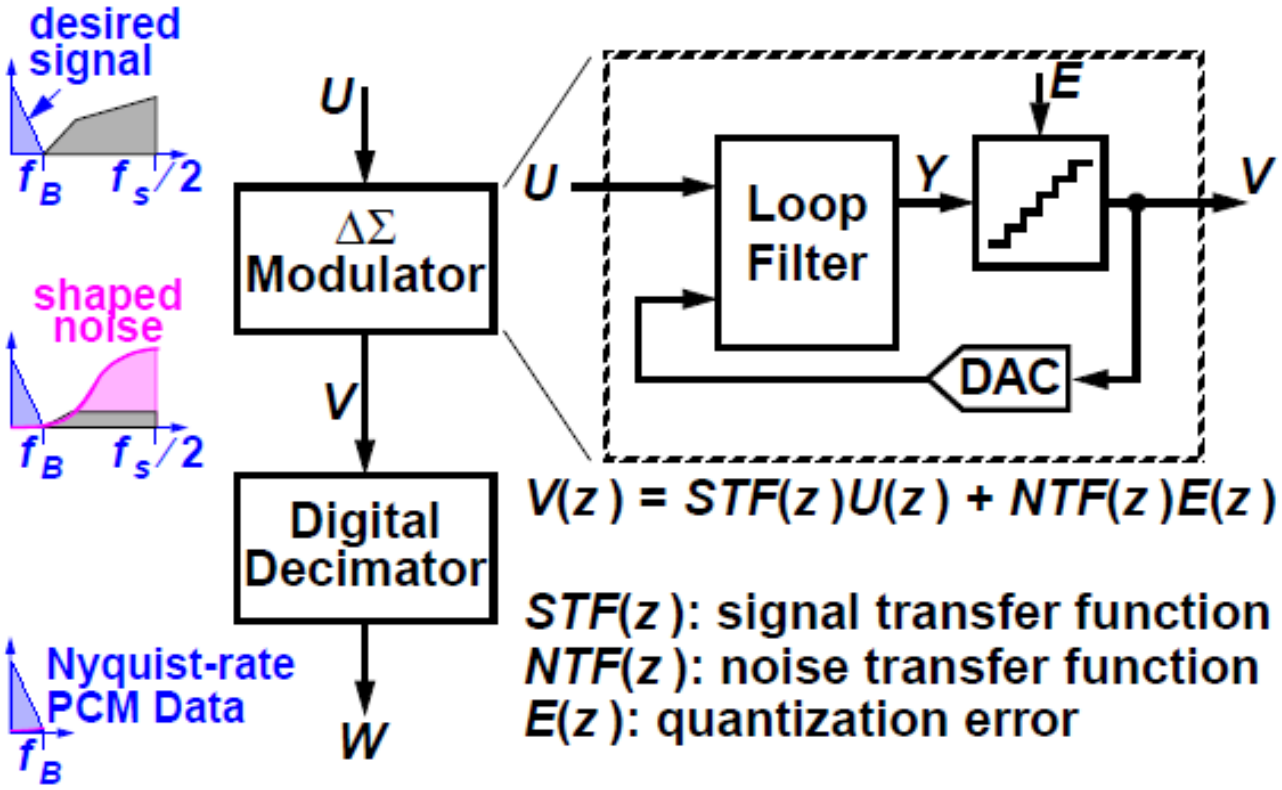
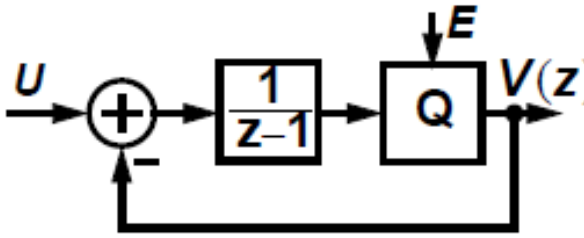
Review: A ΔΣ ADC System



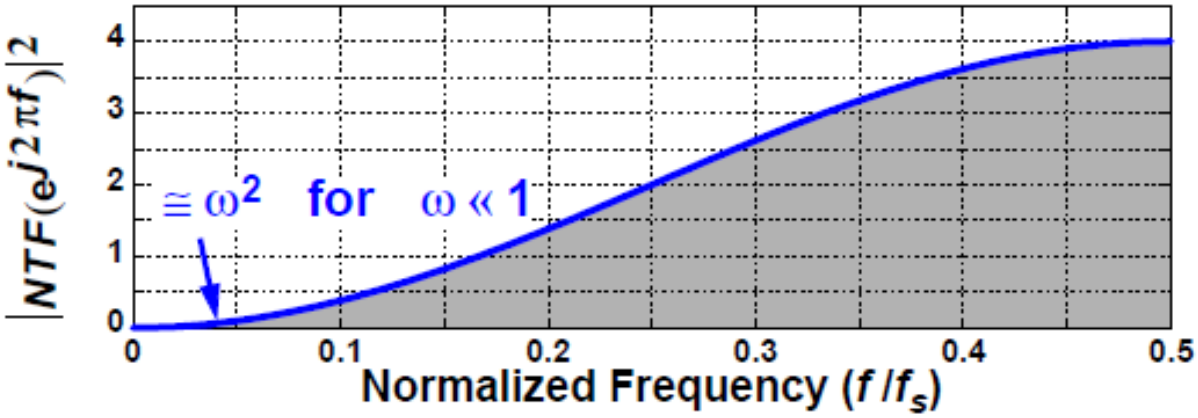
Review: MOD1



$$V(z) = NTF(z)E(z) + STF(z)U(z)$$

$$NTF(z) = (1 - z^{-1})$$

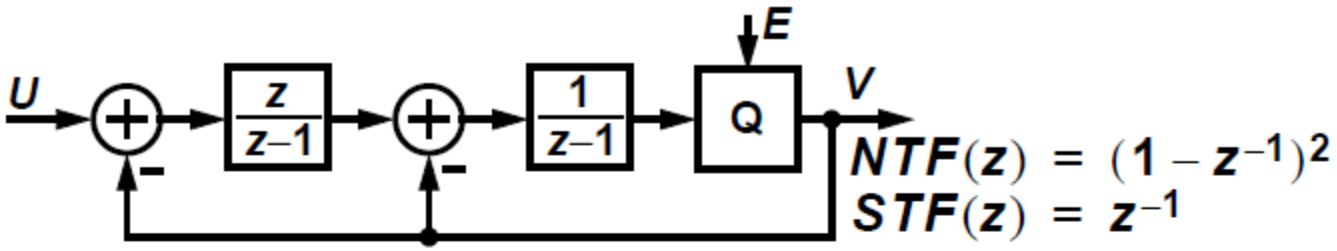
$$STF(z) = z^{-1}$$

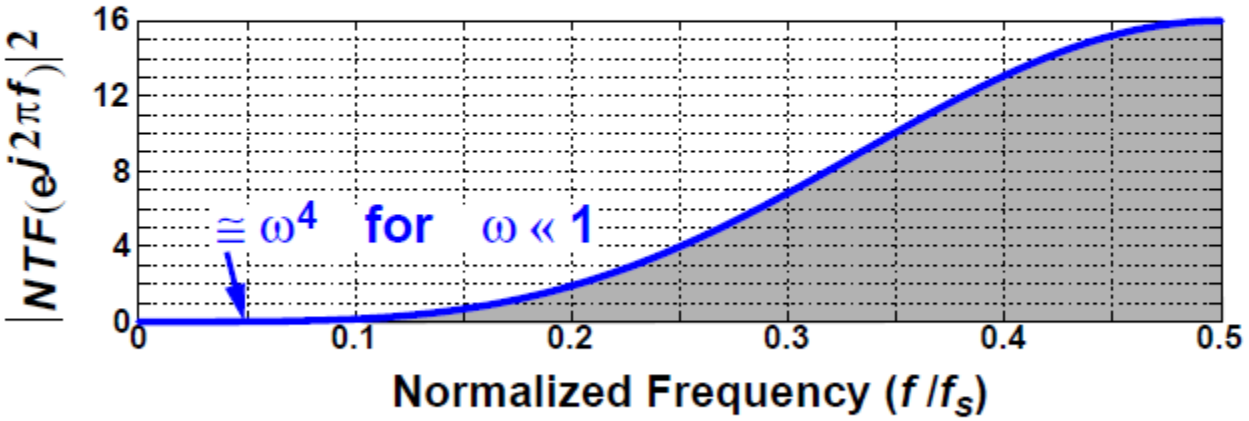


- **Doubling OSR improves SQNR by 9 dB**

  Peak SQNR $\approx$ dbp$(9 \cdot OSR^3/(2\pi^2))$; dbp$(x) \equiv 10\log_{10}(x)$

Review: MOD2

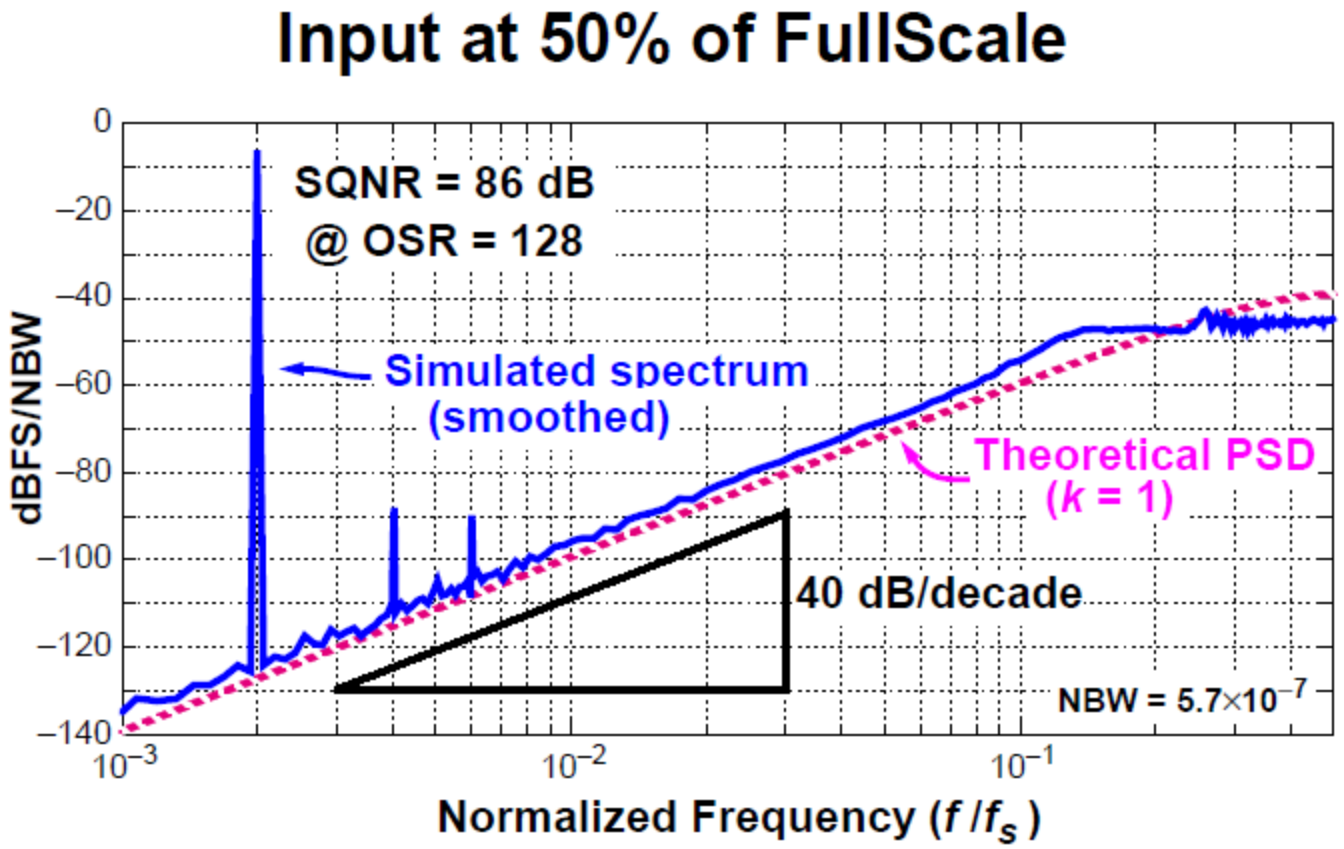




- **Doubling OSR improves SQNR by 15 dB**

  Peak SQNR $\approx$ dbp$((15 \cdot OSR^5)/(4\pi^4))$

Review: Simulated MOD2 PSD



Example Design 1

• Clock at *fs = 1 MHz.*

Assume BW = 1 kHz.

$\Rightarrow OSR = fs/(2 \cdot BW) = 500 \approx 2^9$

• MOD1: SQNR ≈ 9 dB/octave • 9 octaves = 81 dB

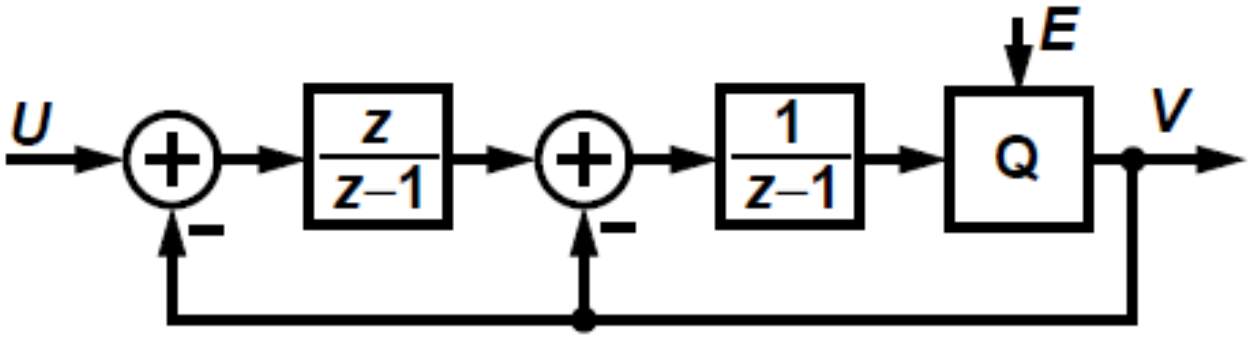
• MOD2: SQNR ≈ 15 dB/octave • 9 octaves =135 dB

Actually more like 120 dB.

• SQNR of MOD1 is not bad, but SQNR of MOD2 is awesome!

MOD2 is usually preferred over MOD1 because MOD2's quantization noise is more well-behaved.

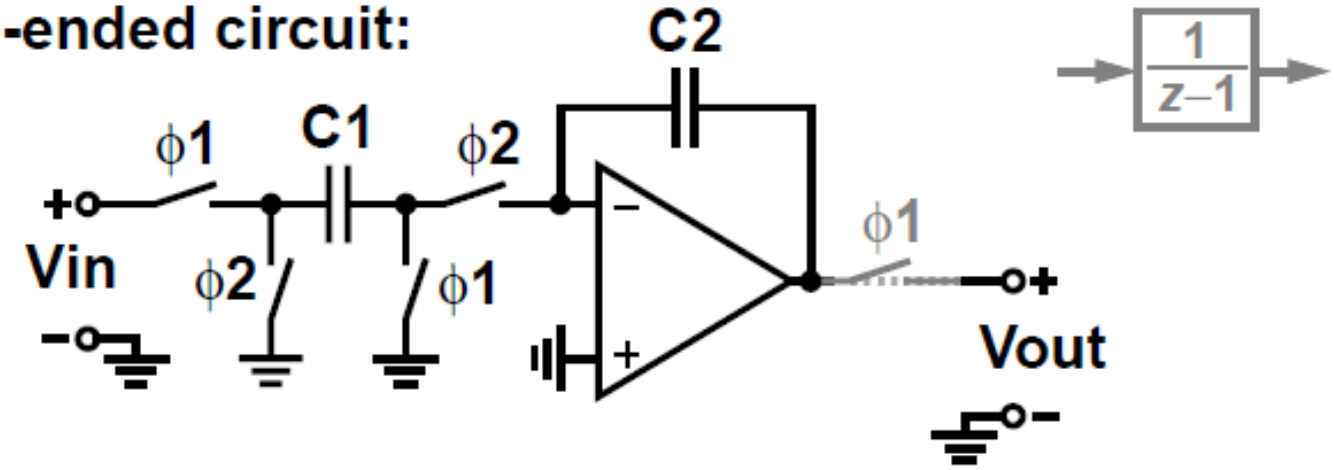
Block Diagram



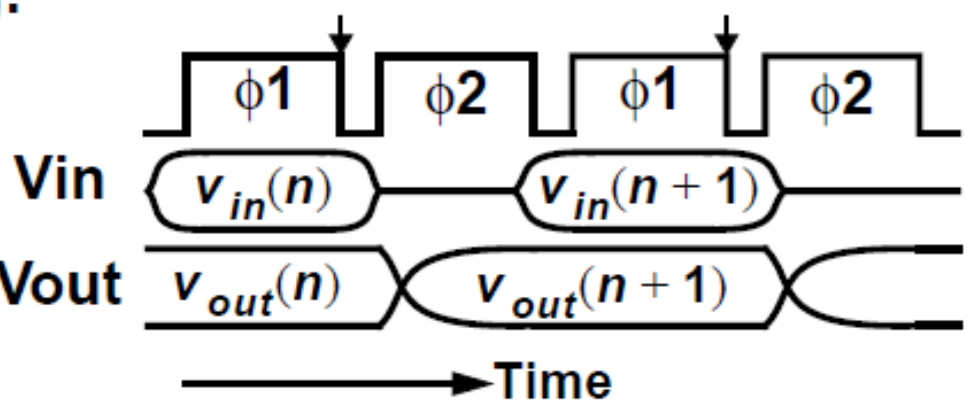
- Summation blocks
- Delaying and non-delaying discrete-time
- integrators
- Quantizer (1-bit)
- Feedback DACs (1-bit)
- Decimation filter (not shown)
  - Digital and therefore “easy”

Switched-Capacitor Integrator

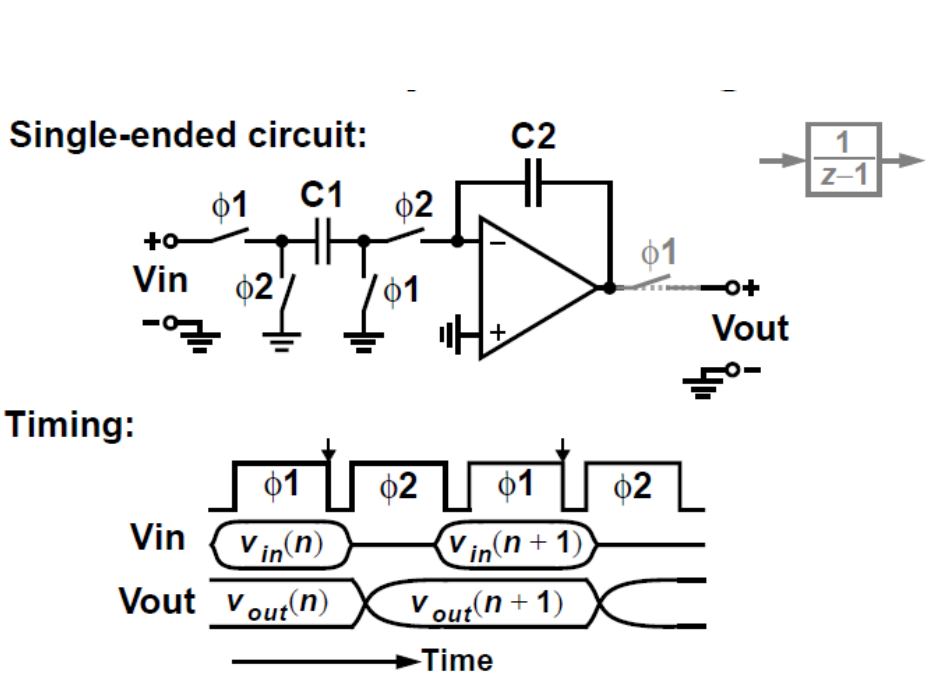
Single-ended circuit:

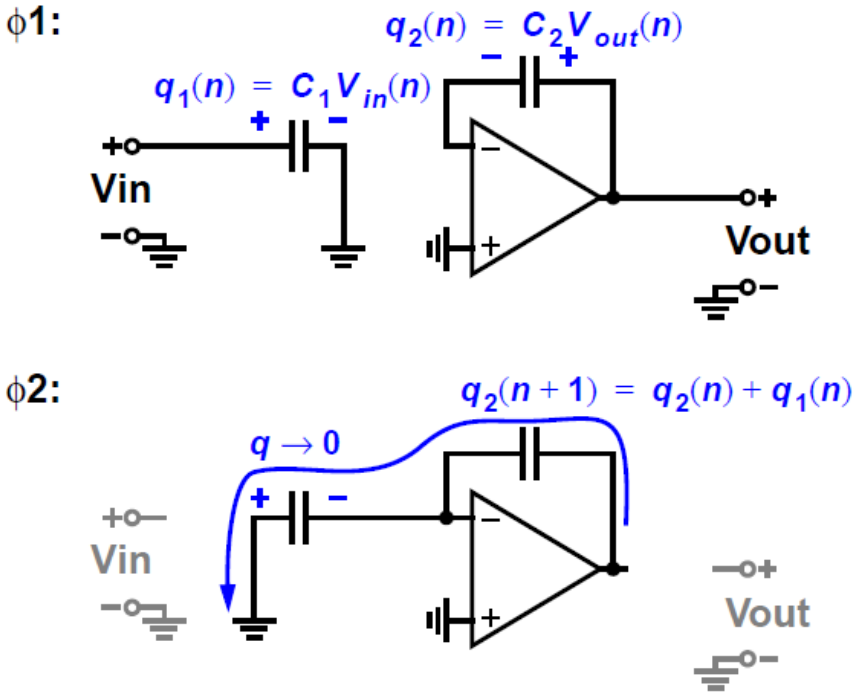


Timing:



Switched-Capacitor Integrator contd.





Switched-Capacitor Integrator contd.

$$q_2(n+1) = q_2(n) + q_1(n)$$

$$z\,Q_2(z) = Q_2(z) + Q_1(z)$$

$$Q_2(z) = \frac{Q_1(z)}{z-1}$$

- This circuit integrates charge

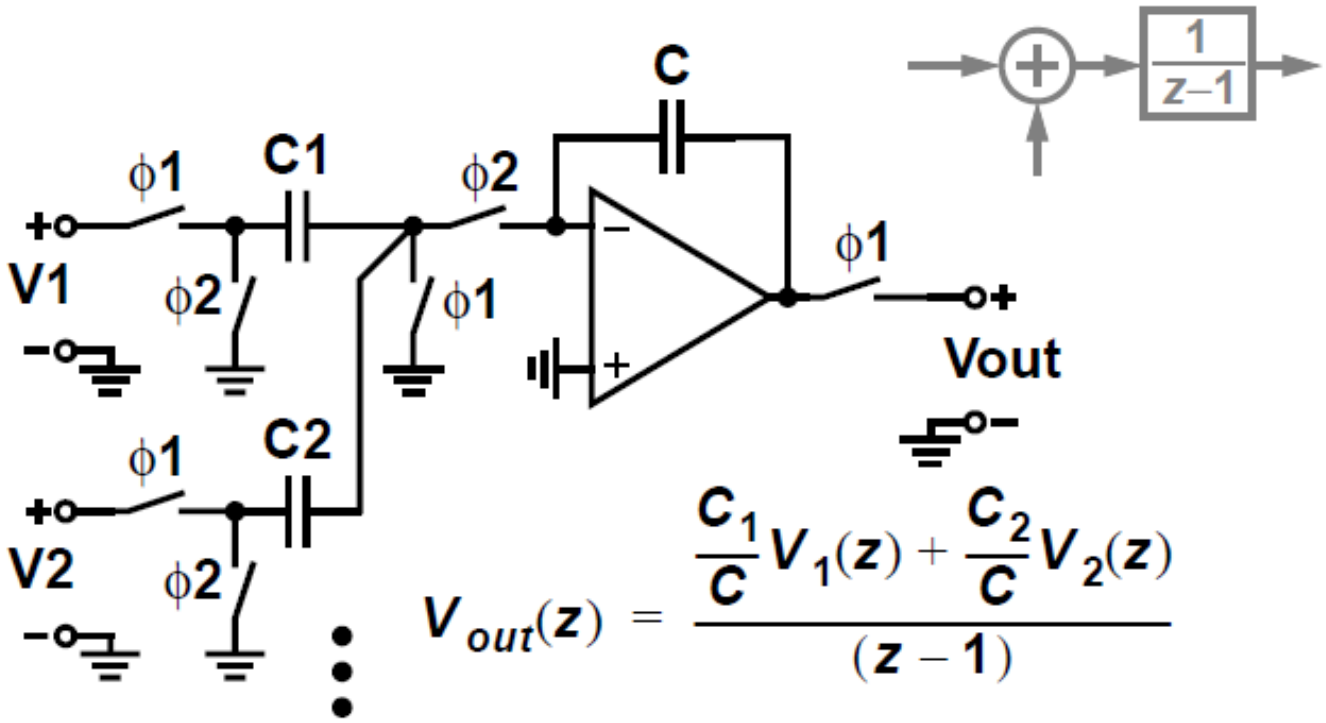
- Since $Q_1 = C_1 V_{in}$ and $Q_2 = C_2 V_{out}$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-1}$$

- Note that the voltage gain is controlled by a *ratio* of capacitors

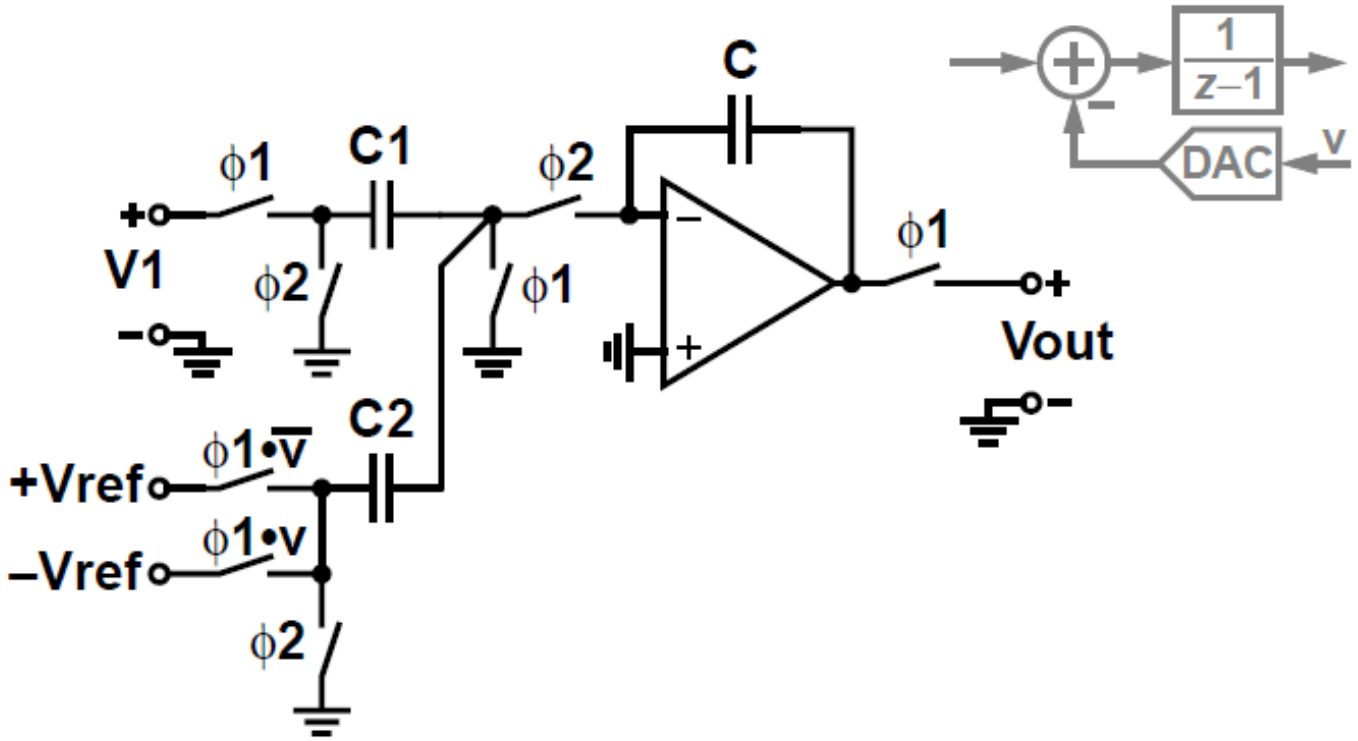
  With careful layout, 0.1% accuracy is possible.

Summation and Integration



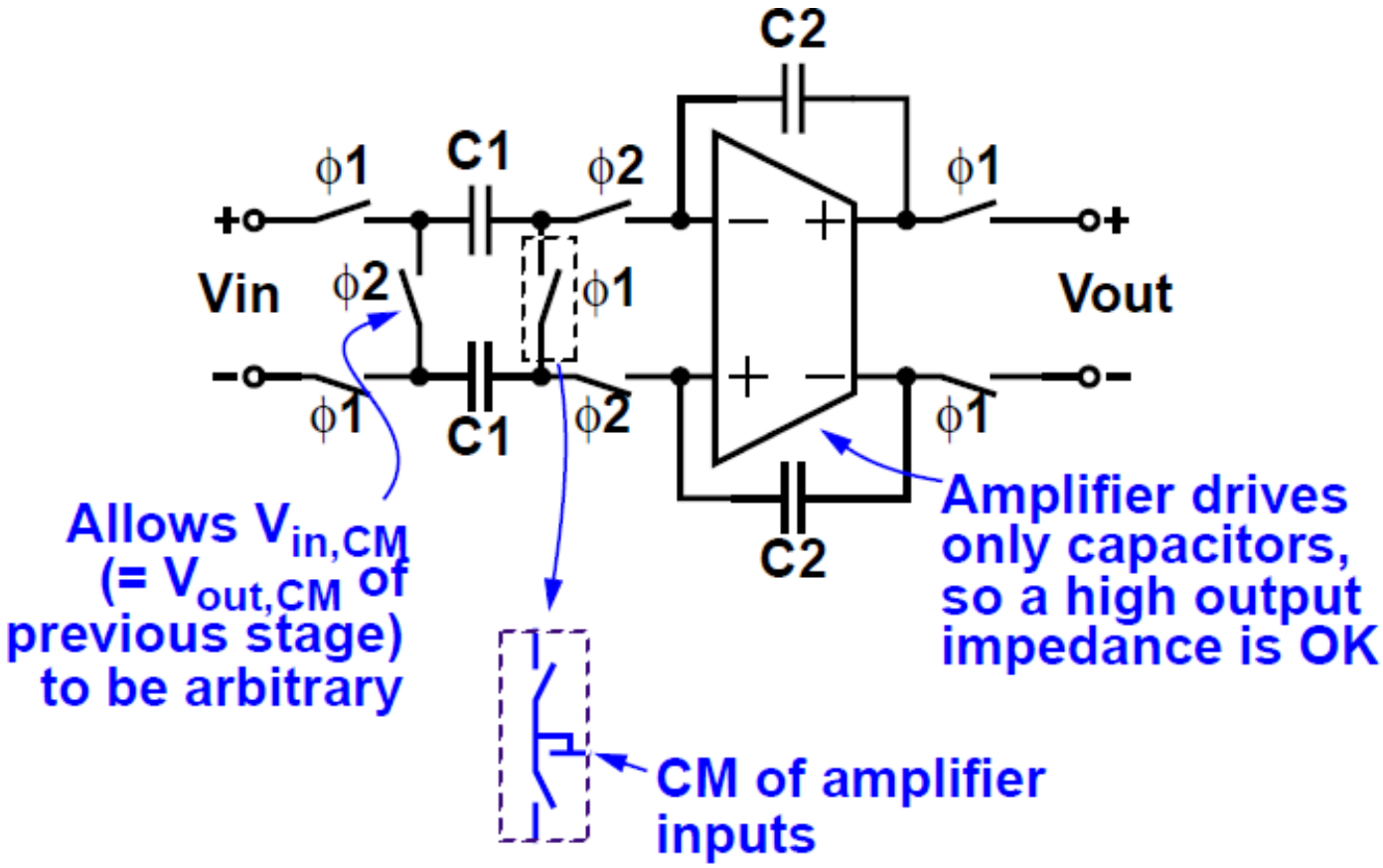
- Adding an extra input branch accomplishes addition, with weighting

1-bit DAC + Summation + Integration



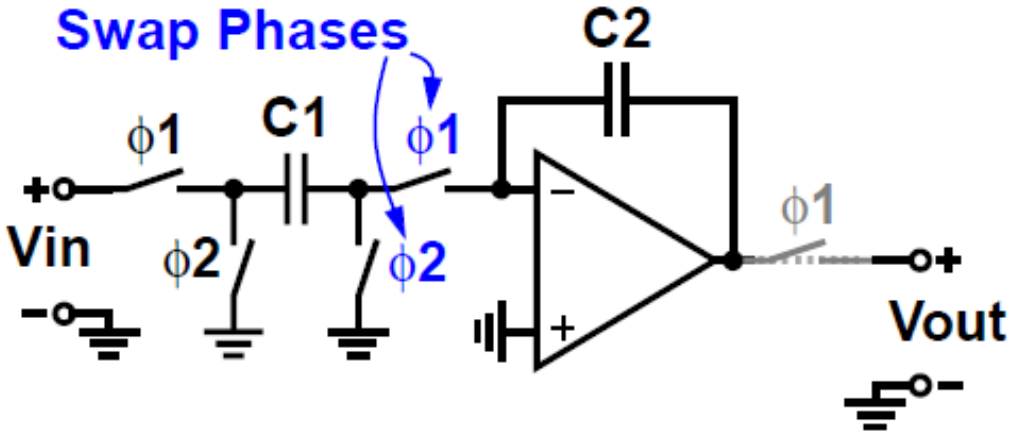
- 1-bit DAC by switching between references (+/-V_{ref})

Fully-Differential Integrator

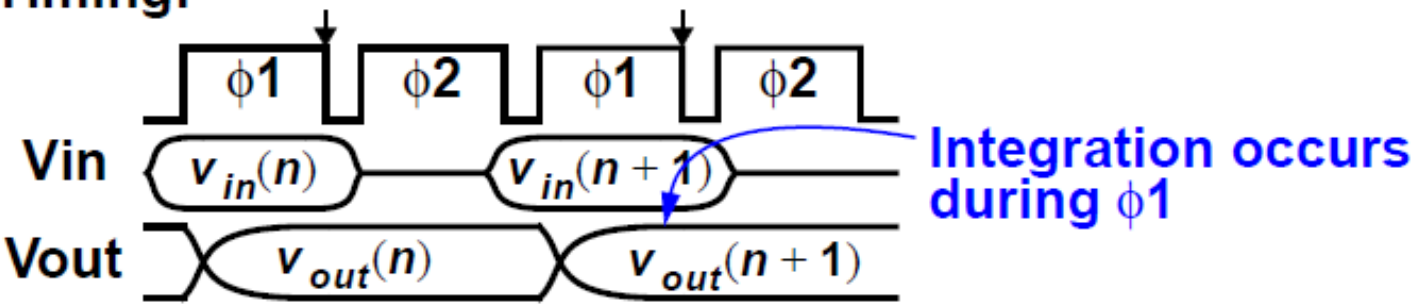


Non-Delaying Integrator

Single-ended circuit:

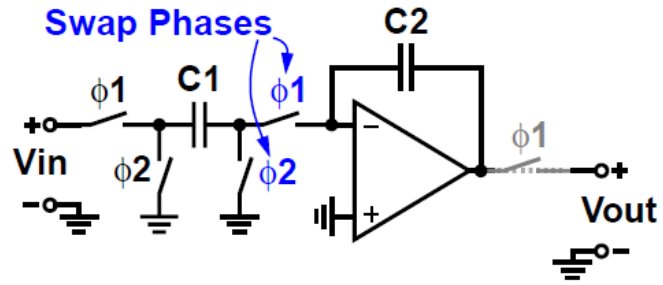


Timing:

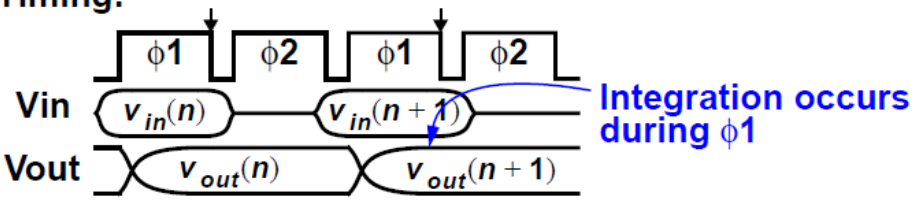


Non-Delaying Integrator contd.

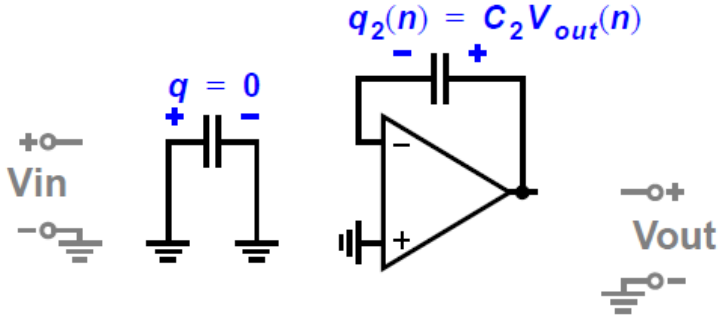
Single-ended circuit:



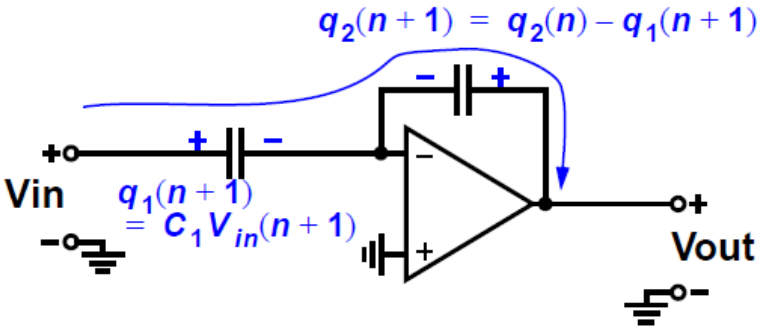
Timing:



ϕ2:



ϕ1:



Non-Delaying Integrator contd.

$$q_2(n+1) = q_2(n) - q_1(n+1)$$

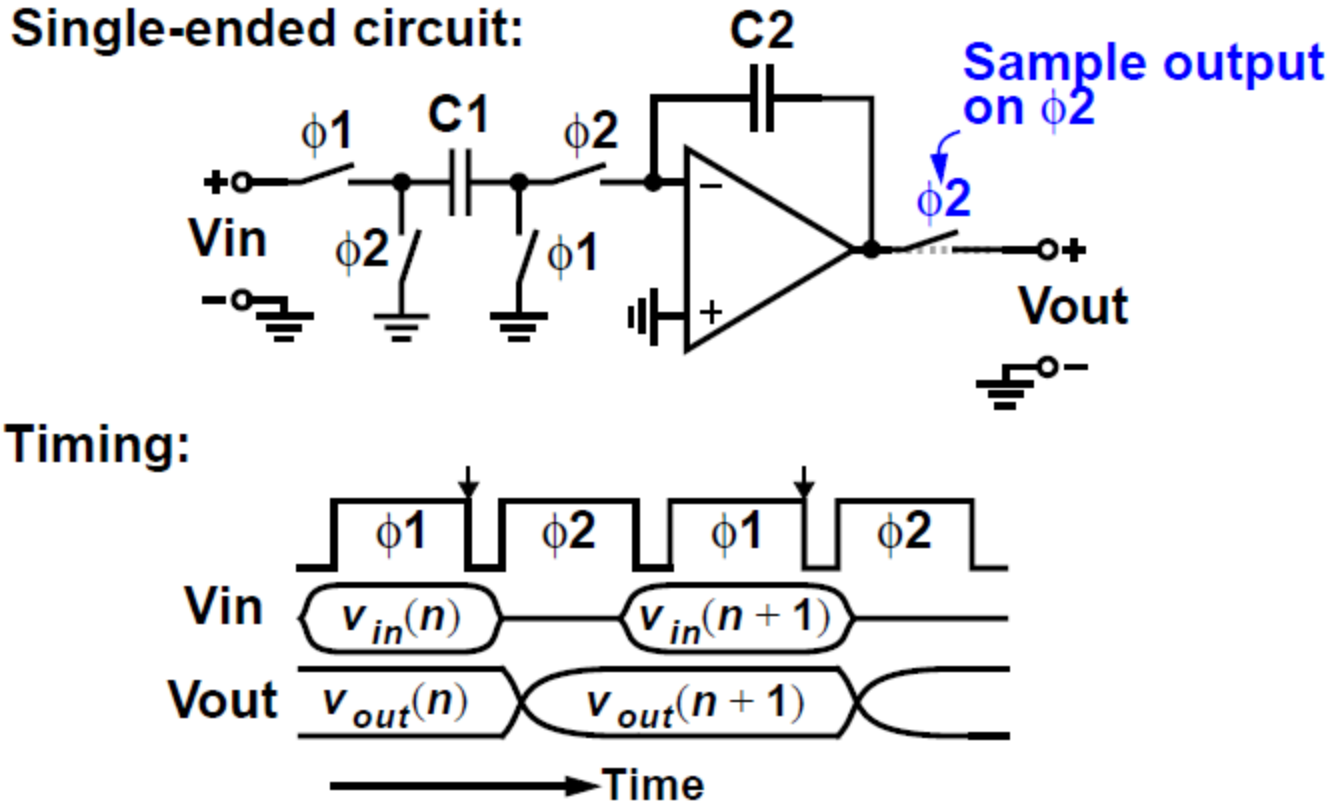
$$z\,Q_2(z) = Q_2(z) - z\,Q_1(z)$$

$$\frac{Q_2(z)}{Q_1(z)} = -\frac{z}{z-1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

- **Delaying (and inverting) integrator**

Half-Delay Integrator



Half-Delay Integrator

- Output is sampled on a different phase than the input
- Some use the notation to denote the shift in sampling time

$$H(z) = \frac{z^{-1/2}}{z-1}$$

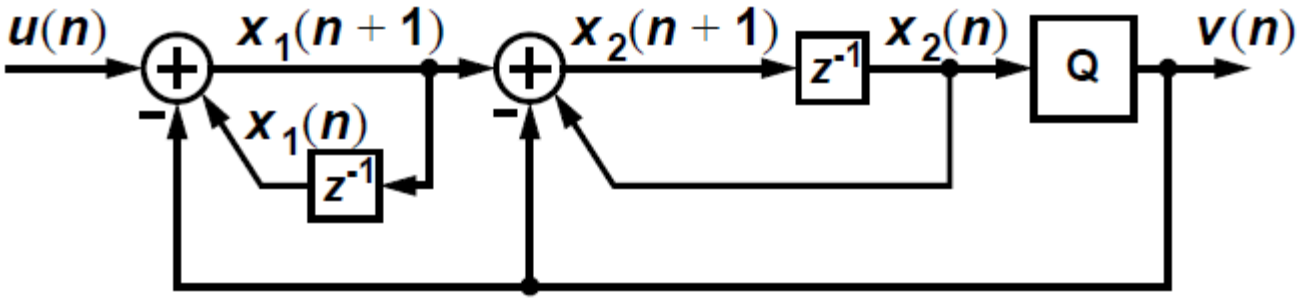
- An alternative method is to declare that the border between time ***n*** *and* ***n+1*** *occurs at the end* of a specific phase, say $\boldsymbol{\varphi_2}$

➢ A circuit which samples on $\boldsymbol{\varphi_1}$ and updates on $\boldsymbol{\varphi_2}$ is non-delaying, i.e. $H(z) = z/(z-1)$

whereas a circuit which samples on $\boldsymbol{\varphi_2}$ and updates on $\boldsymbol{\varphi_1}$ is delaying, i.e. $H(z) = 1/(z-1)$

Timing in a ΔΣ Modulator

- **The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations**
- **E.g. MOD2:**

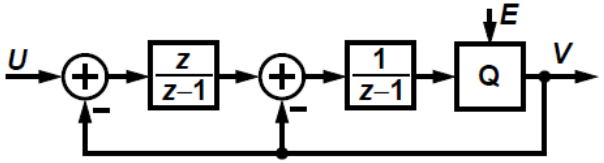


- **Difference Equations:**

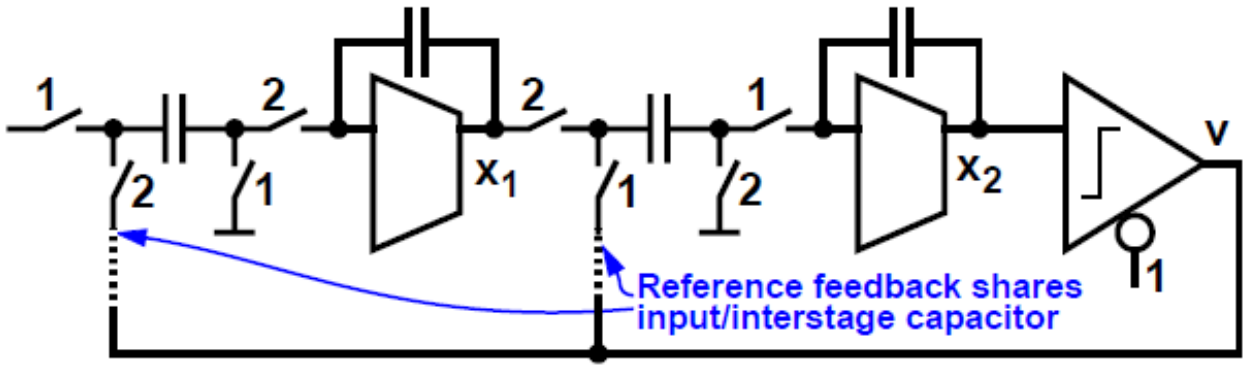
  Eq.0: $v(n) = Q(x_2(n))$

  Eq.1: $x_1(n+1) = x_1(n) - v(n) + u(n)$

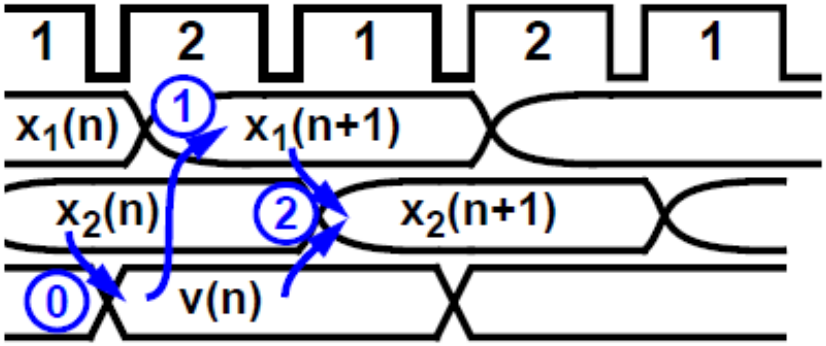
  Eq.2: $x_2(n+1) = x_2(n) - v(n) + x_1(n+1)$



Switched-Capacitor Realization



Timing



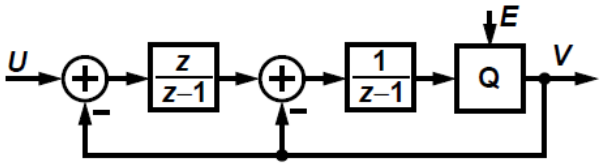
Timing looks OK!

Difference Equations:

Eq.0: $v(n) = Q(x_2(n))$

Eq.1: $x_1(n+1) = x_1(n) - v(n) + u(n)$

Eq.2: $x_2(n+1) = x_2(n) - v(n) + x_1(n+1)$



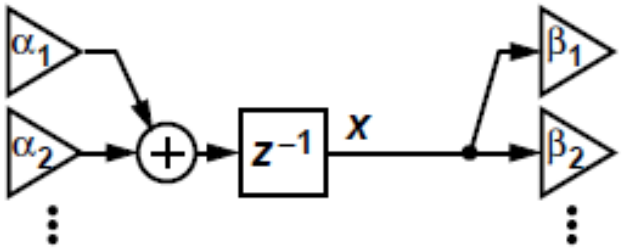
Signal Swing

- So far, we have not paid any attention to how much linear swing the op amps can support, or to the magnitudes of u, V_{ref}, x_1 and x_2
- For simplicity, assume:
  - the full-scale range of u is +/-1V
  - the opamp swing is also +/-1V and
  - V_{ref} = +/-1V
- We still need to know the ranges of $x1$ and $x2$ in order to accomplish *dynamic-range scaling*

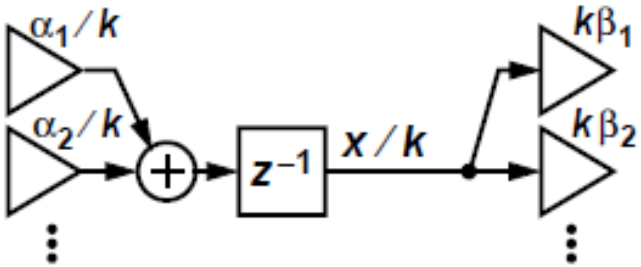
Dynamic Range Scaling

- In a linear system with known state bounds, the states can be scaled to occupy any desired range
- Use state-space similarity transform for dynamic range scaling

e.g. one state of original system

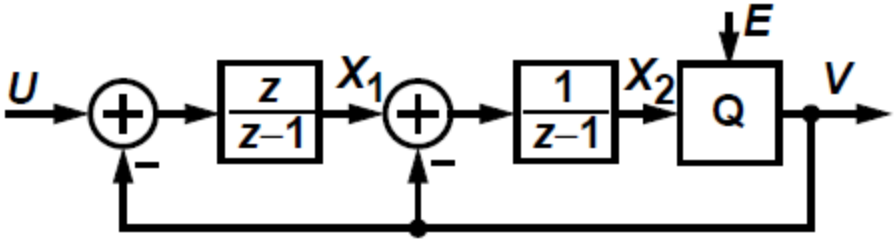


The state scaled by 1/*k*



State Swings in MOD2

- **Using linear theory**



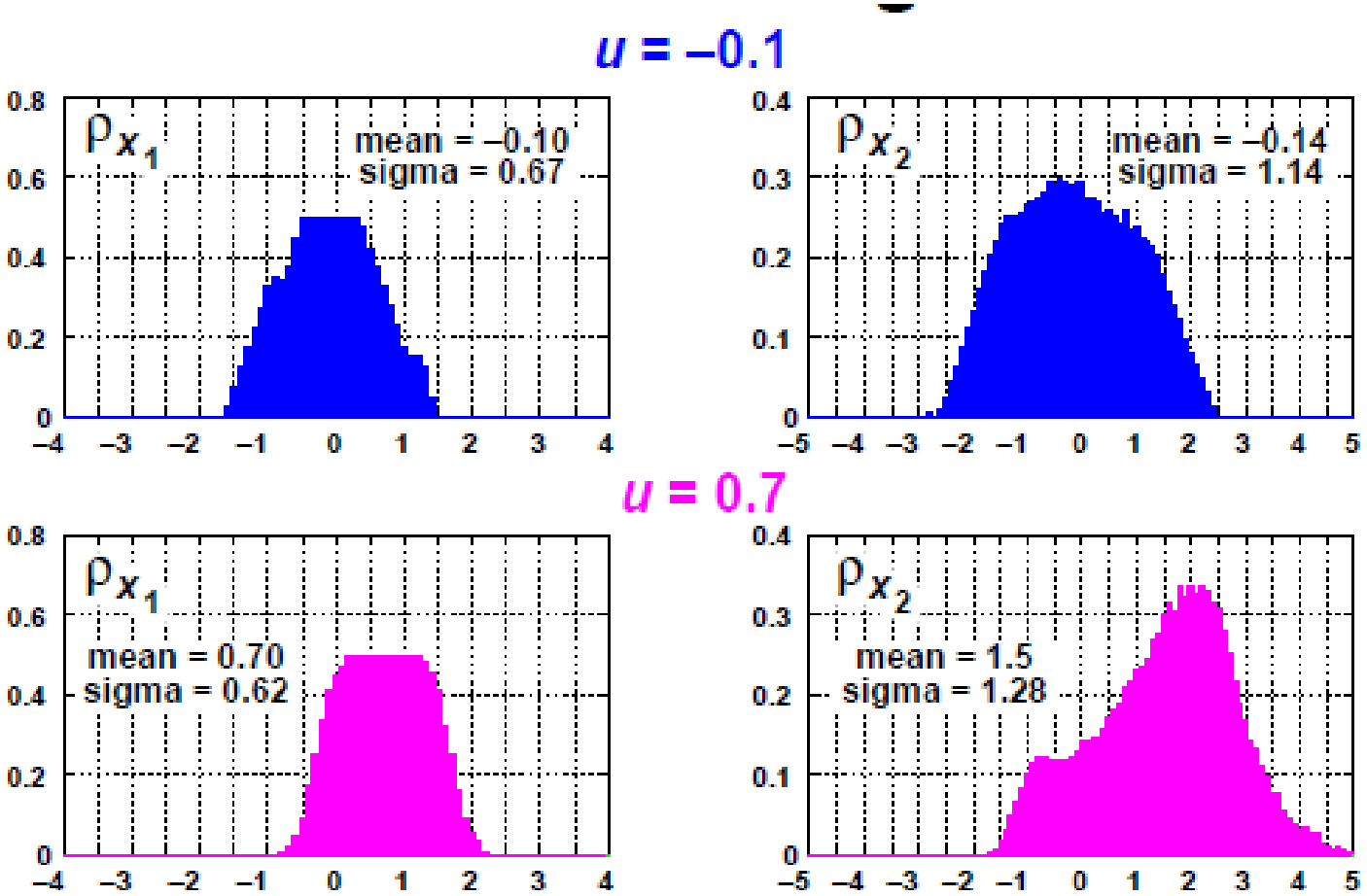
$$V = z^{-1}U + (1 - z^{-1})^2 E$$

$$X_1 = \frac{z}{z-1}(U - V) = U - (1 - z^{-1})E$$

$$X_2 = V - E = z^{-1}U + (-2z^{-1} + z^{-2})E$$

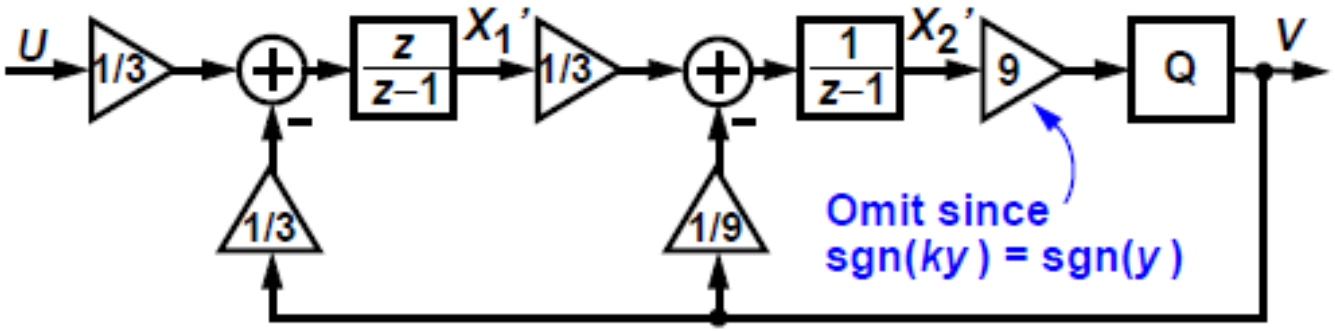
- **If u is constant and E is white with power $\sigma_e^2 = 1/3$, then**
  - **Mean (x_1) = u and $\sigma_{x1}^2 = 2\sigma_e^2 = 2/3$**
  - **Mean (x_2) = u and $\sigma_{x1}^2 = 5\sigma_e^2 = 5/3$**

Simulated Histograms



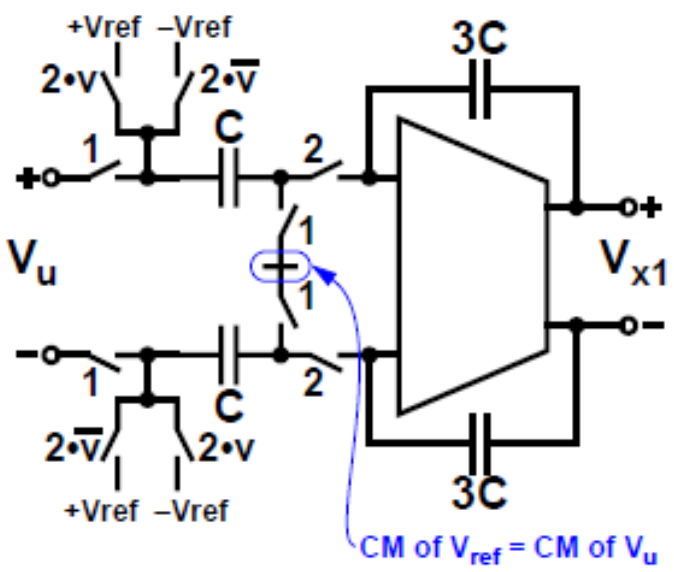
Scaled MOD2

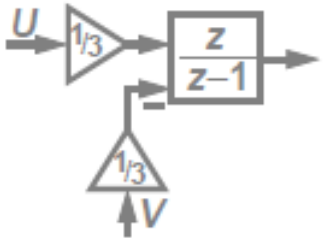
- **Take $\|x_1\|_\infty=3$ and $\|x_2\|_\infty=9$**
  - **The first integrator should not saturate**
  - **The second integrator will not saturate for DC inputs up to –3 dBFS and possibly as high as –1 dBFS.**
- **Our scaled version of MOD2 is then**



First Integrator (INT1)

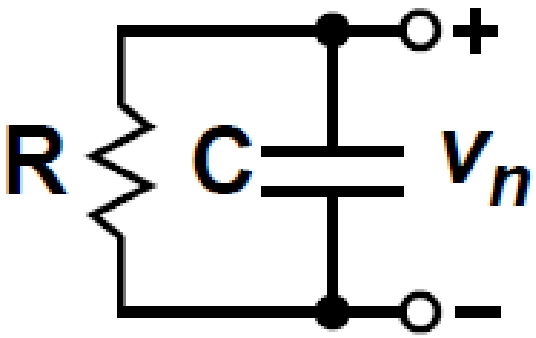
- **Share Input and Reference Caps**





- **What is the optimal value for C ?**

Thermal - kT/C - Noise



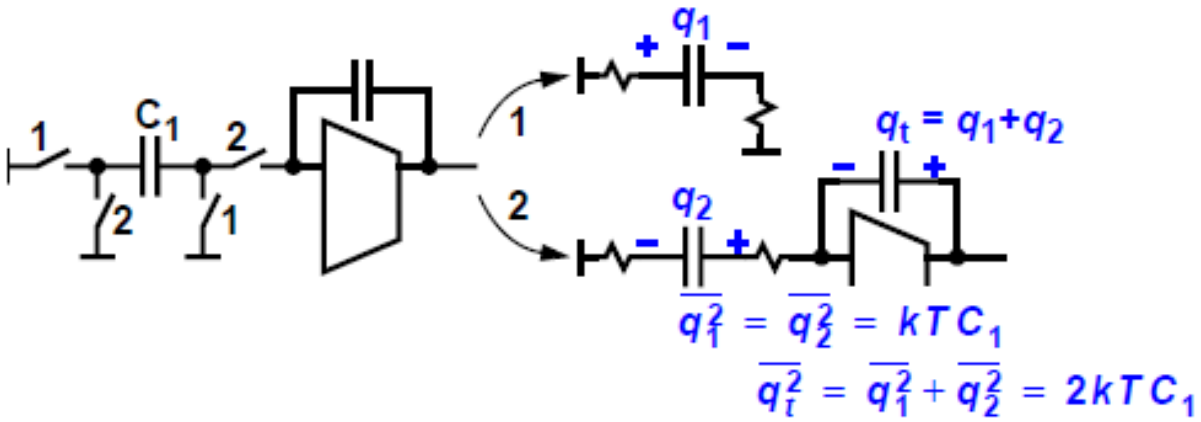
- **From ECE 614 Noise Analysis: Regardless of the value of *R*, the mean square value of the voltage on *C* is**

$$\overline{v_n^2} = \frac{kT}{C}$$

where *k* = 1.38 ×10–23 J/K is *Boltzmann's constant* and *T* is the temperature in Kelvin

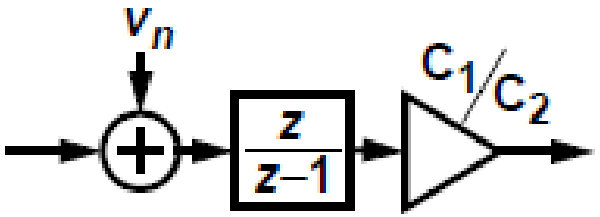
Noise in SC Integrator

- **Each charge/discharge operation has a random component**
  - **The amplifier plays a role during phase 2, but lets assume that the noise in both phases is just kT/C.**
- **For a given cap, these random components are essentially uncorrelated, so the noise is white**



Noise in SC Integrator contd.

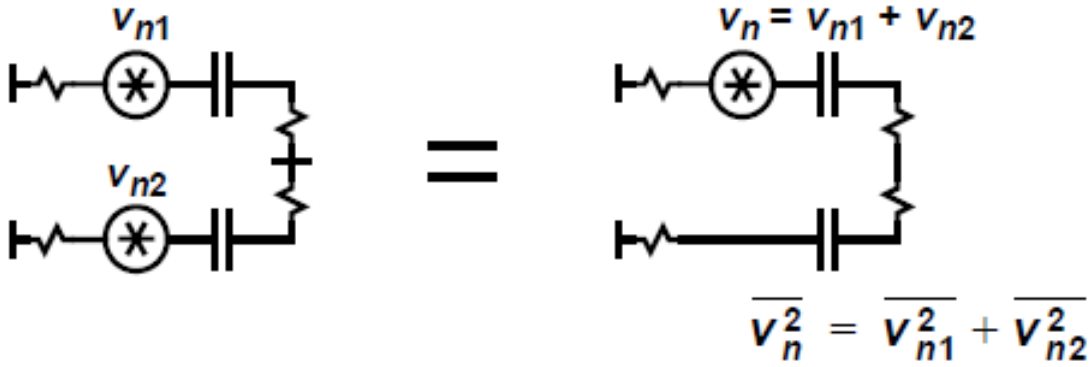
- **This noise charge is equivalent to a noise voltage with ms value $v_n^2=2kT/C_1$ added to the input of the integrator:**



- **This noise power is spread uniformly over all frequencies from 0 to $f_s/2$**

- **The power in the signal band is v_n^2/OSR**

Differential Noise



- **Twice as many switched caps**

⇒ twice as much noise power

- **The input-referred noise power in our differential integrator is**
- **$V_n^2 = 4kT/C_1$**

INT1 Cap Sizes

For SNR = 100 dB @ –3-dBFS input

- The signal power is

$$\overline{v_s^2} = \underbrace{\frac{1}{2}}_{-3\ \text{dBFS}} \bullet \frac{(1\ \text{V})^2}{2} = 0.25\ \text{V}^2$$

$\frac{A^2}{2}$

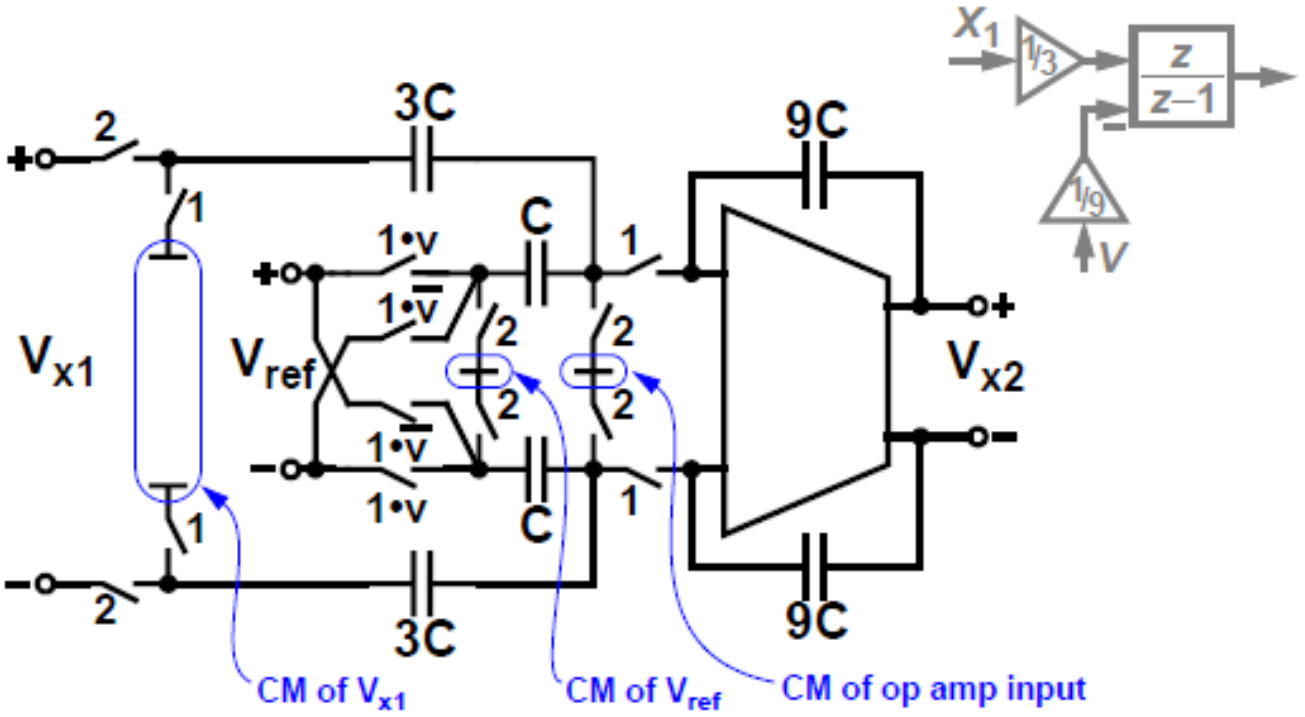
- Therefore we want $\overline{v_{n,\ \text{in-band}}^2} = 0.25 \times 10^{-10}\ \text{V}^2$
- Since $\overline{v_{n,\ \text{in-band}}^2} = \overline{v_n^2}/OSR$

$$C_1 = \frac{4kT}{\overline{v_n^2}} = 1.33\ \text{pF}$$

- If we want 10 dB more SNR, we need 10x caps

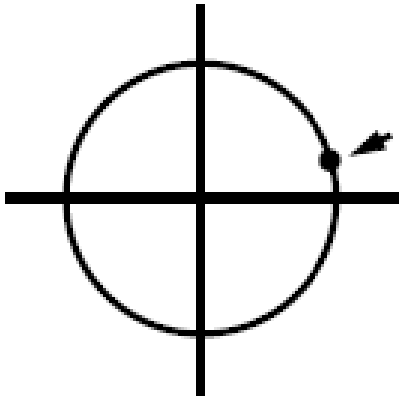
Second Integrator (INT2)

- **Separate Input and Feedback Caps**



INT2 Cap Sizes

- In-band noise of second integrator is greatly attenuated



$$\omega_B = \frac{\pi}{OSR}$$

INT1 gain @ pb edge: $A = \frac{1/3}{\omega_B} = \frac{OSR}{3\pi}$

INT2 noise attenuation: $> OSR \cdot A^2 \approx 10^6$

$\Rightarrow$ Capacitor sizes not dictated by thermal noise

- Charge injection errors and desired ratio accuracy set absolute size

  A reasonable size for a small cap is currently ~10 fF.

Behavioral Schematic for S/C MOD2