ECE615 Mixed-Signal IC Design

Discrete-Time ΔΣ Modulator Implementation

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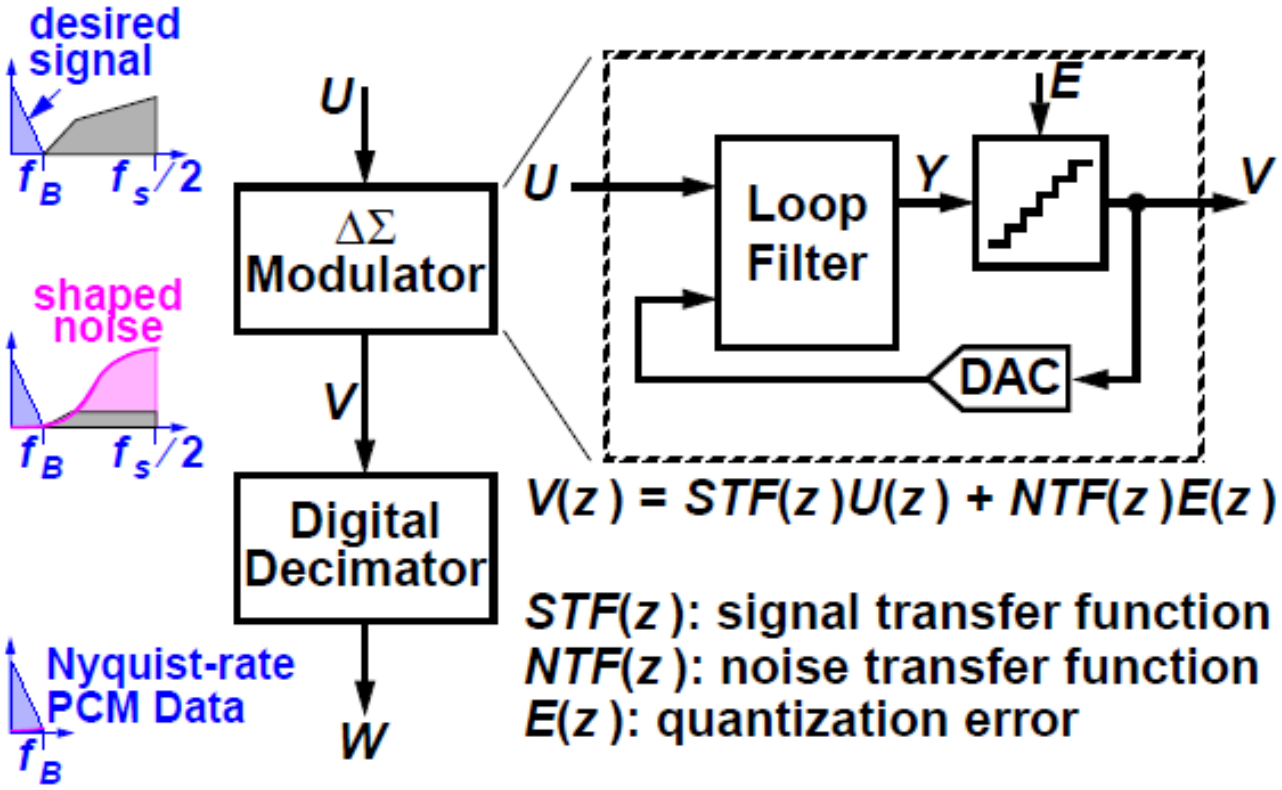
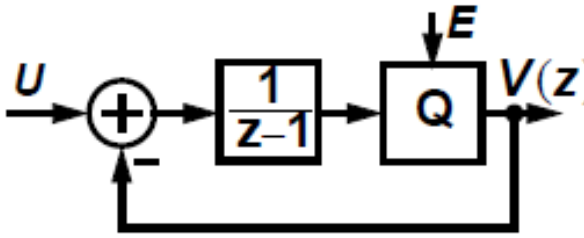
Review: A ΔΣ ADC System



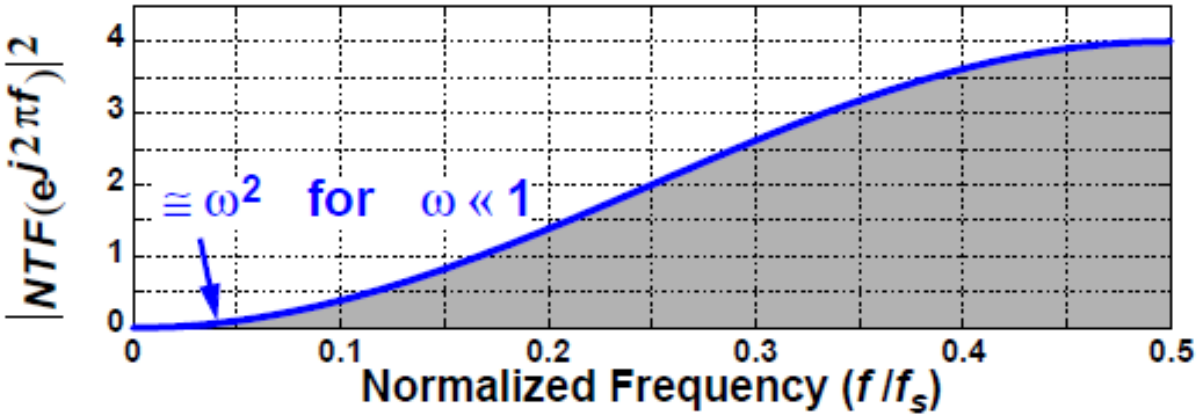
Review: MOD1



$$V(z) = NTF(z)E(z) + STF(z)U(z)$$

$$NTF(z) = (1 - z^{-1})$$

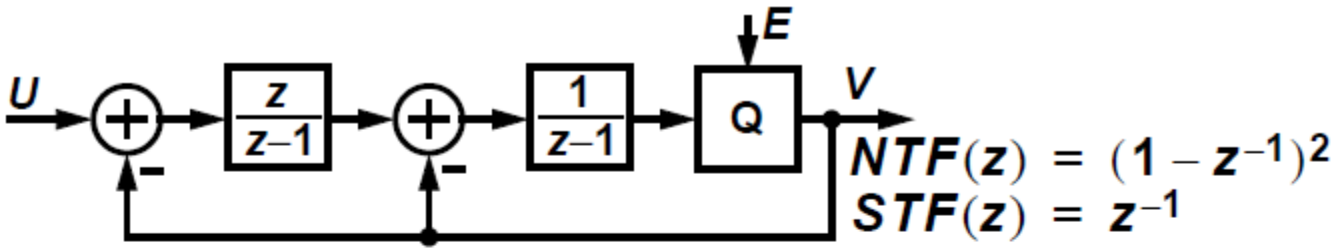
$$STF(z) = z^{-1}$$

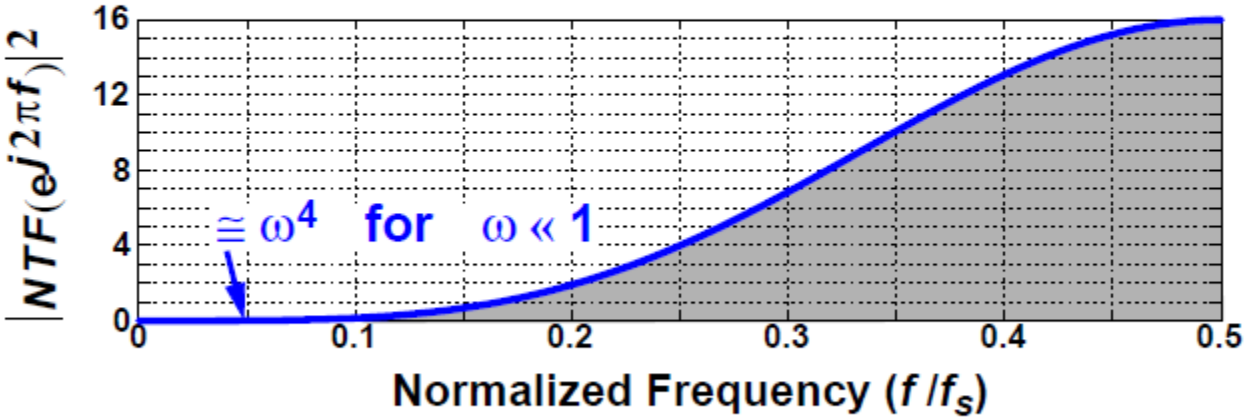


- **Doubling OSR improves SQNR by 9 dB**

  Peak SQNR $\approx$ dbp$(9 \cdot OSR^3/(2\pi^2))$; dbp$(x) \equiv 10\log_{10}(x)$

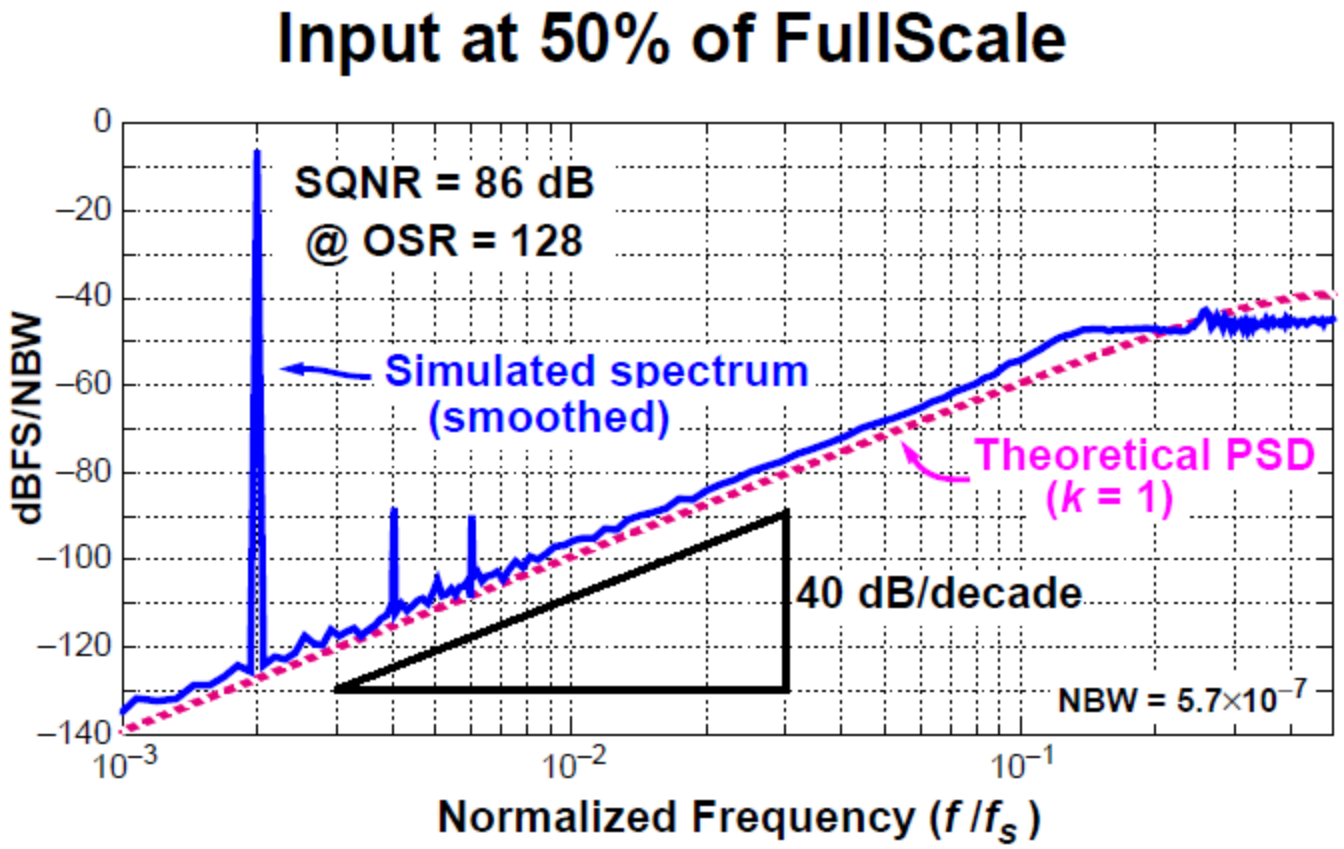
Review: MOD2





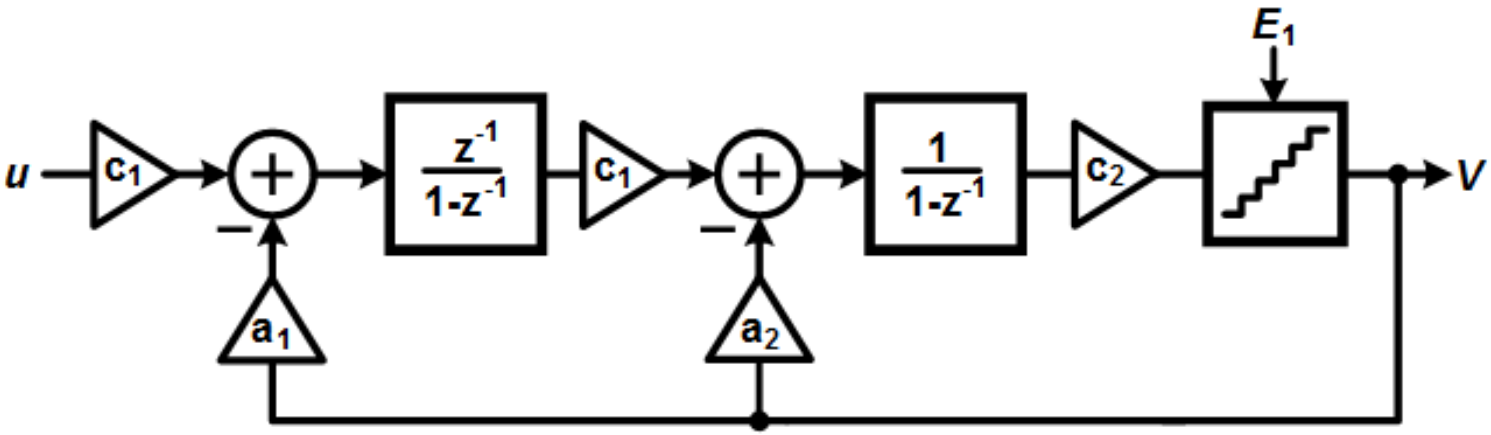
- **Doubling OSR improves SQNR by 15 dB**
  Peak SQNR $\approx$ dbp$((15 \cdot OSR^5)/(4\pi^4))$

Review: Simulated MOD2 PSD



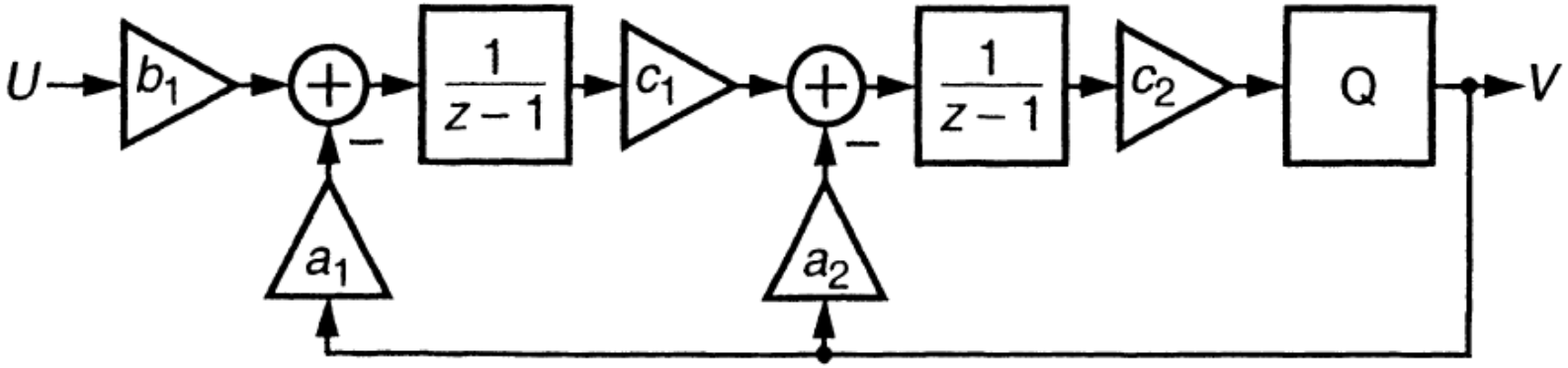
Example Design: 2nd-order Modulator

Parameter	Symbol	Value	Units
Bandwidth	f_B	1	kHz
Sampling Frequency	f_s	1	MHz
Signal-to-Noise Ratio	SNR	100	dB
Supply Voltage	VDD	3	V



NTF Design

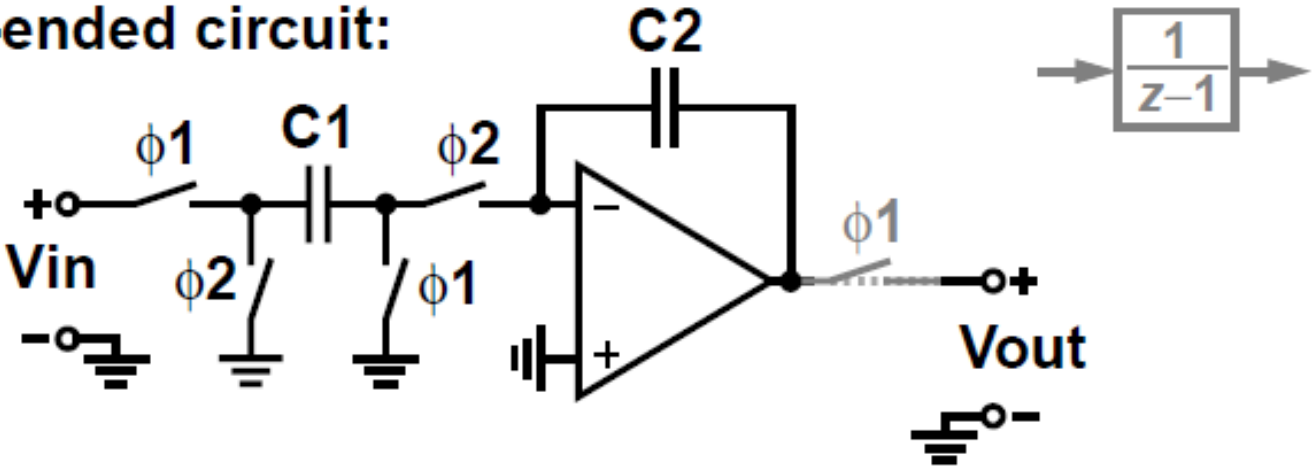
Block Diagram



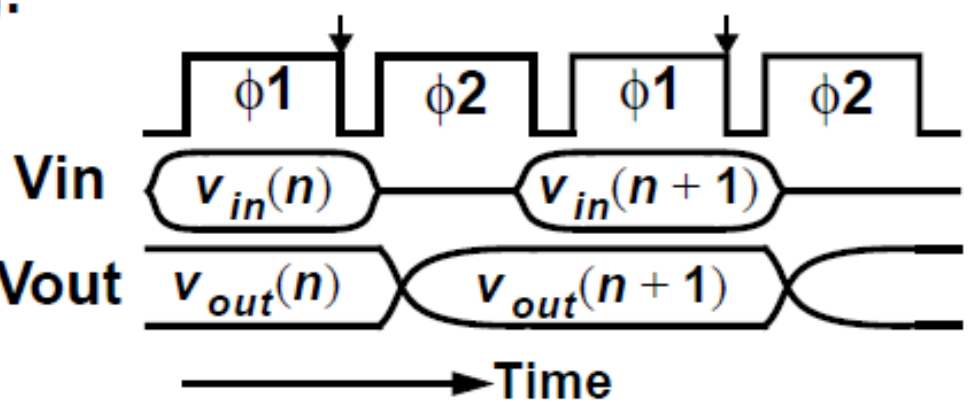
- Summation blocks
- Delaying and non-delaying discrete-time
- integrators
- Quantizer (1-bit)
- Feedback DACs (1-bit)
- Decimation filter (not shown)
  - Digital and therefore “easy”

Switched-Capacitor Integrator

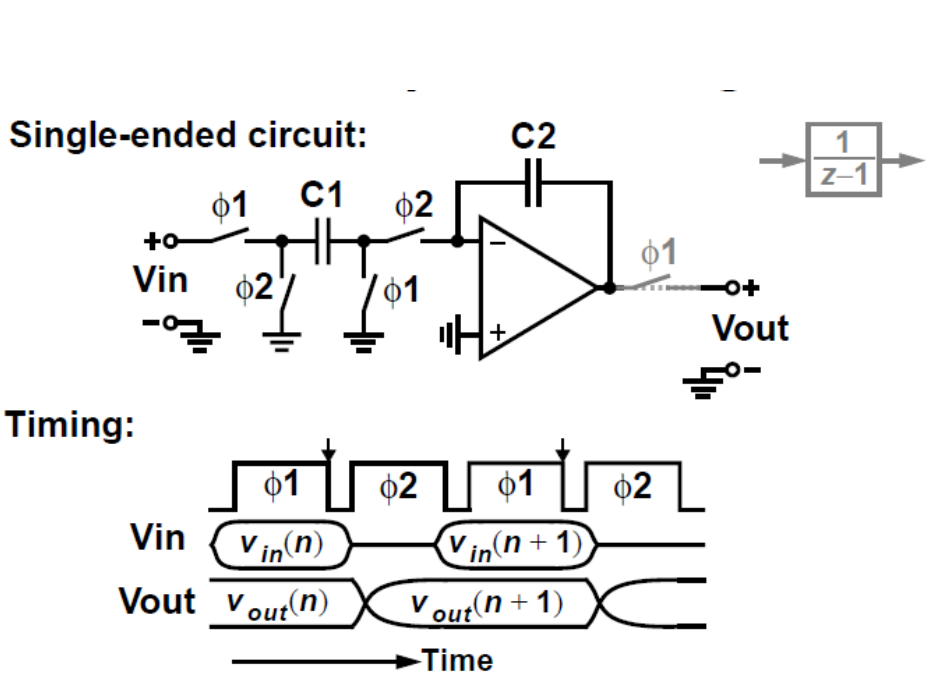
Single-ended circuit:

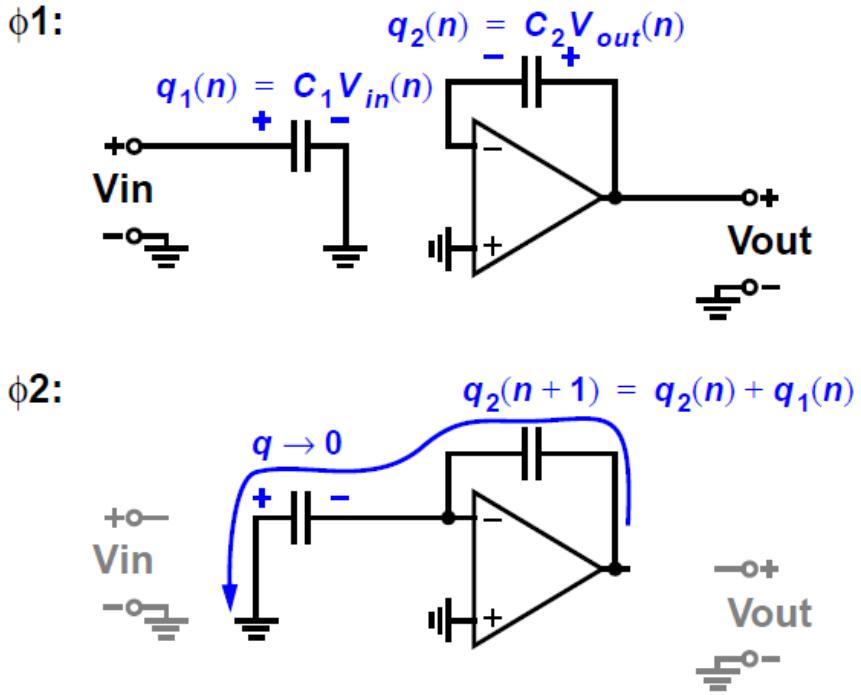


Timing:



Switched-Capacitor Integrator contd.





Switched-Capacitor Integrator contd.

$$q_2(n+1) = q_2(n) + q_1(n)$$

$$z\,Q_2(z) = Q_2(z) + Q_1(z)$$

$$Q_2(z) = \frac{Q_1(z)}{z-1}$$

- This circuit integrates charge

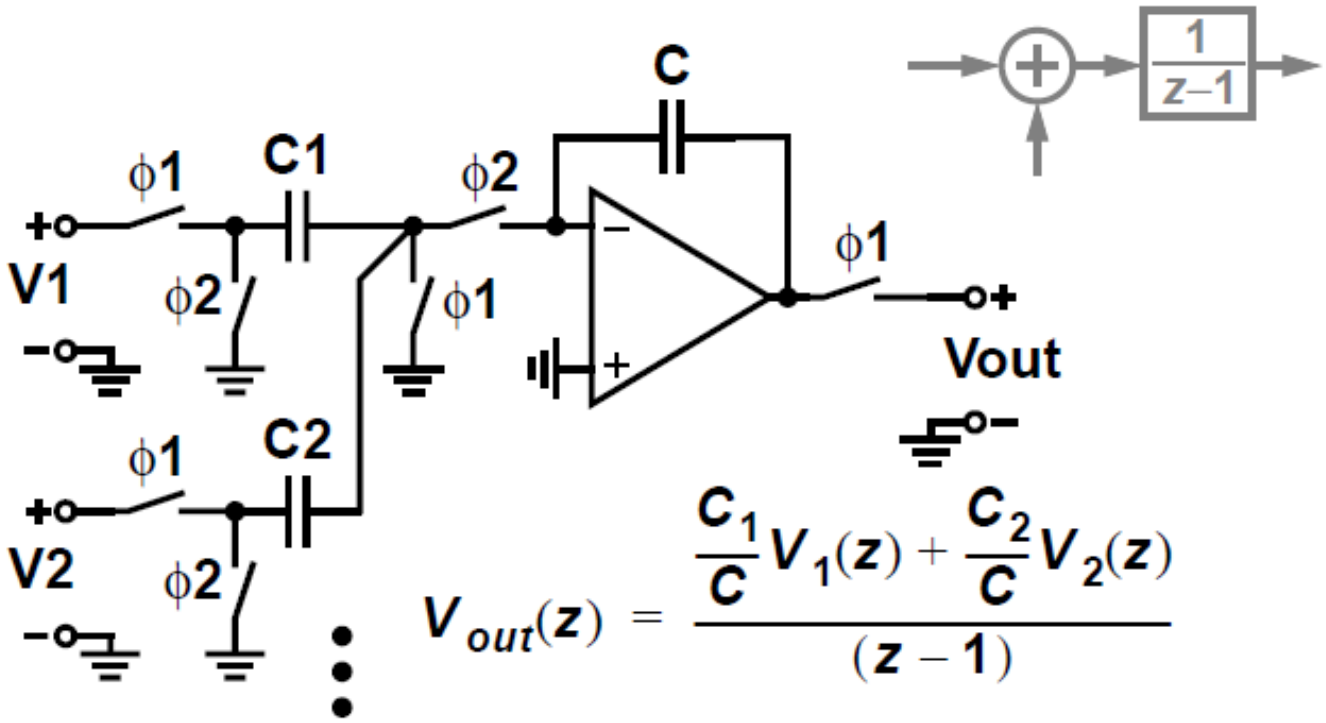
- Since $Q_1 = C_1 V_{in}$ and $Q_2 = C_2 V_{out}$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-1}$$

- Note that the voltage gain is controlled by a *ratio* of capacitors

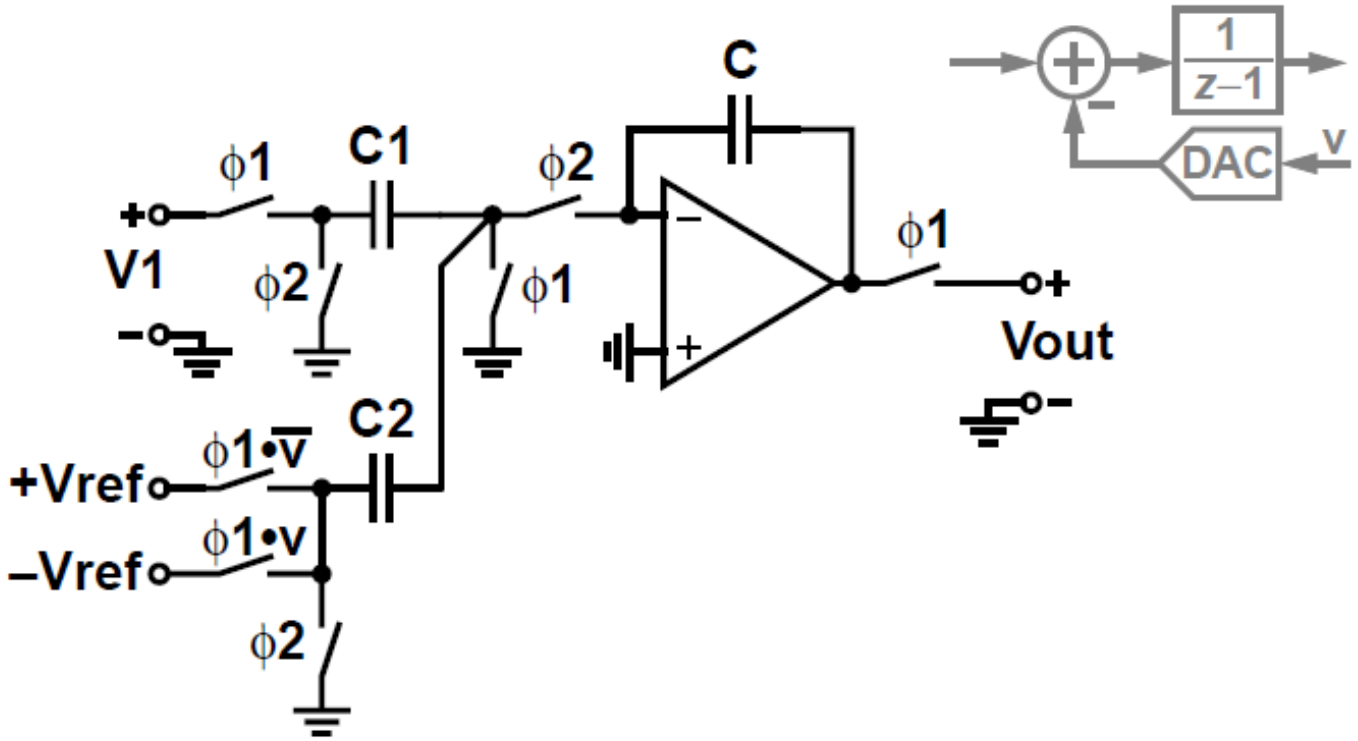
  With careful layout, 0.1% accuracy is possible.

Summation and Integration



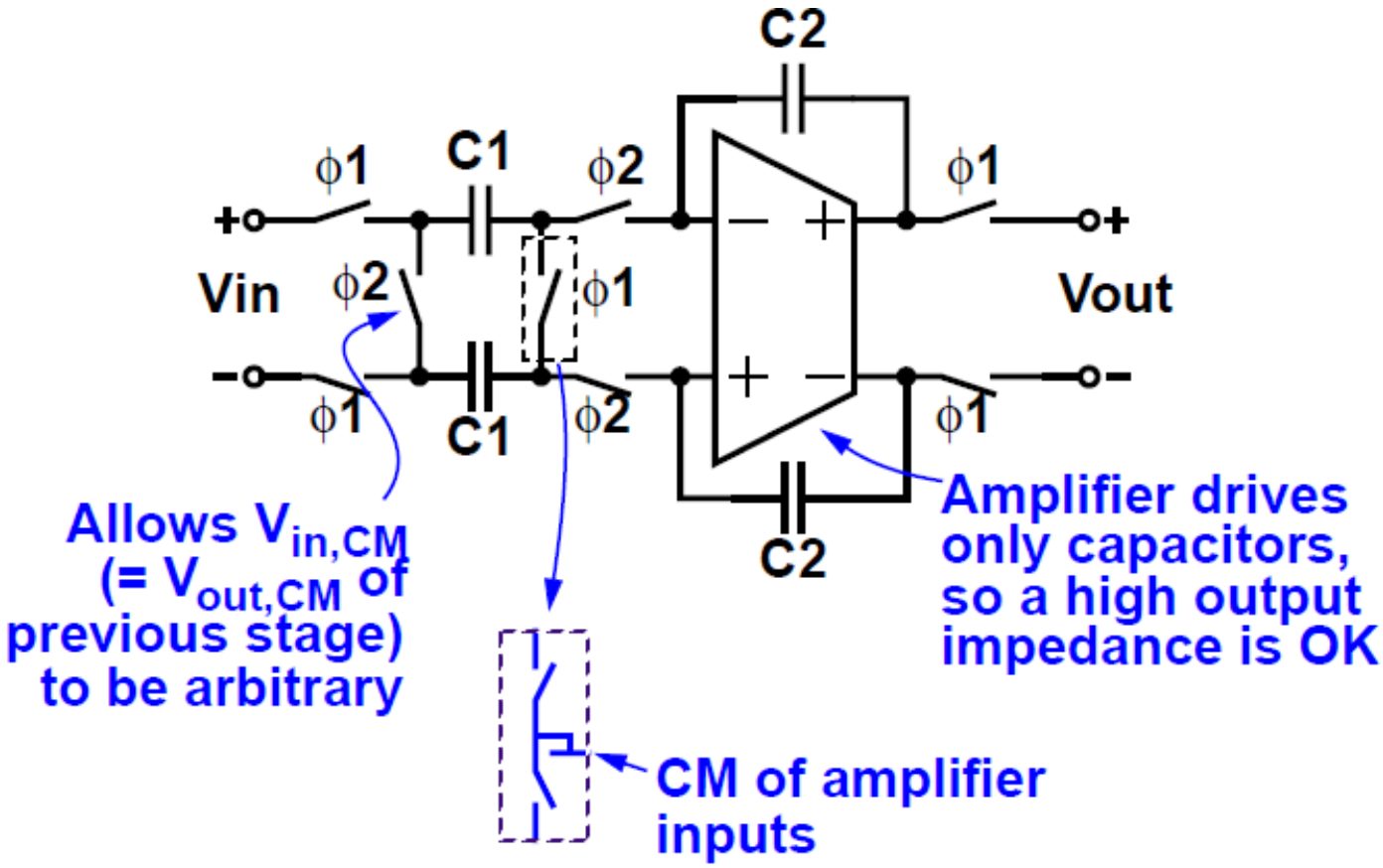
- Adding an extra input branch accomplishes addition, with weighting

1-bit DAC + Summation + Integration



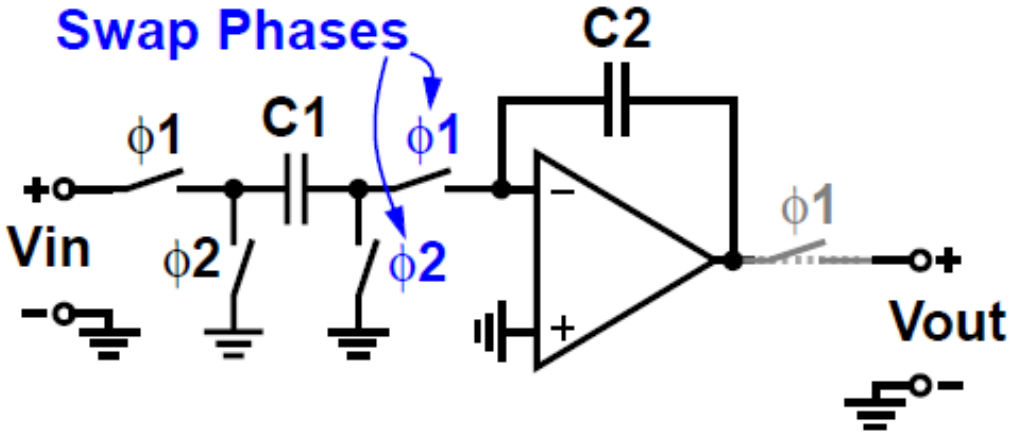
- 1-bit DAC by switching between references (+/-V_{ref})

Fully-Differential Integrator

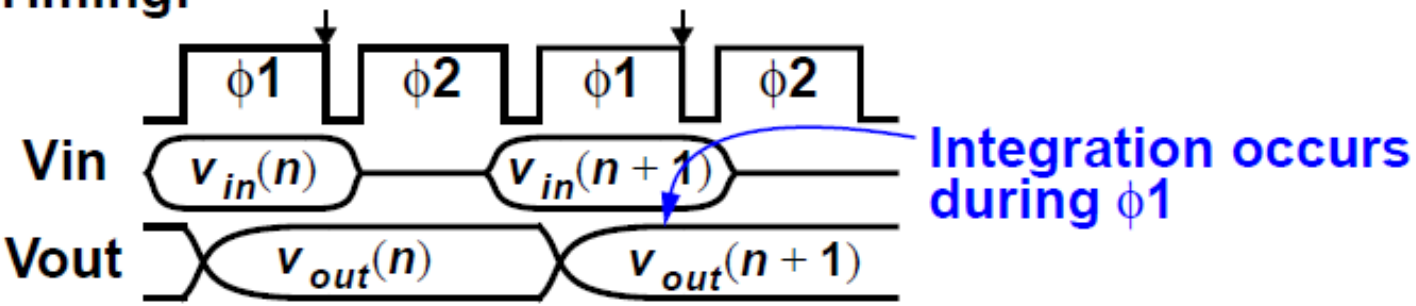


Non-Delaying Integrator

Single-ended circuit:

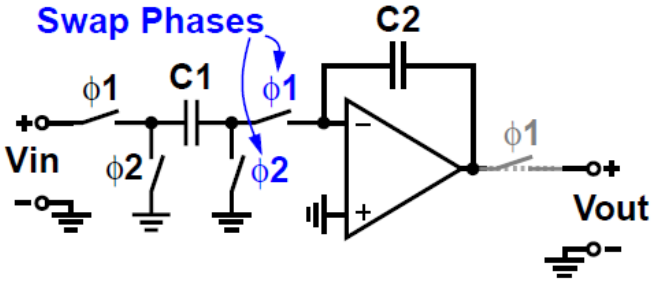


Timing:

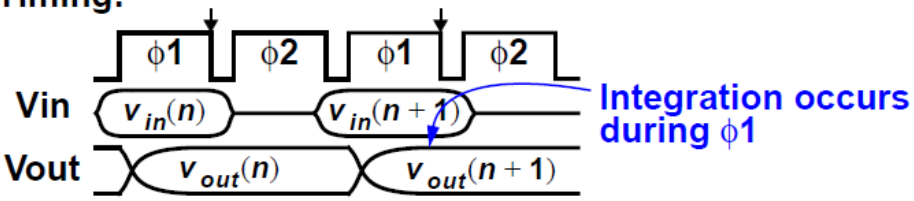


Non-Delaying Integrator contd.

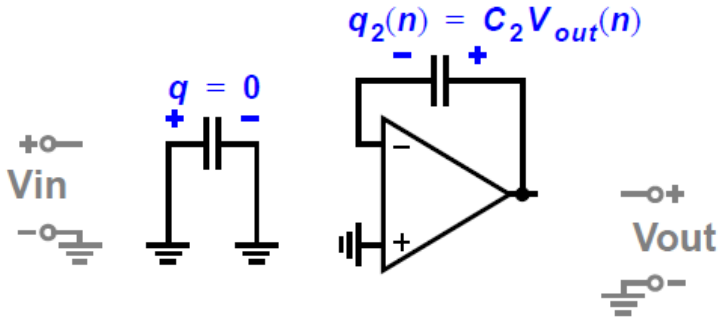
Single-ended circuit:



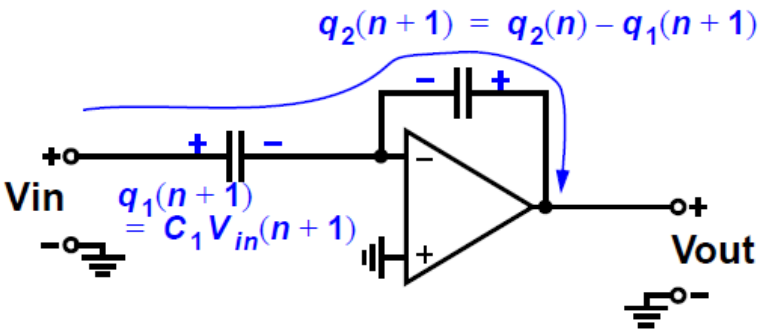
Timing:



ϕ2:



ϕ1:



Non-Delaying Integrator contd.

$$q_2(n+1) = q_2(n) - q_1(n+1)$$

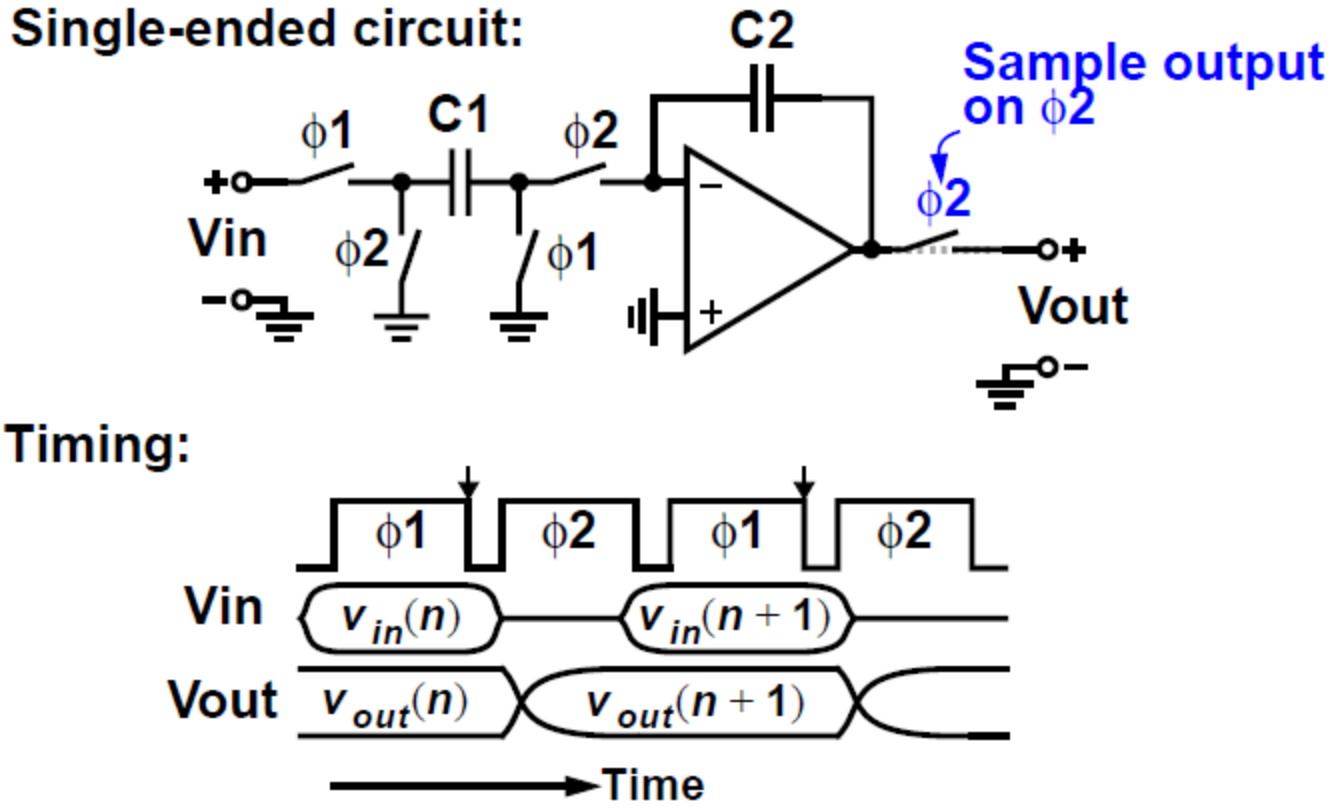
$$z\,Q_2(z) = Q_2(z) - z\,Q_1(z)$$

$$\frac{Q_2(z)}{Q_1(z)} = -\frac{z}{z-1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

- **Delaying (and inverting) integrator**

Half-Delay Integrator



Half-Delay Integrator

- Output is sampled on a different phase than the input
- Some use the notation to denote the shift in sampling time

$$H(z) = \frac{z^{-1/2}}{z-1}$$

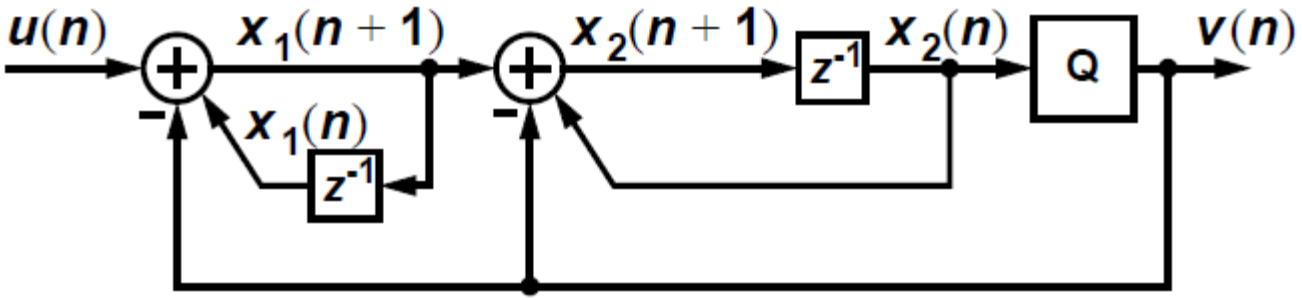
- An alternative method is to declare that the border between time ***n*** *and* ***n+1*** *occurs at the end* of a specific phase, say $\boldsymbol{\varphi_2}$

➢ A circuit which samples on $\boldsymbol{\varphi_1}$ and updates on $\boldsymbol{\varphi_2}$ is non-delaying, i.e. $H(z) = z/(z-1)$

whereas a circuit which samples on $\boldsymbol{\varphi_2}$ and updates on $\boldsymbol{\varphi_1}$ is delaying, i.e. $H(z) = 1/(z-1)$

Timing in a ΔΣ Modulator

- **The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations**
- **E.g. MOD2:**

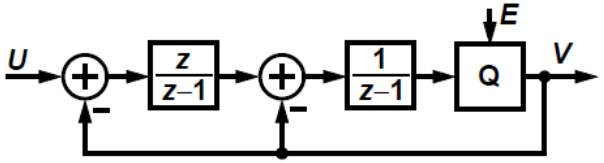


- **Difference Equations:**

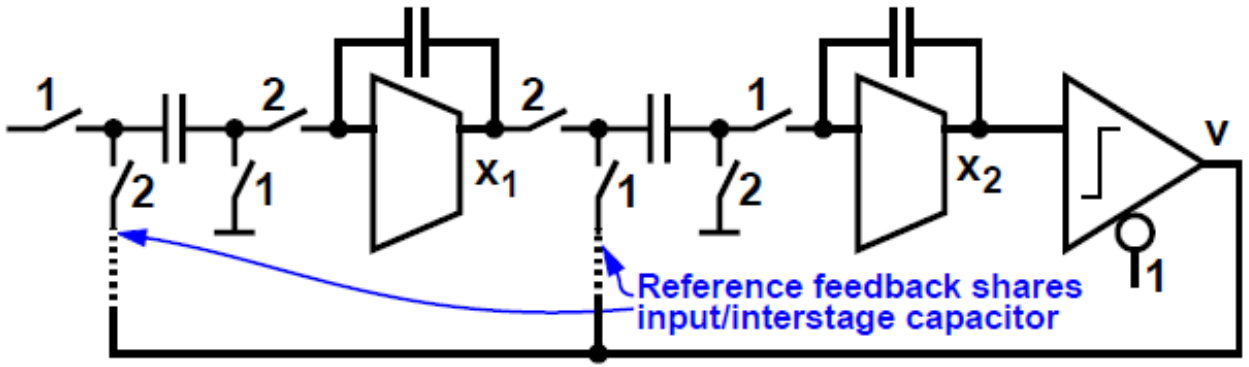
  Eq.0: $v(n) = Q(x_2(n))$

  Eq.1: $x_1(n+1) = x_1(n) - v(n) + u(n)$

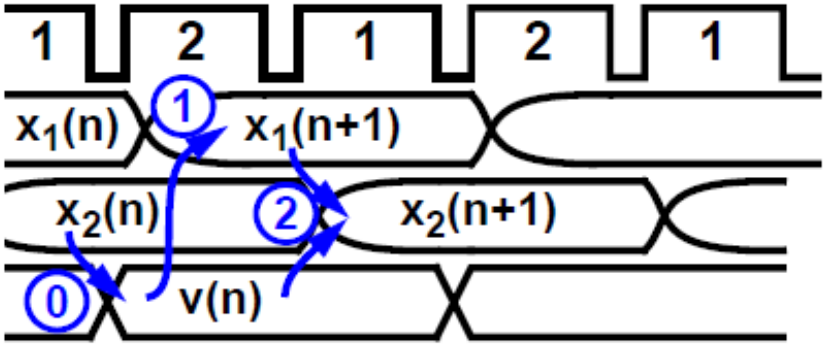
  Eq.2: $x_2(n+1) = x_2(n) - v(n) + x_1(n+1)$



Switched-Capacitor Realization



Timing



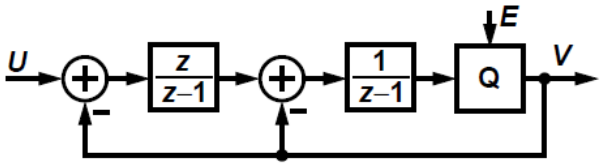
Timing looks OK!

Difference Equations:

Eq.0: $v(n) = Q(x_2(n))$

Eq.1: $x_1(n+1) = x_1(n) - v(n) + u(n)$

Eq.2: $x_2(n+1) = x_2(n) - v(n) + x_1(n+1)$



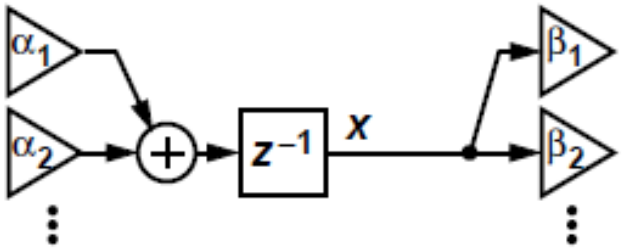
Signal Swing

- So far, we have not paid any attention to how much linear swing the op amps can support, or to the magnitudes of u, V_{ref}, x_1 and x_2
- For simplicity, assume:
  - the full-scale range of u is +/-1V
  - the opamp swing is also +/-1V and
  - V_{ref} = +/-1V
- We still need to know the ranges of x_1 and x_2 in order to accomplish *dynamic-range scaling*

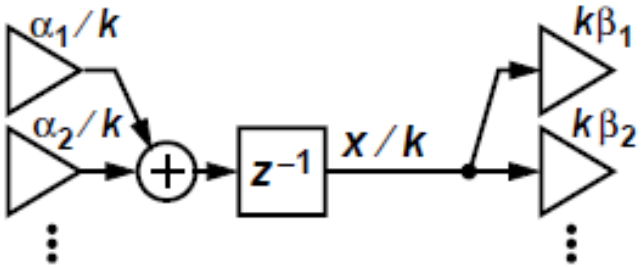
Dynamic Range Scaling

- In a linear system with known state bounds, the states can be scaled to occupy any desired range
- Use state-space similarity transform for dynamic range scaling

e.g. one state of original system

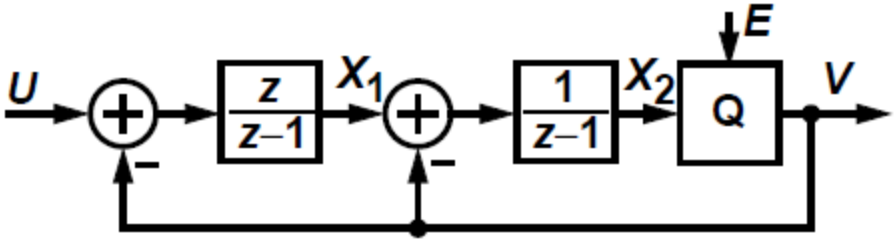


The state scaled by 1/*k*



State Swings in MOD2

- **Using linear theory**



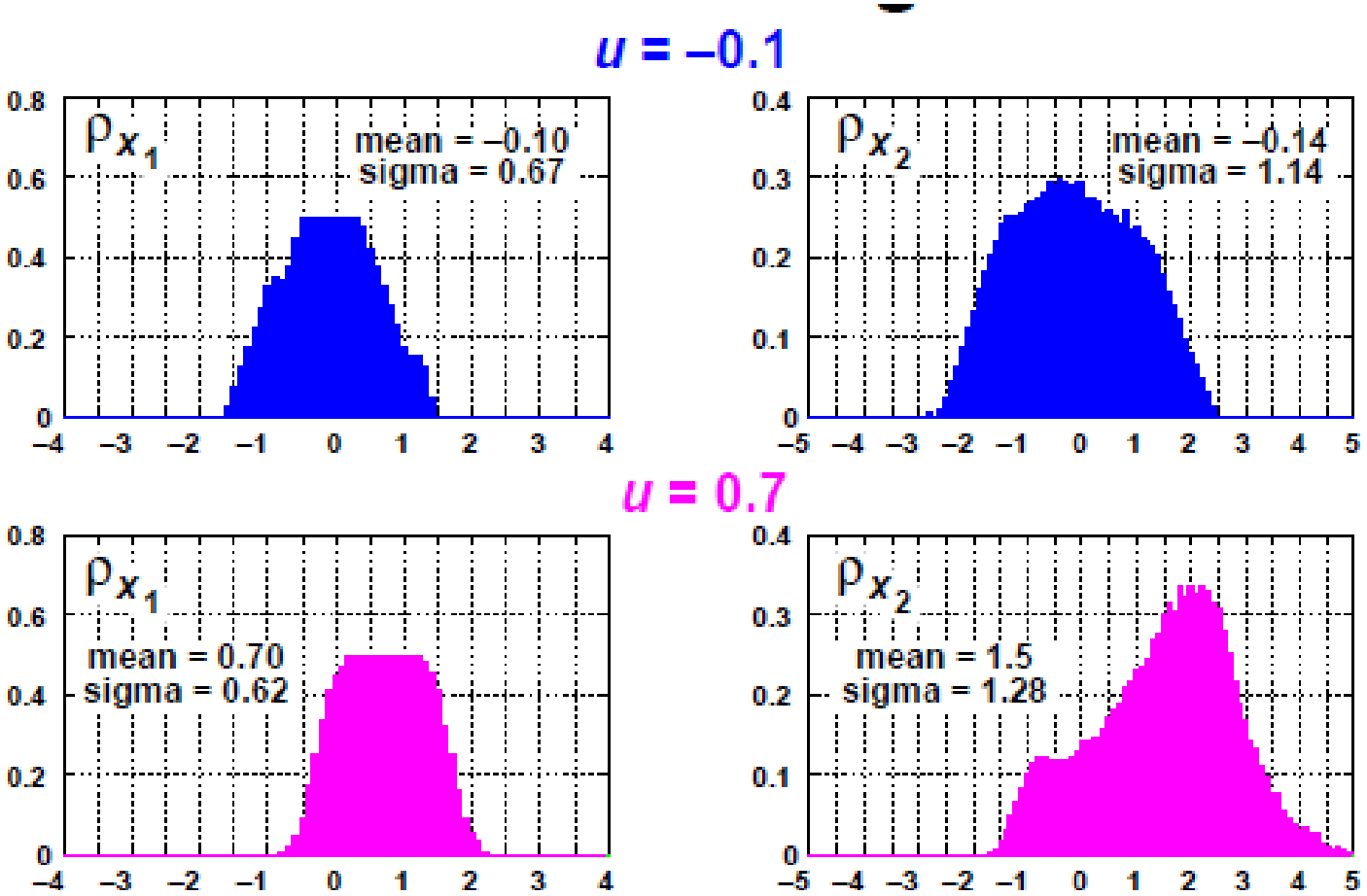
$$V = z^{-1}U + (1 - z^{-1})^2 E$$

$$X_1 = \frac{z}{z-1}(U - V) = U - (1 - z^{-1})E$$

$$X_2 = V - E = z^{-1}U + (-2z^{-1} + z^{-2})E$$

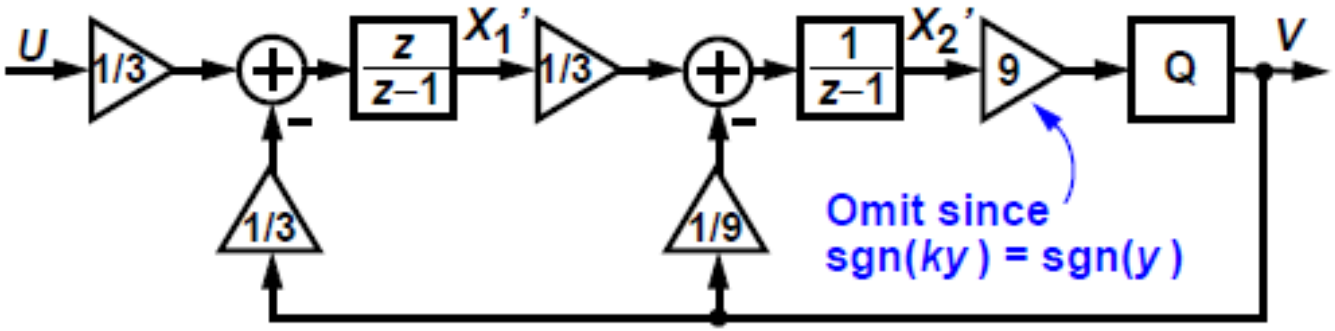
- **If u is constant and E is white with power $\sigma_e^2 = 1/3$, then**
  - **Mean (x_1) = u and $\sigma_{x1}^2 = 2\sigma_e^2 = 2/3$**
  - **Mean (x_2) = u and $\sigma_{x1}^2 = 5\sigma_e^2 = 5/3$**

Simulated Histograms



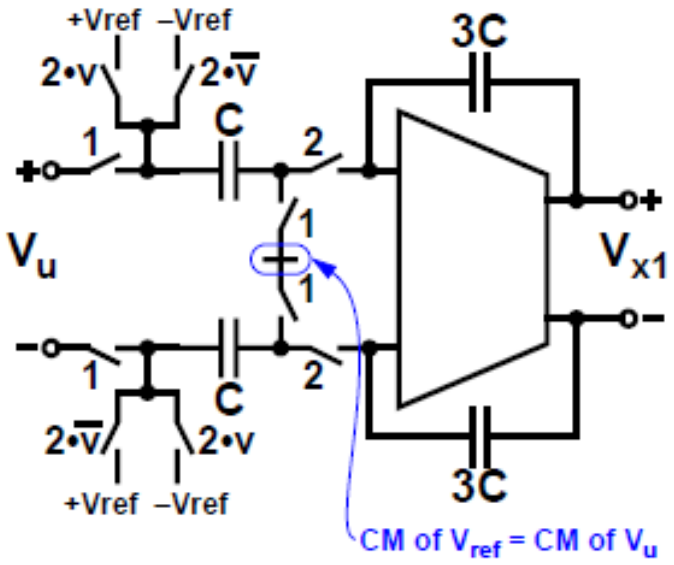
Scaled MOD2

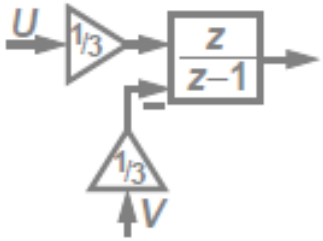
- **Take $\|x_1\|_\infty=3$ and $\|x_2\|_\infty=9$**
  - **The first integrator should not saturate**
  - **The second integrator will not saturate for DC inputs up to –3 dBFS and possibly as high as –1 dBFS.**
- **Our scaled version of MOD2 is then**



First Integrator (INT1)

- **Share Input and Reference Caps**





- **What is the optimal value for C ?**

Obtaining the Coefficients

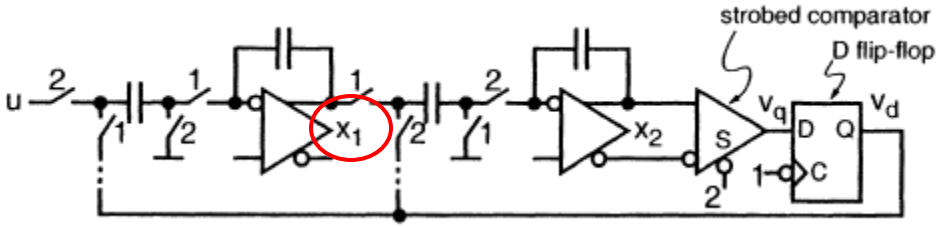
```
H = synthesizeNTF(2,500,0,2);
form = 'CIFB';
[a,g,b,c] = realizeNTF(H,form);
b(2:end) = 0;
ABCD = stuffABCD(a,g,b,c,form);
[ABCDs umax] = scaleABCD(ABCD);
[a,g,b,c] = mapABCD(ABCDs,form);
```

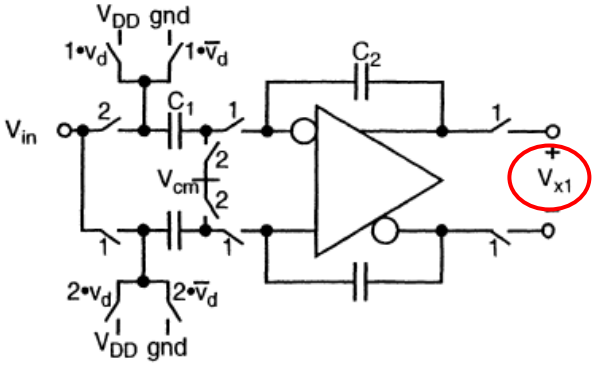
Voltage Scaling from the Toolbox

- **Translation of toolbox block diagram to a practical circuit.**
  - **Toolbox assumes the input of a single-bit modulator ranges from -1 to +1**
  - **The default DRS is also such that the integrator states occupy the [-1,1] range**
  - **The toolbox quantizer LSB size is 2 units**
- **However, in analog circuits the range must have physical units and match the voltage limits set by the technology**
- **Example:**
  - **Lets say the FS input is 3V, whereby the toolbox value is 2**
  - **Lets assume that the amplifier supports a diff swing of 2Vpp (same as the toolbox)**

Voltage Scaling Example

- **Example:**
  - **Lets say the FS input is 3V, whereby the toolbox value is 2**
  - **Lets assume that the amplifier supports a diff swing of 2Vpp (same as the toolbox)**





- **Relationship between the circuit variables and the state variables are**

$$x_1 = \frac{v_{x1}}{1\ \text{V}},$$

$$u = \frac{v_{in} - 1.5\ \text{V}}{1.5\ \text{V}}$$

$$v = 2v_d - 1$$

Voltage Scaling Example contd.

- **The difference equation we need to implement is**

$$x_1(n+1) = x_1(n) + b_1 u(n) - a_1 v(n)$$

where $a_1 = b_1 = 1/4$. The circuit equation becomes

$$v_{x1}(n+1) = v_{x1}(n) + \frac{b_1[v_{in}(n) - 1.5\ \text{V}]}{1.5} - a_1[2v_d(n) - 1] \cdot 1\ \text{V}$$

$$= v_{x1}(n) + \frac{v_{in}(n)}{6} - 0.5\ \text{V} \cdot v_d(n)$$

The equation from the circuit implementation

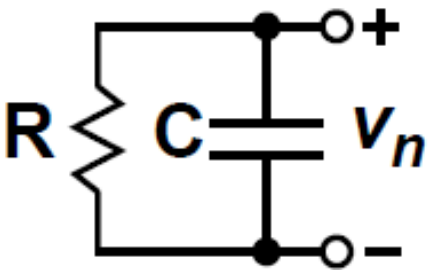
$$v_{x1}(n+1) = v_{x1}(n) + \frac{2C_1}{C_2} v_{in}(n) - \frac{2C_1}{C_2} V_{DD} v_d(n)$$

The capacitor ratio of the input and integrating capacitors needs to be

$$C_1/C_2 = 1/12.$$

With V_{DD} = 3 V , the above ratio also gives the correct coefficient for v_d.

Thermal - kT/C - Noise



- ***From ECE 614 Noise Analysis:***

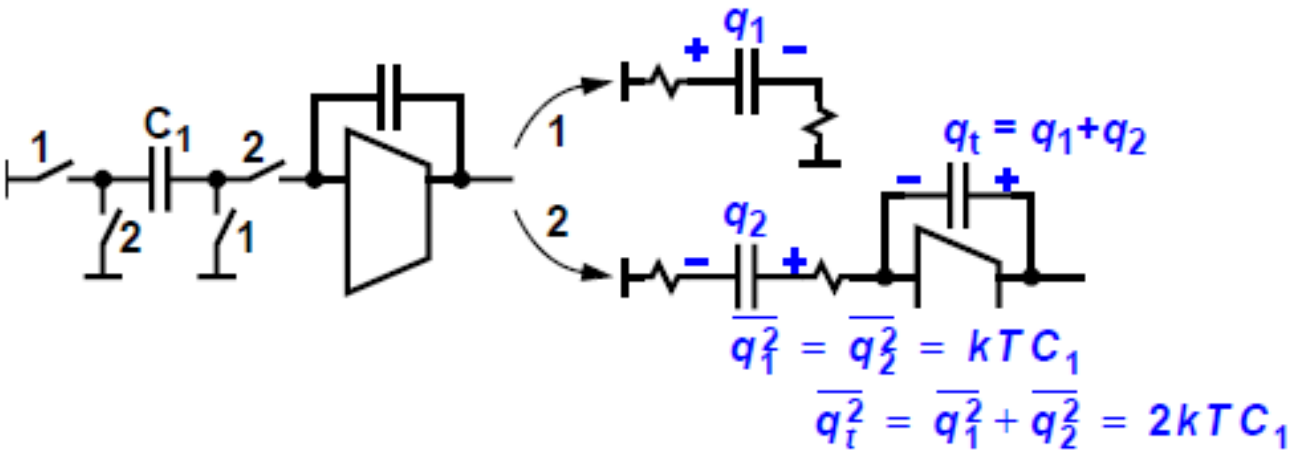
Regardless of the value of *R*, the mean square value of the voltage on *C* is

$$\overline{v_n^2} = \frac{kT}{C}$$

where *k* = 1.38 ×10–23 J/K is *Boltzmann's constant* and *T* is the temperature in Kelvin

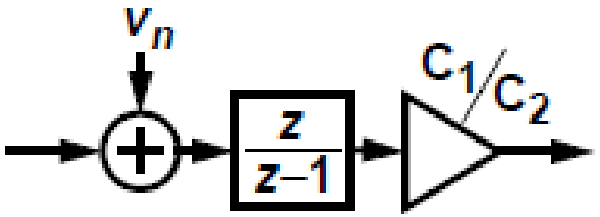
Noise in SC Integrator

- **Each charge/discharge operation has a random component**
  - **The amplifier plays a role during phase 2, but lets assume that the noise in both phases is just kT/C.**
- **For a given cap, these random components are essentially uncorrelated, so the noise is white**



Noise in SC Integrator contd.

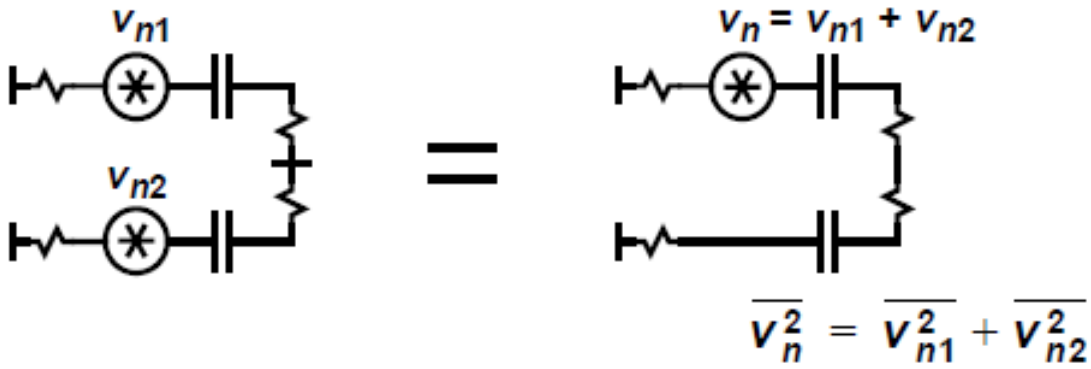
- **This noise charge is equivalent to a noise voltage with ms value $v_n^2=2kT/C_1$ added to the input of the integrator:**



- **This noise power is spread uniformly over all frequencies from 0 to $f_s/2$**

- **The power in the signal band [0, f_B] is v_n^2/OSR**

Differential Noise



- **Twice as many switched caps**

⇒ twice as much noise power

- **The input-referred noise power in our differential integrator is**
- **$V_n^2 = 4kT/C_1$**

INT1 Cap Sizes

For SNR = 100 dB @ –3-dBFS input

- The signal power is

$$\overline{v_s^2} = \underbrace{\frac{1}{2}}_{-3\ \text{dBFS}} \bullet \frac{(1\ \text{V})^2}{2} = 0.25\ \text{V}^2$$

$\frac{A^2}{2}$

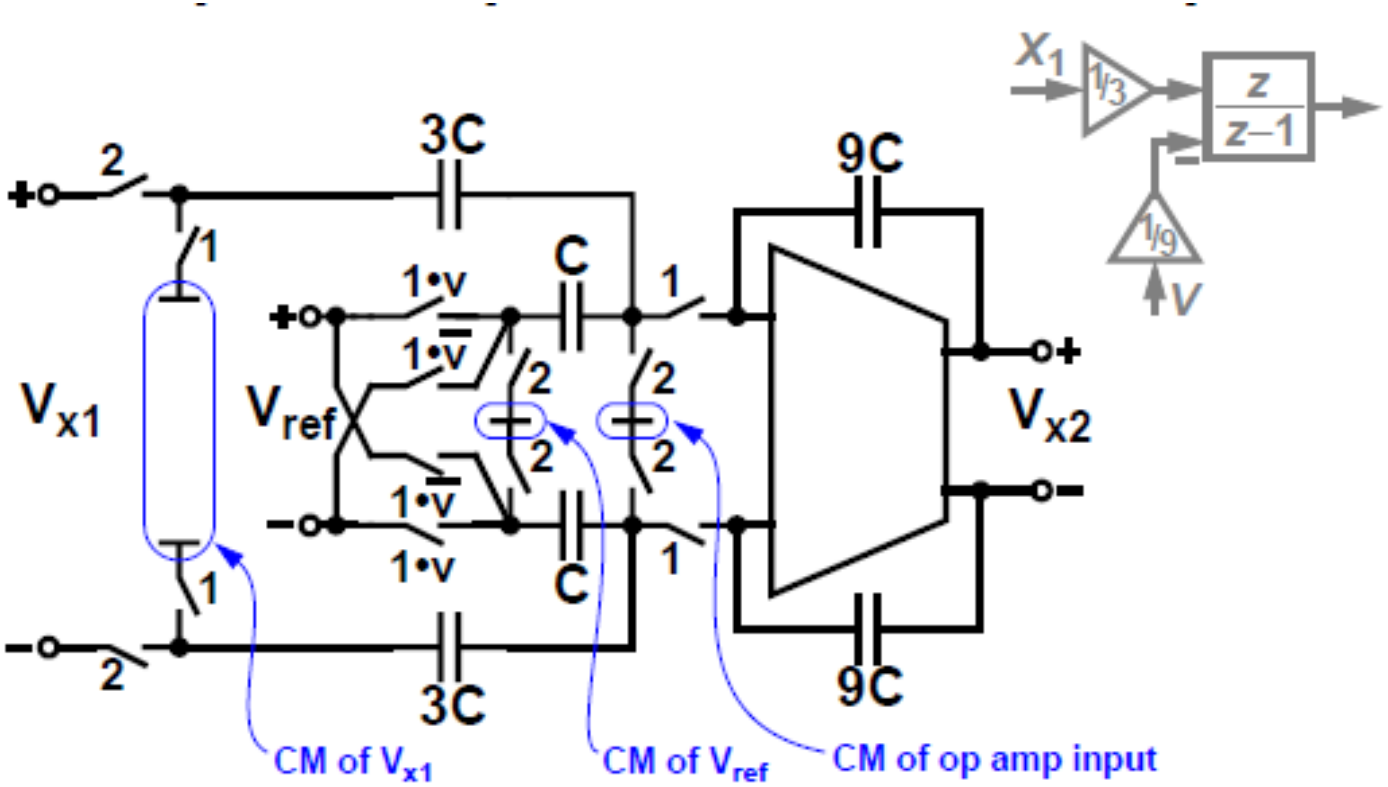
- Therefore we want $\overline{v_{n,\ \text{in-band}}^2} = 0.25 \times 10^{-10}\ \text{V}^2$
- Since $\overline{v_{n,\ \text{in-band}}^2} = \overline{v_n^2}/OSR$

$$C_1 = \frac{4kT}{\overline{v_n^2}} = 1.33\ \text{pF}$$

- If we want 10 dB more SNR, we need 10x caps

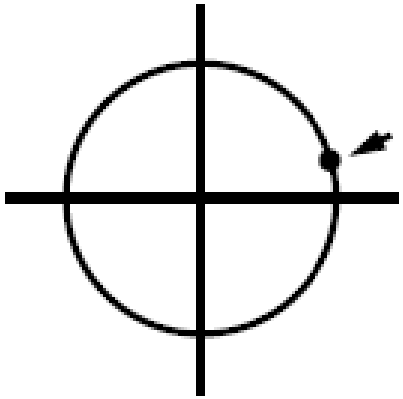
Second Integrator (INT2)

- **Separate Input and Feedback Caps**



2nd Integrator Cap Sizes

- In-band noise of second integrator is greatly attenuated



$$\omega_B = \frac{\pi}{OSR}$$

INT1 gain @ pb edge: $A = \frac{1/3}{\omega_B} = \frac{OSR}{3\pi}$

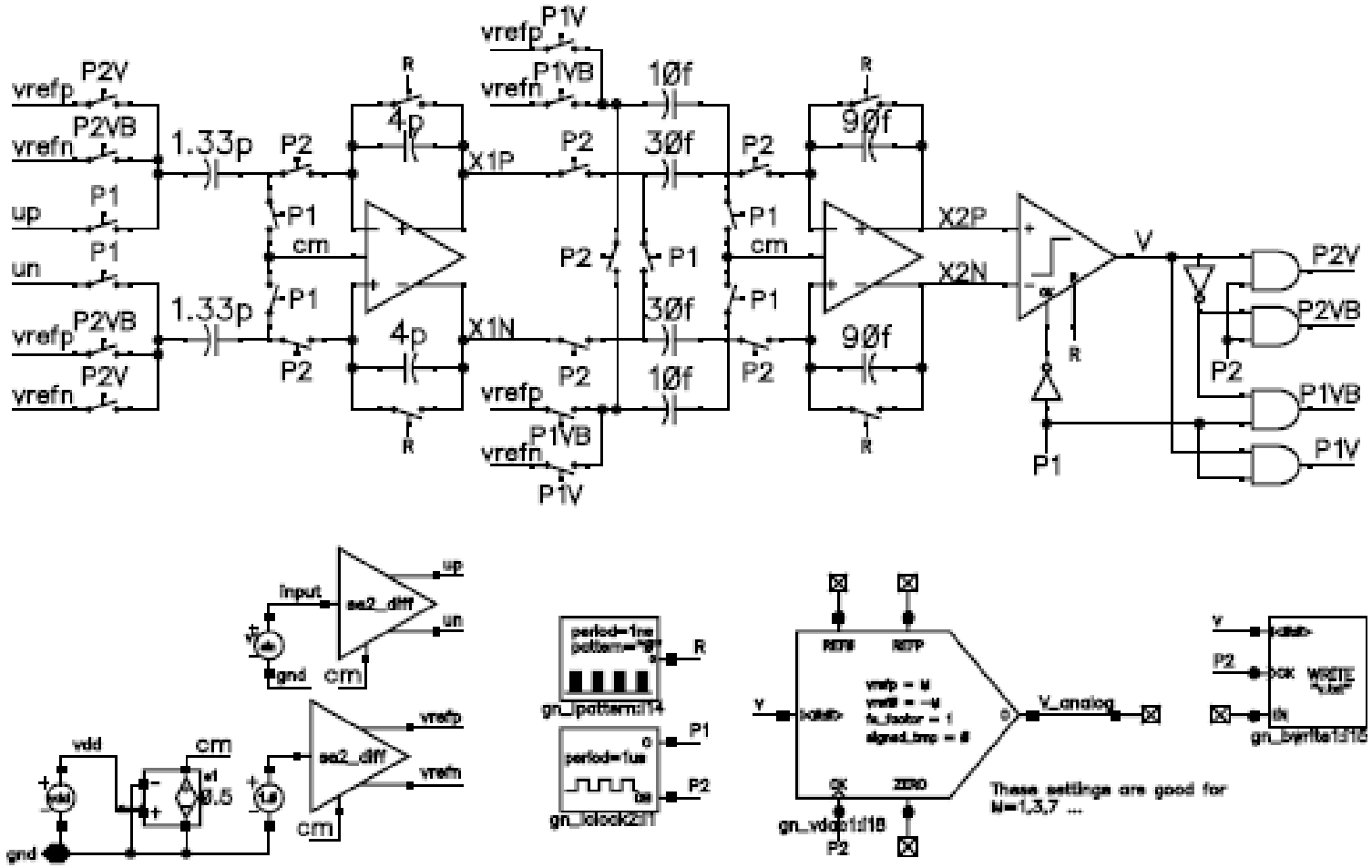
INT2 noise attenuation: $> OSR \cdot A^2 \approx 10^6$

$\Rightarrow$ Capacitor sizes not dictated by thermal noise

- Charge injection errors and desired ratio accuracy set absolute size

  A reasonable size for a small cap is currently ~10 fF.

Behavioral Schematic for SwitCap MOD2

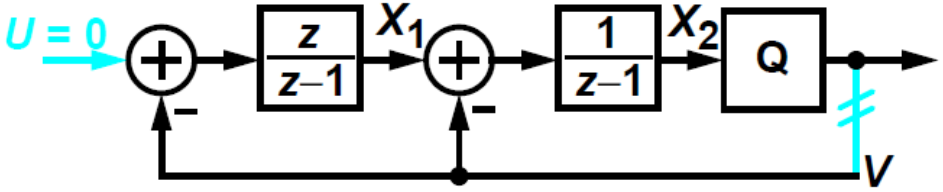


Verification

- **Open-loop Verification**
- **Loop filter**
- **Comparator**
  - **In case of a single-bit integrator only polarity and timing can go wrong**
- **Closed-loop Verification**
  - **Swing of internal states**
  - **Spectrum: SQNR, STF gain**
  - **Sensitivity, start-up, overload recovery,…**

Loop-Filter Check - Theory

- **Open-loop the feedback loop, set u=0, and drive an impulse through the feedback path**



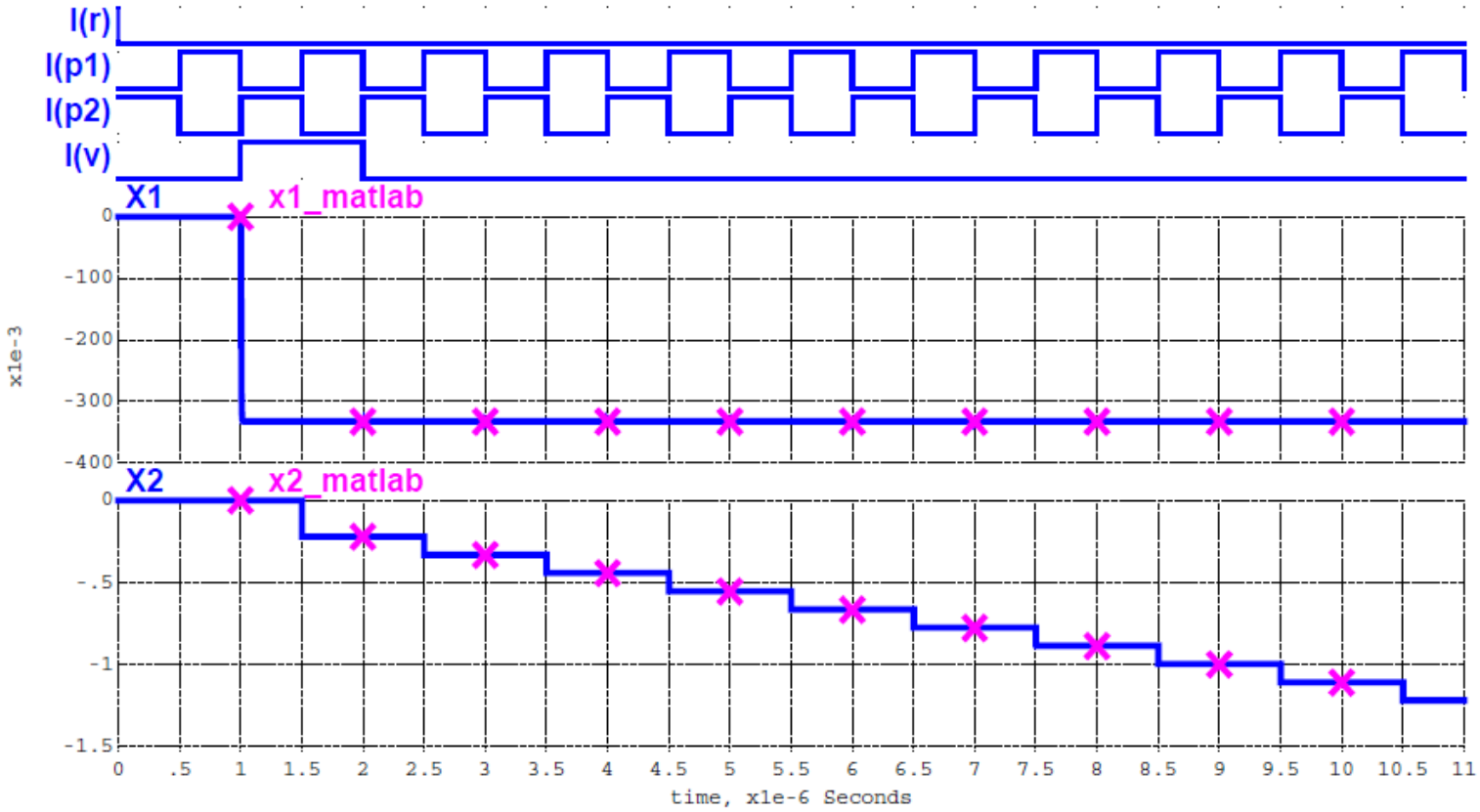
$$X_2 = \frac{-1}{z-1}\left(1 + \frac{z}{z-1}\right)Y$$

$$\therefore y(n) = \{1, 0, 0, \ldots\} \Rightarrow x_2(n) = \{-2, -3, -4, \ldots\}$$

- **If y=x2 is as predicted then the open-loop response, -*L*(*z*), is correct**
  => The correct NTF will be realized by the circuit

Loop-Filter Check - Simulation

- **But….**

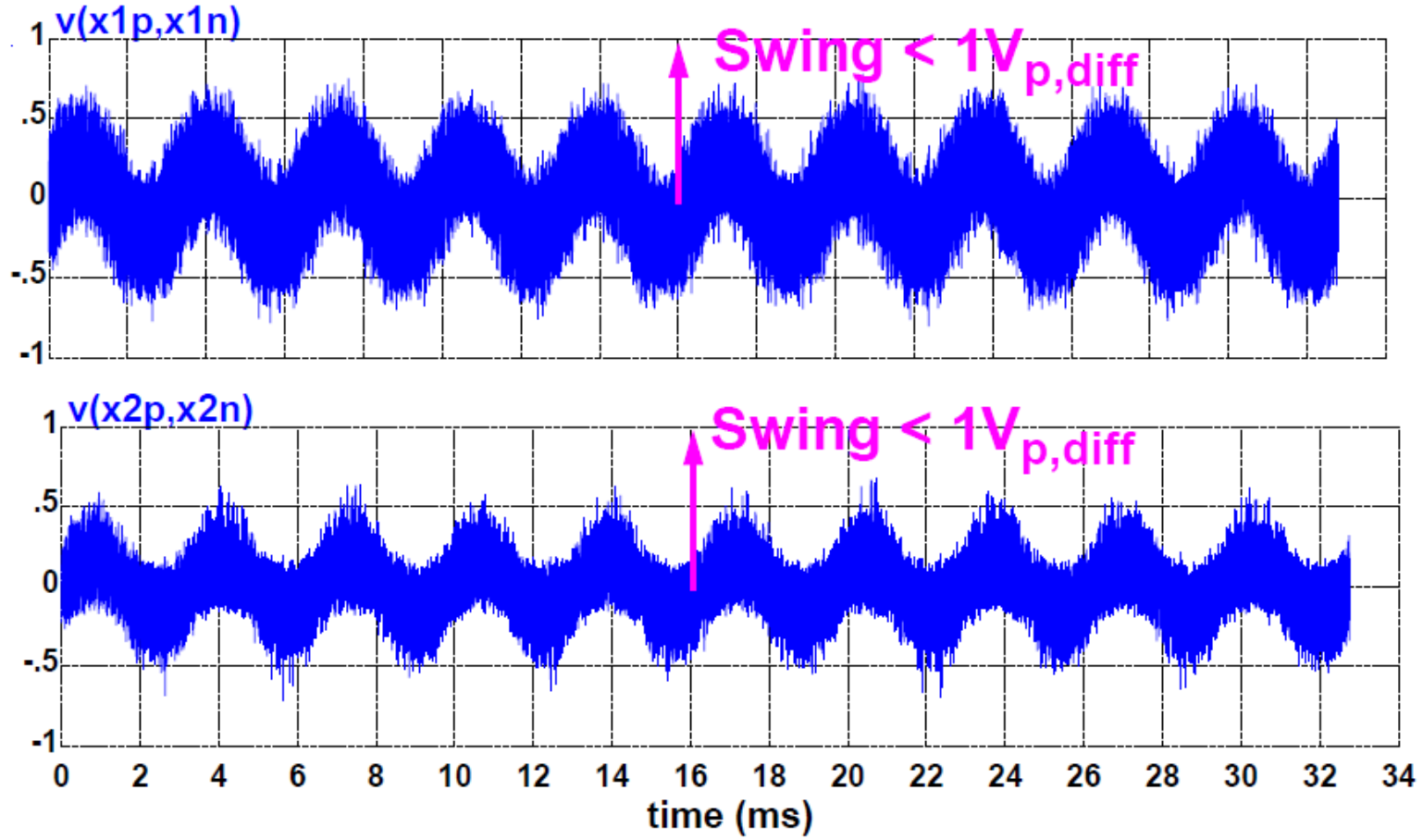


Loop-Filter Check - Specifics

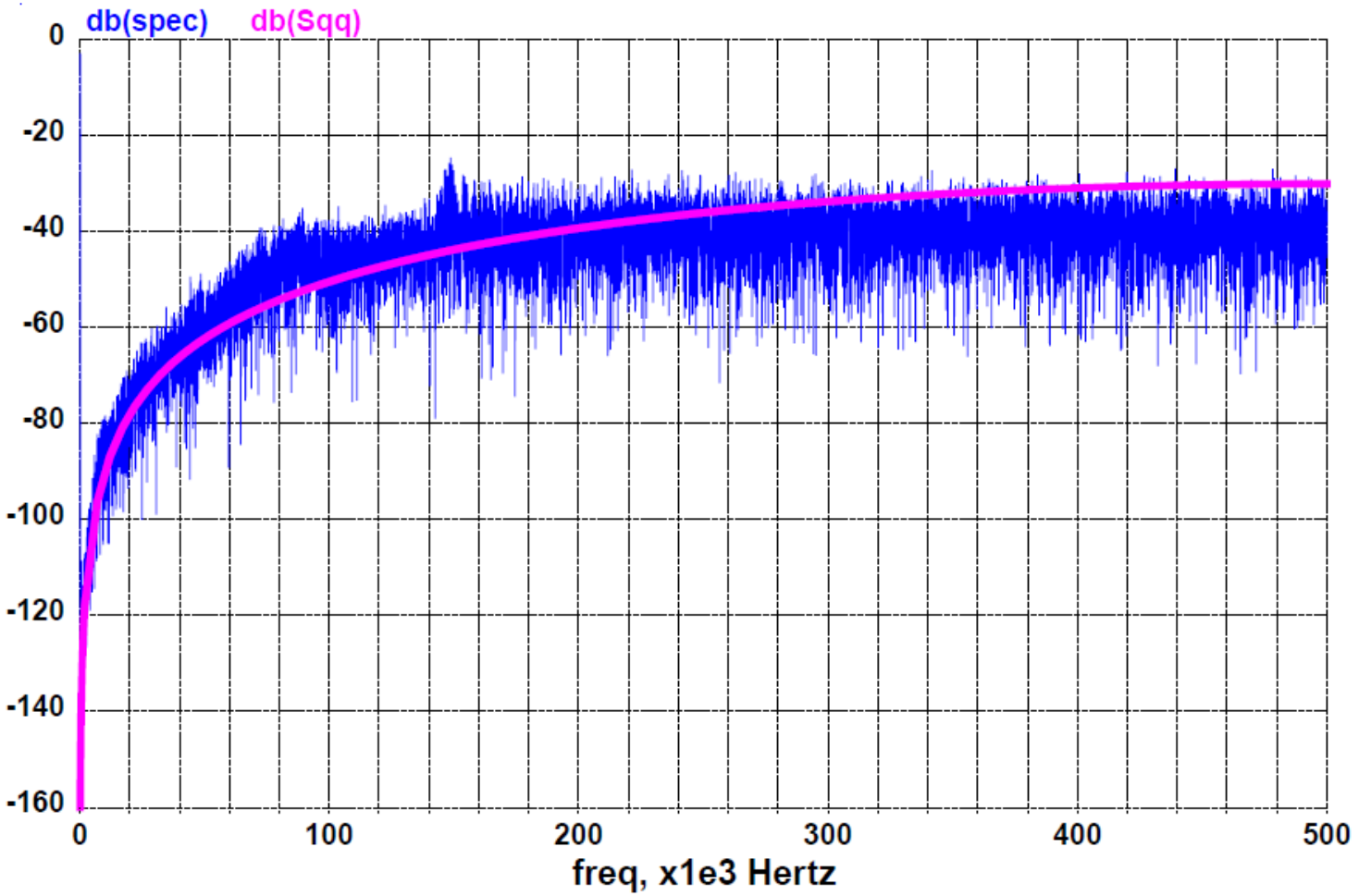
- **An impulse response is {1,0,0,0}, but a binary DAC can only output +/-1 , i.e. it can't produce a zero**
- ***Q*: So how can we determine the impulse response of the loop filter through simulation?**
- ***A*: Do two simulations: one with v={-1,-1,-1,….} and one with v={+1,-1,-1,…}.**
- **Then take the difference.**
- **According to linear superposition, the result is the response to v={2,0,0,…}, so divide by 2.**
  - **To keep the integrator states from growing too quickly, one could also use v={-1,-1,+1,-1,…} and then v={+1,-1,+1,-1,…}**

Simulated State Swings

- **-3-dBFS ~300-Hz sine wave**

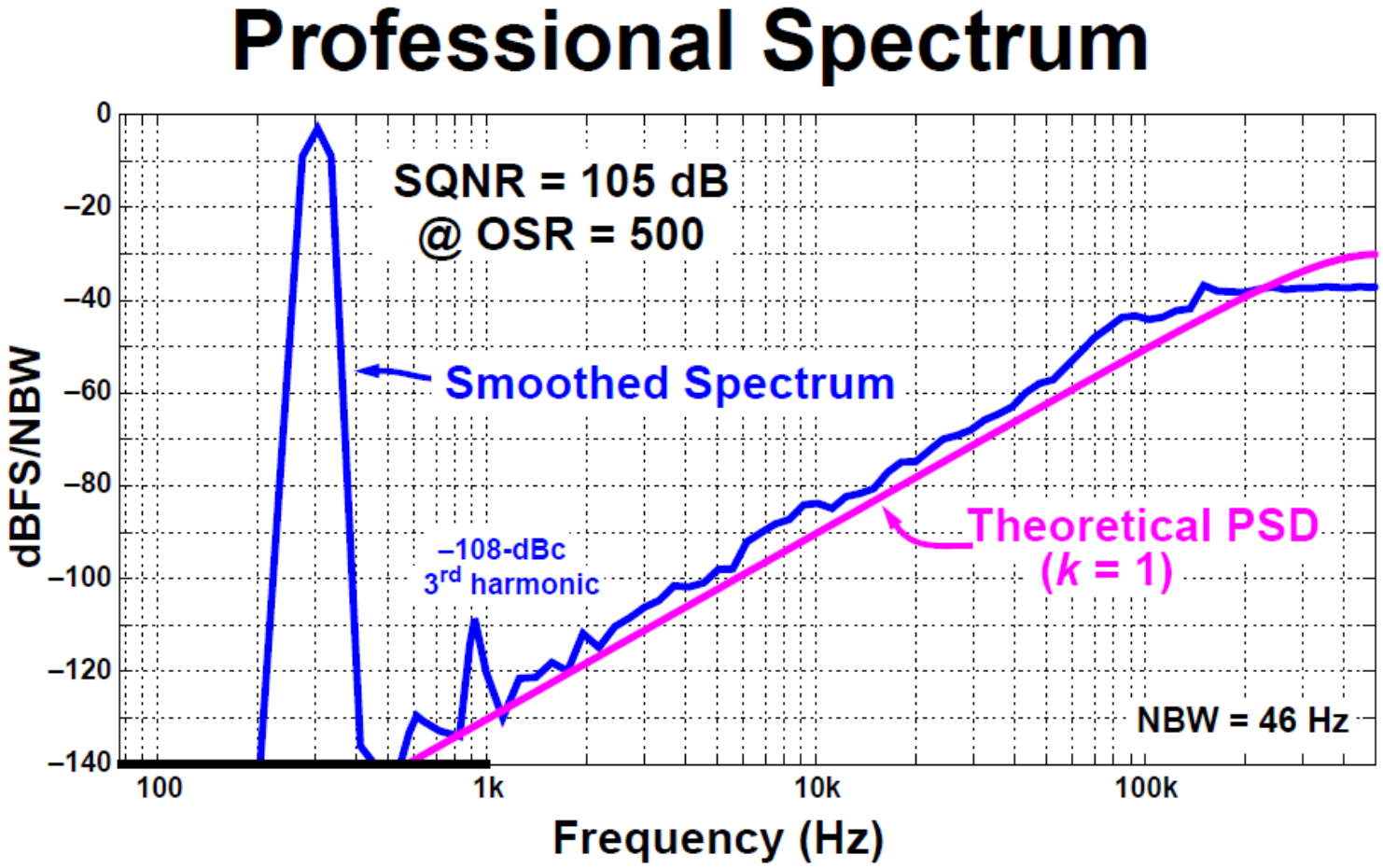


Rookie Spectrum



Professional Spectrum

- **SNDR dominated by -109-dBFS 3rd harmonic**

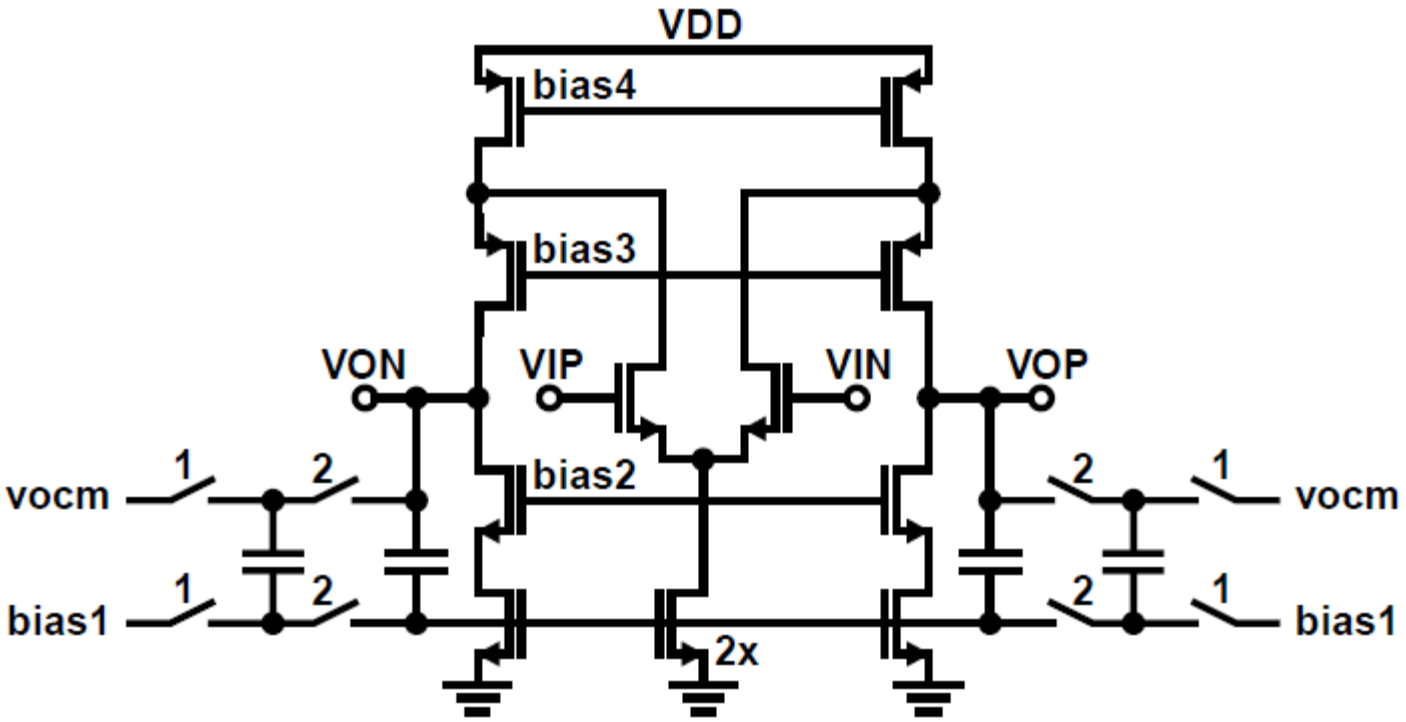


Implementation Summary

1. **Choose a viable SC topology and manually verify timing**
2. **Do coefficient quantization and dynamic-range scaling**
   - **You now have a set of capacitor ratios.**
   - **Verify operation: loop filter, timing, swing, spectrum.**
3. **Determine absolute capacitor sizes**
   - **Verify noise.**
4. **Determine op-amp specs and construct a transistor-level schematic**
   - **Verify everything.**
5. **Layout, fabricate, debug, publish/market!**

Building Block - Opamp

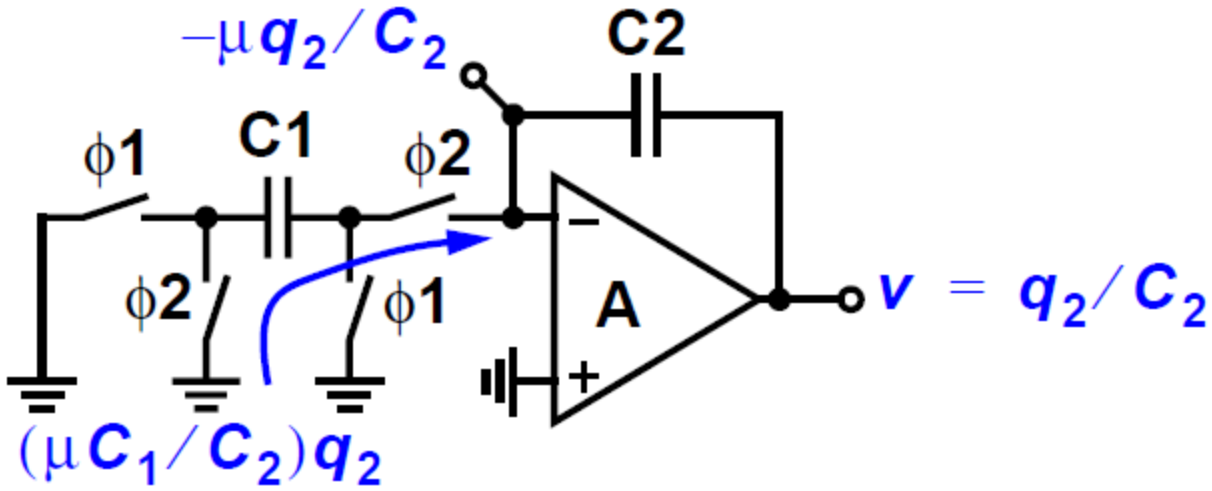
- **Folded-cascode op-amp with switched-capacitor common-mode feedback**



Effect of Finite Opamp Gain

Linear Theory

- Suppose that the amplifier has finite DC gain A. Define $\mu = 1/A$.
- To determine the effect on the integrator pole, let's look at our SC integrator with zero input:



Effect of Finite Opamp Gain

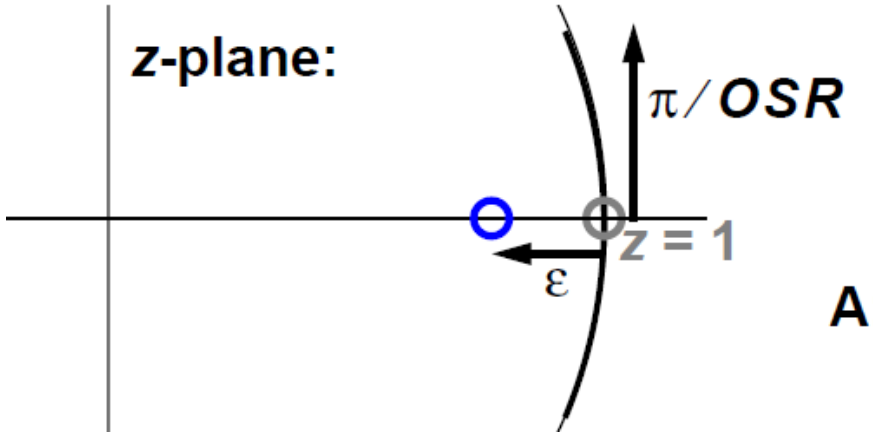
- A fraction of q_2 leaks away each clock cycle:

$$q_2(n+1) = (1-\varepsilon)q_2(n),$$

where $\varepsilon = \mu C_1/C_2$

- Thus, the integrator is lossy, with a pole at $z = 1-\varepsilon$

Q: How big can ε get before the effect becomes significant?



A: $\varepsilon \approx \pi/OSR$

Opamp Gain Requirement

Linear Theory

- According to the linear theory, finite op amp gain should not degrade the noise significantly as long as

$$A > (C_1/C_2)(OSR/\pi)$$

- For our implementation of MOD2, in which $C_1/C_2 = 1/4$ and $OSR = 500$, this leads to

$$A > 40 = 32 \text{ dB},$$

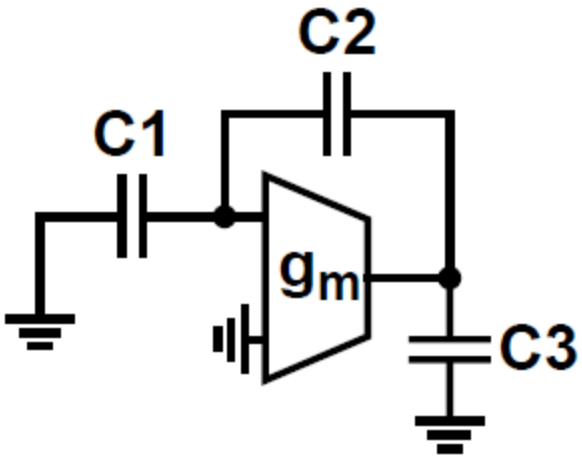
which is quite a lax requirement!

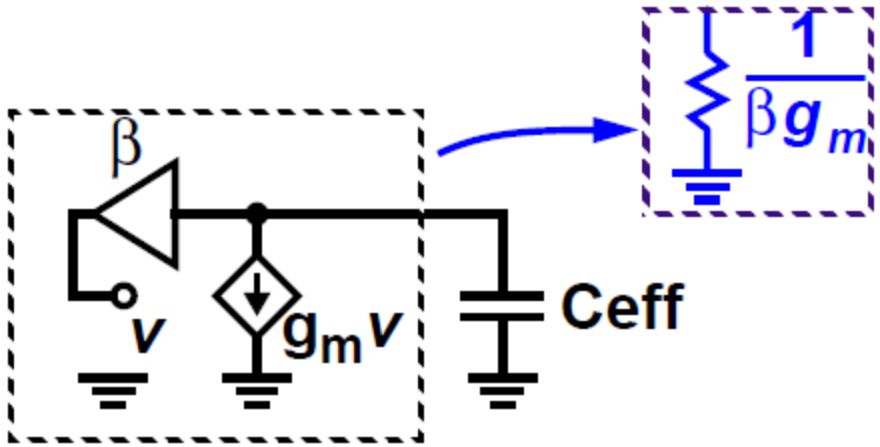
- As OSR is decreased, the gain requirement goes down

Opamp Transconductance

Settling time

- Model the op amp as a simple g_m:





$$\beta = C_2/(C_1 + C_2)$$

$$C_{eff} = C_3 + C_1C_2/(C_1 + C_2)$$

- This is a single-time-constant-circuit with $\tau = C_{eff}/(\beta g_m)$

Opamp Settling Requirements

- If g_m is linear, incomplete settling has the same effect as a coefficient error and thus g_m can be very low
- In practice, the g_m is not linear and we need to ensure nearly complete settling
- As a worst case scenario, let's require transients to settle to 1 part in 10^5

  This should be more than enough for –100 dBc distortion.

Opamp Settling Requirements contd.

- If linear settling is allocated 1/4 of a clock period, we want $\exp\left(-\frac{T/4}{\tau}\right) = 10^{-5}$, or $\tau = \frac{T}{4\ln 10^5} = 20$ ns

  and thus $g_m = \frac{C_{eff}}{\beta\tau} = \frac{C_{eff}}{\beta} 4 f_s \ln 10^5$

- For INT1 of our MOD2:

$$C_{eff} = 0.5\left(\frac{4\text{p} \cdot 1.33\text{p}}{4\text{p} + 1.33\text{p}} + 30\text{f}\right) = 0.5 \text{ pF}^*$$

$$\beta = 3/4$$

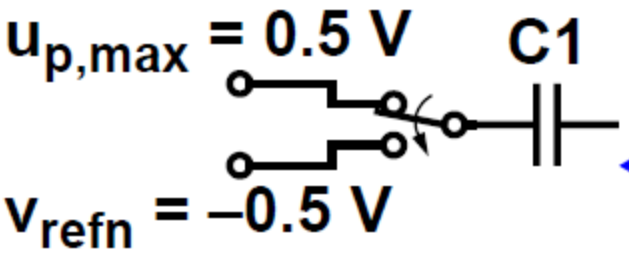
$$f_s = 1 \text{ MHz}$$

$$\Rightarrow \quad g_m = 30 \ \mu\text{A/V}$$

*. 0.5 comes from the single-ended to differential translation.

Opamp Slewing

- The maximum charge transferred through C1 is

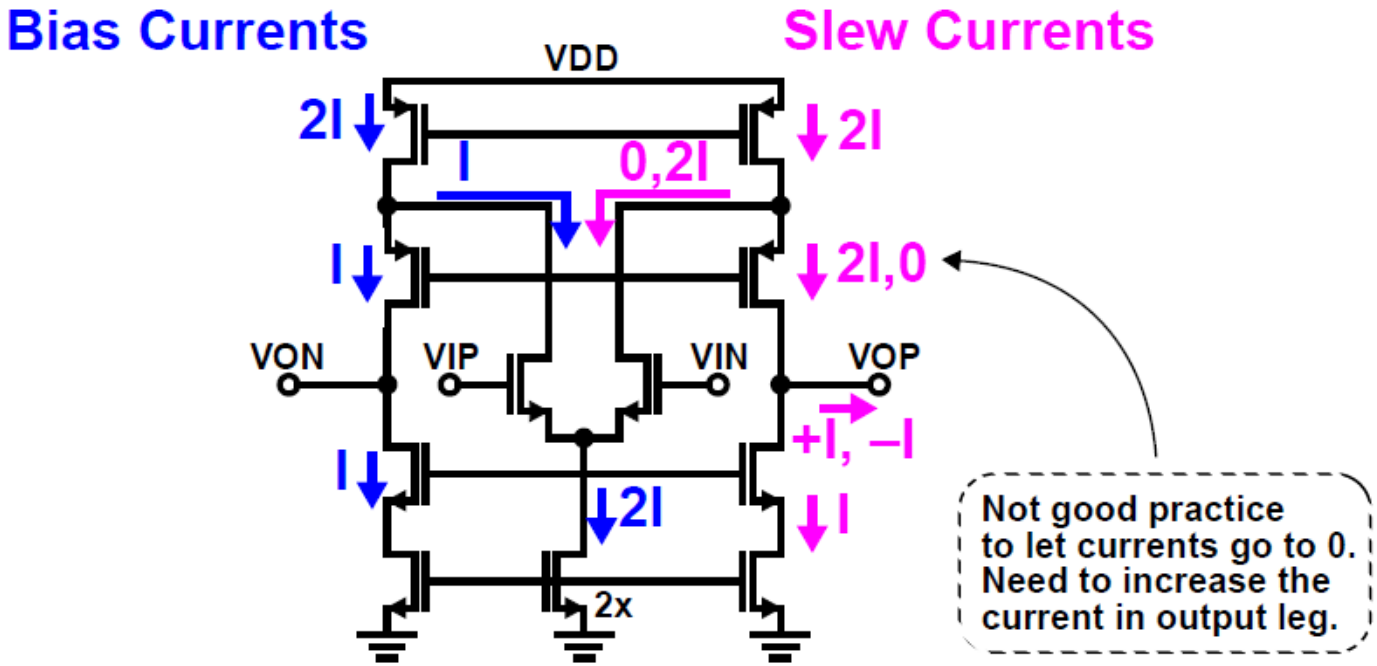


$$\leftarrow q_{max} = C_1 \cdot 1V = 1.33\ pC$$

- If we require the slew current to be enough to transfer q_{max} in 1/4 of a clock period, then

$$I_{slew} = \frac{q_{max}}{T/4} \approx 5\ \mu A$$

Opamp Design – Bias Current



- **Slew constraint dictates I>5uA**