Project 1

ECE 615 – Mixed Signal IC Design

1 Problem Statement

Design of an Audio ADC: This project involves *realistic* design process for a $\triangle\Sigma$ ADC intended for audio recording devices. The design is to be implemented using a 180-nm mixed-mode CMOS process with a $V_{DD} = 1.8\,V$ supply voltage. The target specifications for the single-loop multi-bit audio $\triangle\Sigma$ modulator are as follows:

Table 1: $\triangle\Sigma$ ADC design specifications.

Parameter	Specified Value
Supply voltage, V_{DD}	1.8 V
Input signal bandwidth (f_B)	24 KHz
Resolution	$\geq$ 18 bits
Minimum Full-Scale (FS) input voltage	$0.6 \cdot V_{DD}$
Output sample rate (after decimation)	48 KHz
Maximum clock speed (f_{CLK})	12.5 MHz
Quantizer Range (fully-differential)	3 $V_{pp,diff}$

For details on noise calculations in audio conversion systems refer to [2].

2 $\triangle\Sigma$ Modulator Design

The following steps will guide you through the design and documentation process (Also refer to the design example in Chapter 9 of the textbook).

1. **Design Space Selection:** Determine the order (L), OSR, the number of quantizer levels (nLev) and the out-of-band gain (OBG). Provide reasons for your choice of design space (L, OSR, nLev, OBG) and argue why is your choice is optimal.

2. **NTF Design:** Determine a suitable NTF for your design. Plot the theoretical SNR, SNDR (in dB) vs amplitude (in dBFS), and mark peak-SNR, peak-SNDR, DR and SFDR on the plot (create a script).

3. **Loop-Filter Design:** Select a loop-filter architecture to implement the designed NTF.

   (a) The loop-filter is implemented using fully-differential discrete-time circuits. Knowing that the op-amps in the integrators are linear only for roughly 50% of the V_{DD}, limit the integrator output range to 1.5 $V_{pp,diff}$ (peak-to-peak differential). Apply Dynamic Range Scaling (DRS) to ensure that the loop-filter states are bounded and the op-amps don't saturate.

(b) Find the effective quantizer gain (k) using simulations and use this value to ensure that the STF is distortionless (e.g. $b_{N+1} = 1/k$). Also show that the modulator is stable with the quantizer gain variation (*Hint:* NTF root locus).

(c) Find the loop-filter coefficients and quantize them to a realizable capacitor ratio. To quantify the degradation due to coefficient quantization, compare the original NTF response with the final one. Neatly tabulate the original and final loop-filter coefficients, and the required capacitor ratios. Show relevant plots including $NTF(e^{j\omega})$ and $STF(e^{j\omega})$ with the selected loop-filter topology.

(d) Simulate the resulting modulator topology in MATLAB showing its performance. Show that the modulator states lie in the linear range when the input is within the stable input range.

3 Project Report

Submit your neatly typed report in a two-column IEEE transactions format [7]. Show neatly drawn schematics and block diagrams. You may download the Visio schematic symbols from the course website [8]. Provide relevant references in your report. Show the modulator overall ADC performance (peak SNR/SNDR, dynamic range, etc.) in a neatly tabulated manner along with the conclusion.

References

[1] A 24-bit, 192 kHz Multi-bit Audio ADC: CS5430 Datasheet, Wesbite, Cirrus Logic, 2008.

[2] Audio Conversion Systems Noise Calculations and Requirements, App. note AN263, Cirrus Logic, 2008.

[3] R. Schreier, J. Silva, J. Steensgaard, G. C. Temes,"Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits," *IEEE TCAS-I*, vol. 52, no. 11, pp. 2358-2368, Nov. 2005.

[4] K. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," *Designer's Guide Community* [Online].

[5] K. Kundert, "Device Noise Simulation of Delta-Sigma Modulators," *Designer's Guide Community* [Online].

[6] SIMSIDES, SIMulink-based SIgma-DElta Simulator ," University of Seville. Available [Online].

[7] IEEE Transactions Templates. Available [Online].

[8] Visio Schematic Symbols. Available [Online].