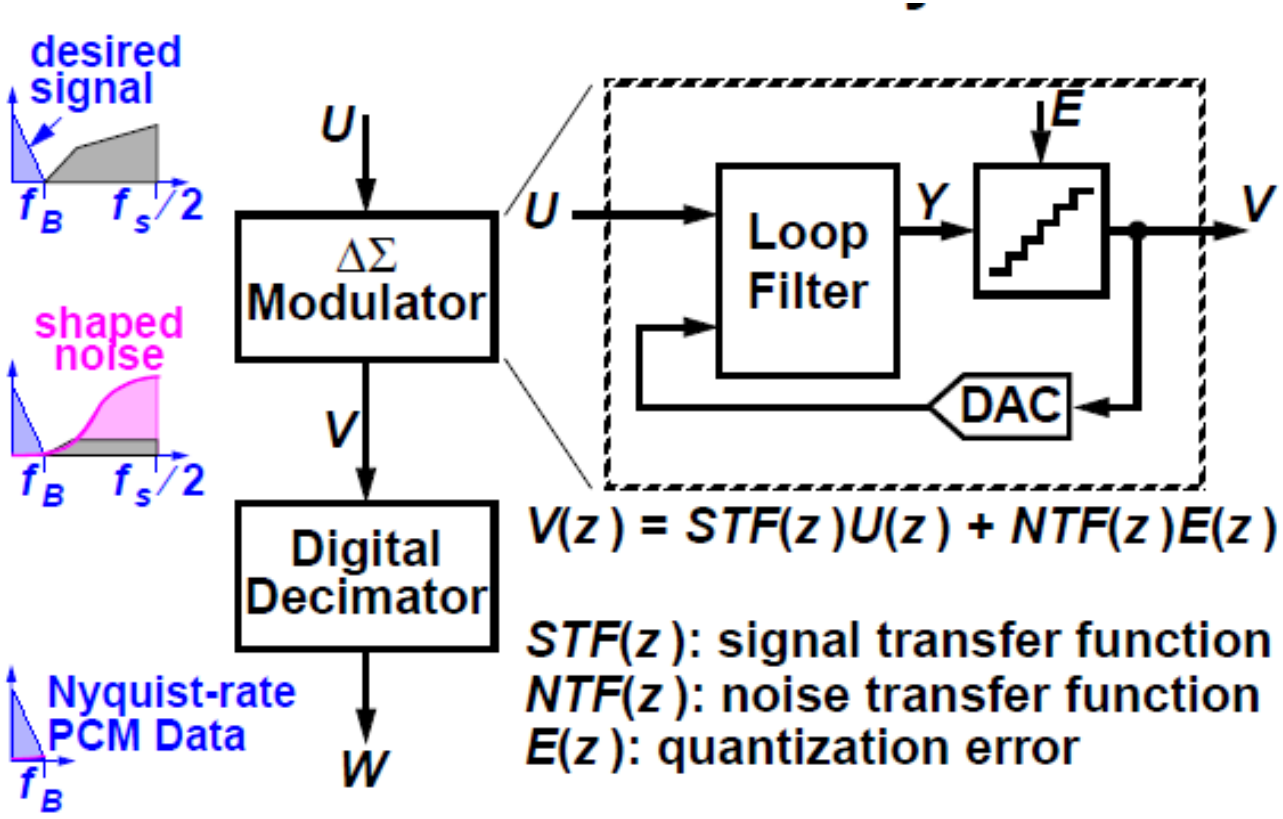
ECE615 Mixed-Signal IC Design

Discrete-Time $\Delta\Sigma$ Modulator Implementation

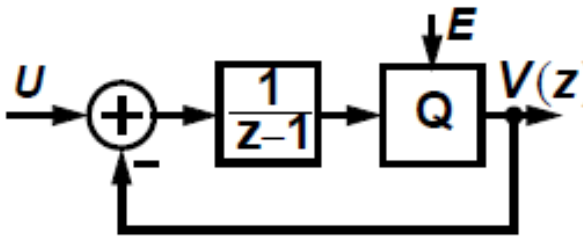
Vishal Saxena, Boise State University
(vishalsaxena@boisestate.edu)

Analog Mixed Signal IC Laboratory
Boise State University

Review: A ΔΣ ADC System



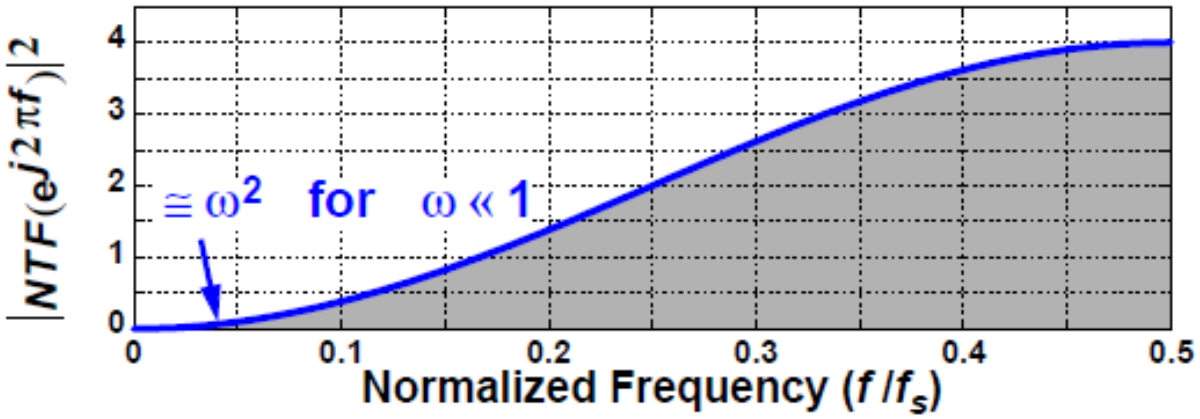
Review: MOD1



$$V(z) = NTF(z)E(z) + STF(z)U(z)$$

$$NTF(z) = (1 - z^{-1})$$

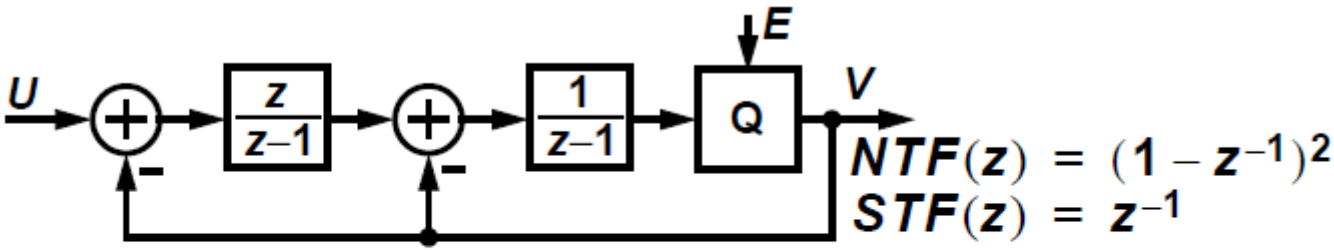
$$STF(z) = z^{-1}$$

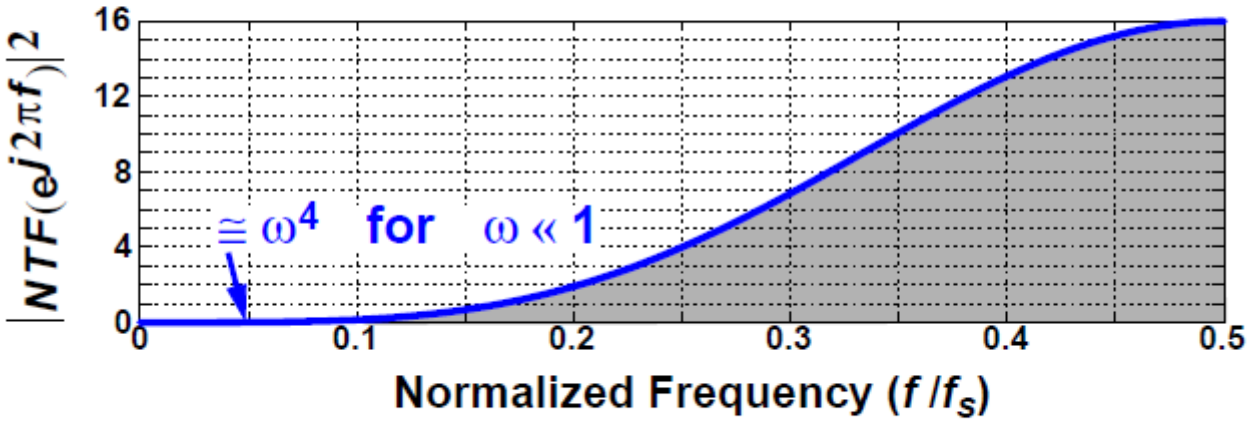


- **Doubling OSR improves SQNR by 9 dB**

  Peak SQNR $\approx$ dbp$(9 \cdot OSR^3/(2\pi^2))$; dbp$(x) \equiv 10\log_{10}(x)$

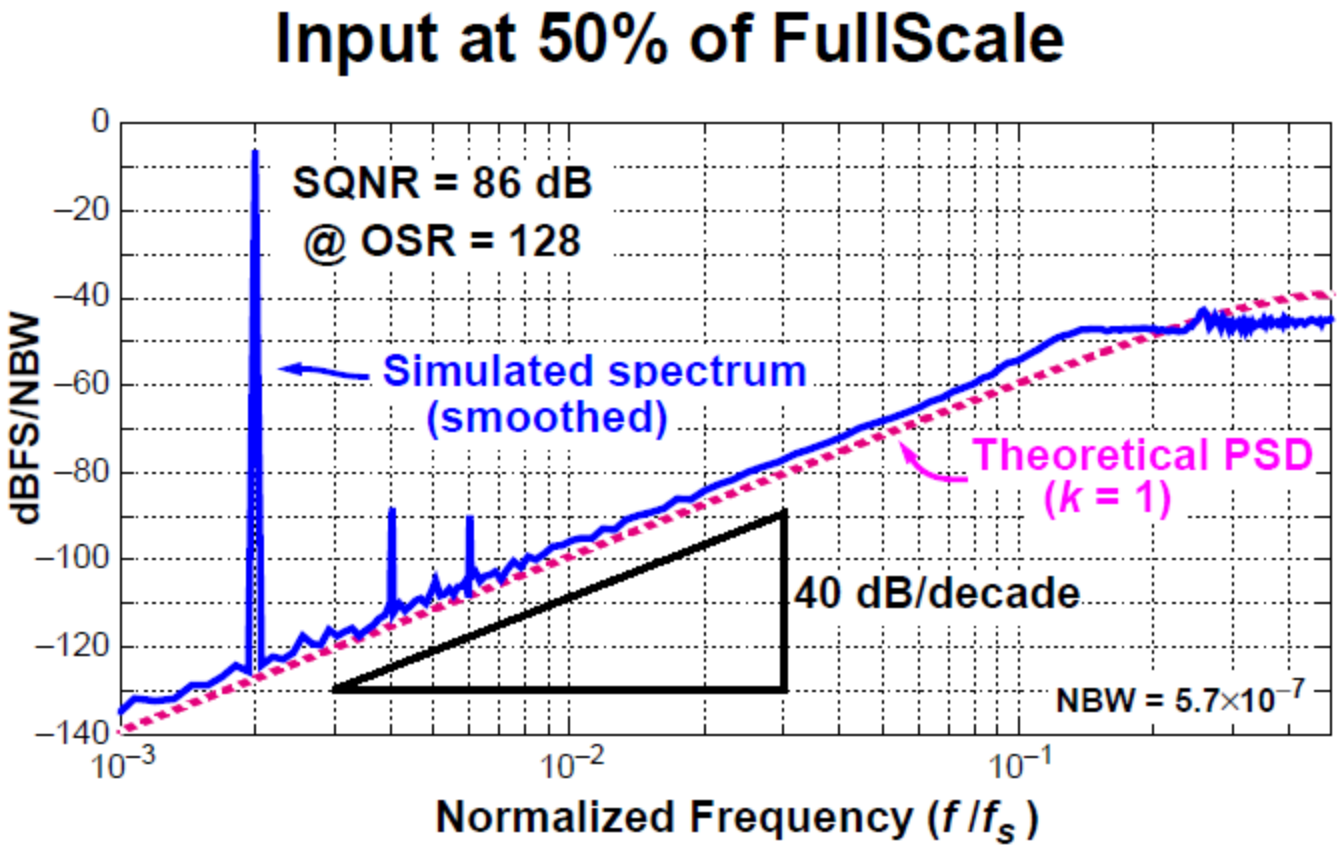
Review: MOD2





- **Doubling OSR improves SQNR by 15 dB**
  Peak SQNR ≈ dbp($(15 \cdot OSR^5)/(4\pi^4)$)

Review: Simulated MOD2 PSD



Example Design 1

• Clock at $fs = 1\ MHz$.

Assume BW = 1 kHz.

$\Rightarrow OSR = fs/(2 \cdot BW) = 500 \approx 29$

• MOD1: SQNR ≈ 9 dB/octave • 9 octaves = 81 dB

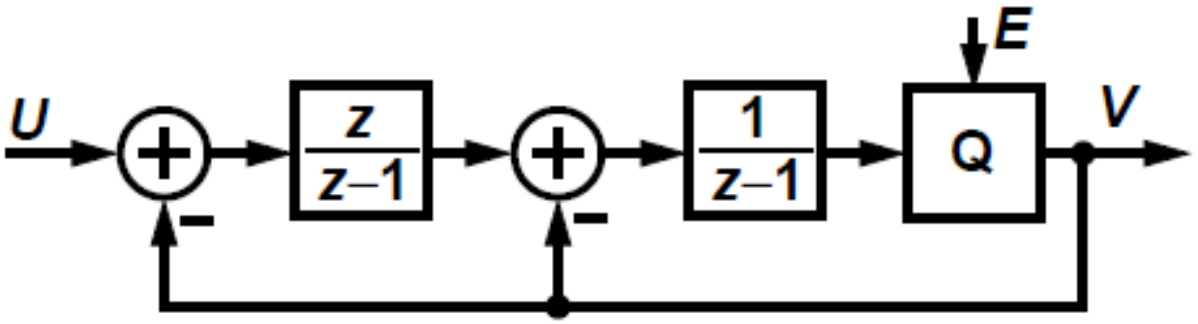
• MOD2: SQNR ≈ 15 dB/octave • 9 octaves =135 dB

Actually more like 120 dB.

• SQNR of MOD1 is not bad, but SQNR of MOD2 is awesome!

MOD2 is usually preferred over MOD1 because MOD2's quantization noise is more well-behaved.

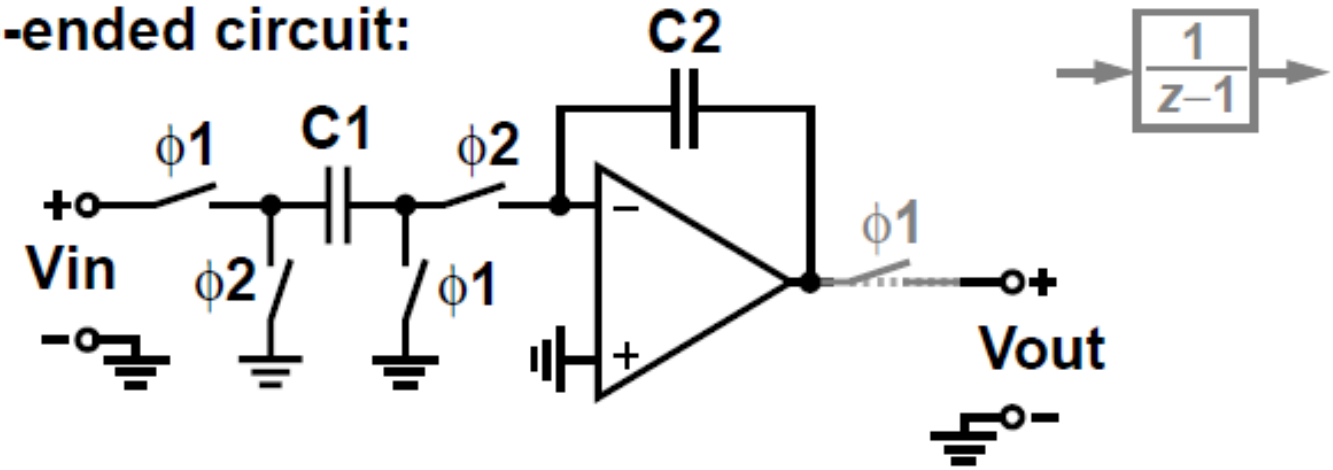
Block Diagram



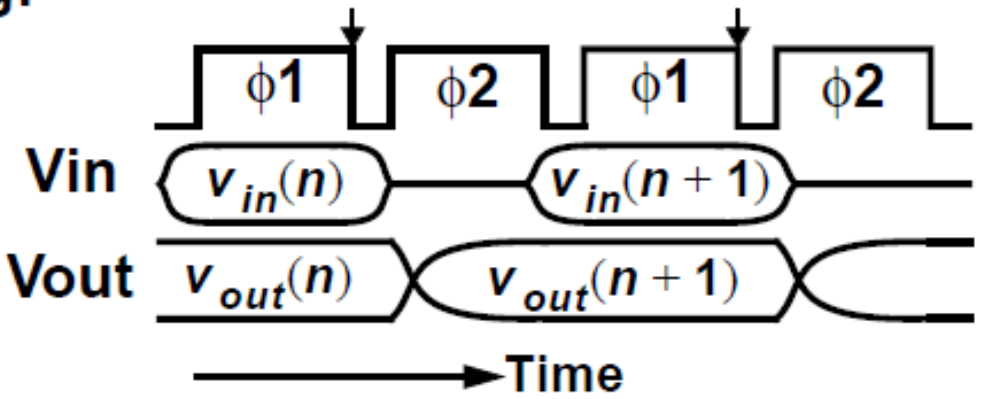
- **Summation blocks**
- **Delaying and non-delaying discrete-time**
- **integrators**
- **Quantizer (1-bit)**
- **Feedback DACs (1-bit)**
- **Decimation filter (not shown)**
  - **Digital and therefore “easy”**

Switched-Capacitor Integrator

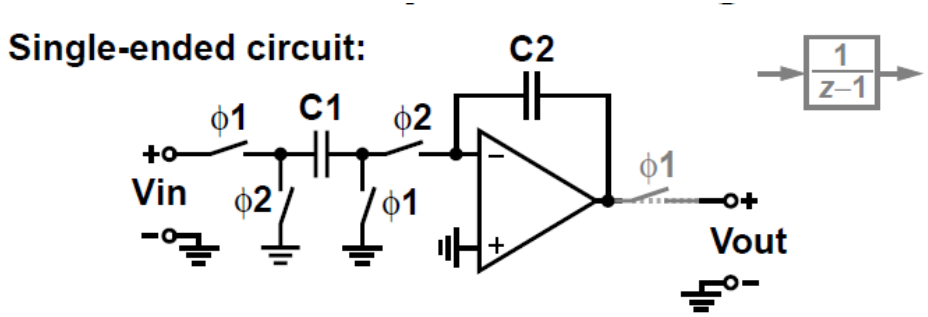
Single-ended circuit:

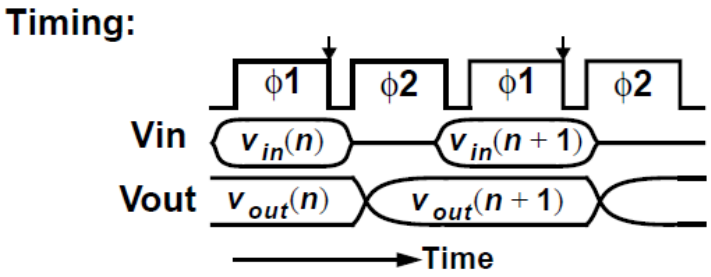


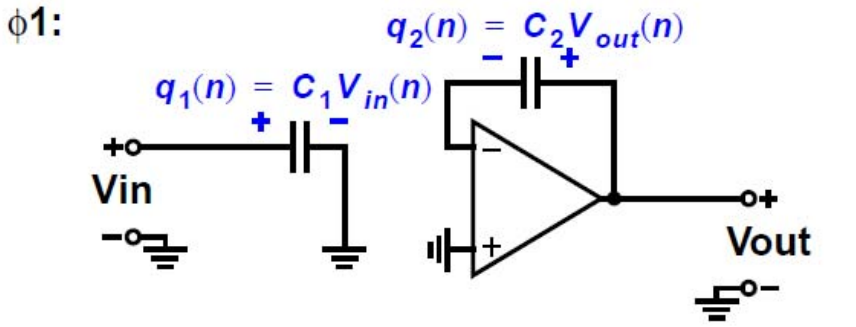
Timing:

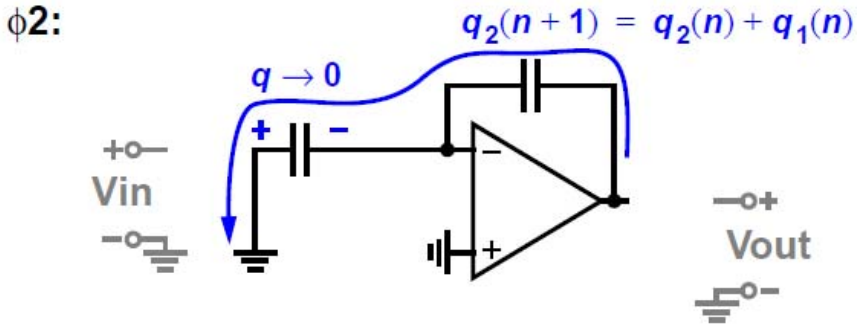


Switched-Capacitor Integrator contd.

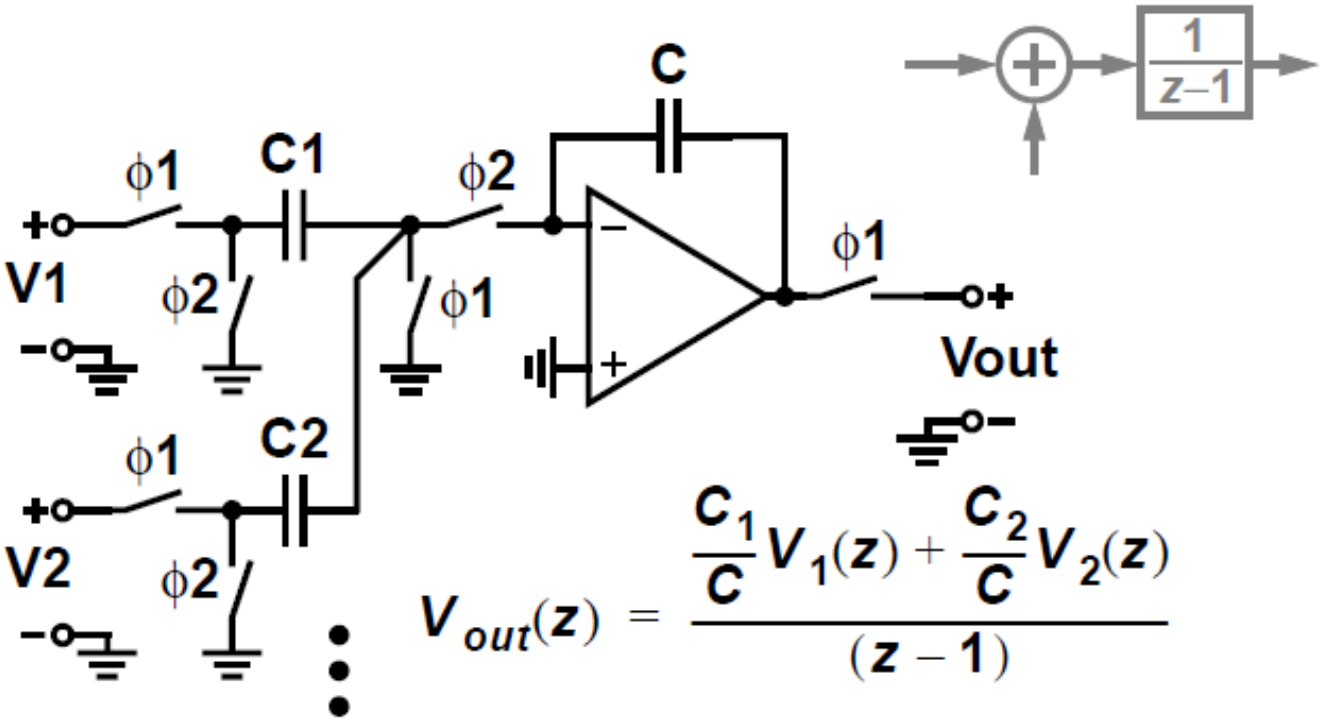






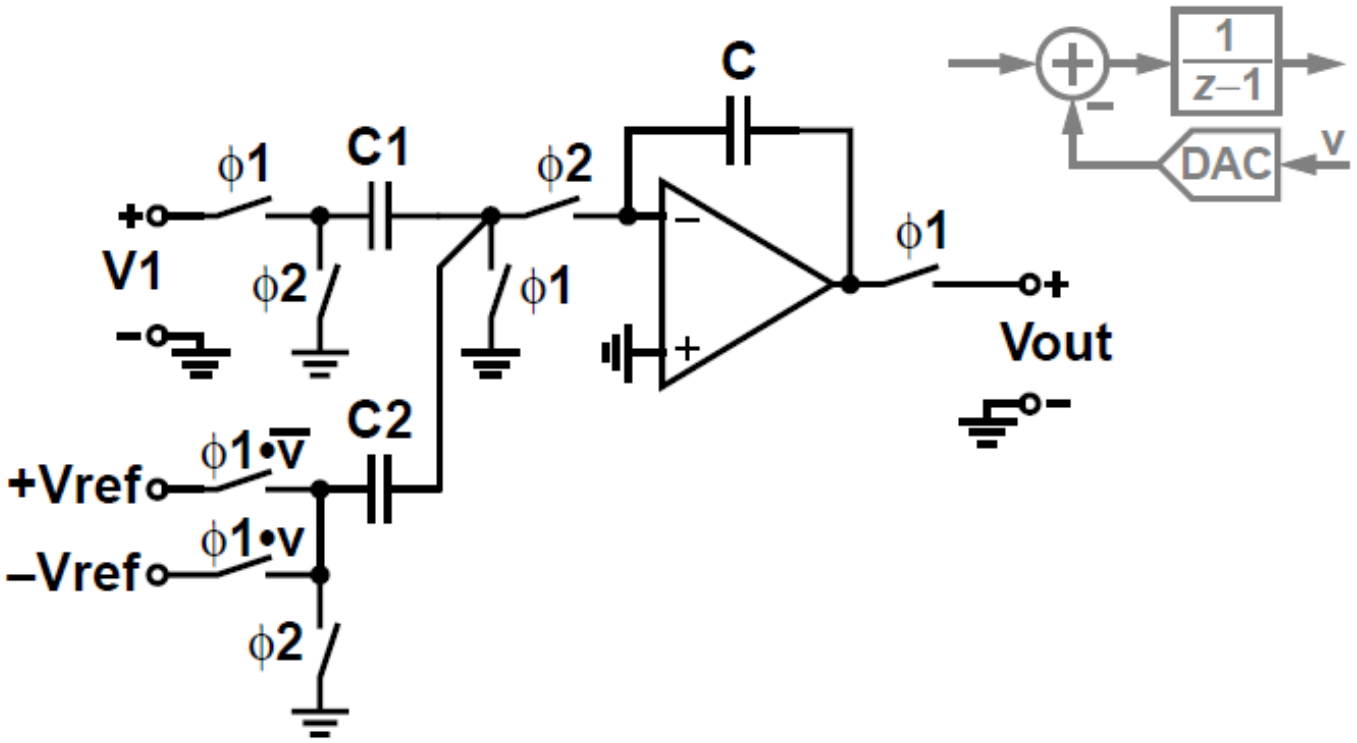


Summation and Integration

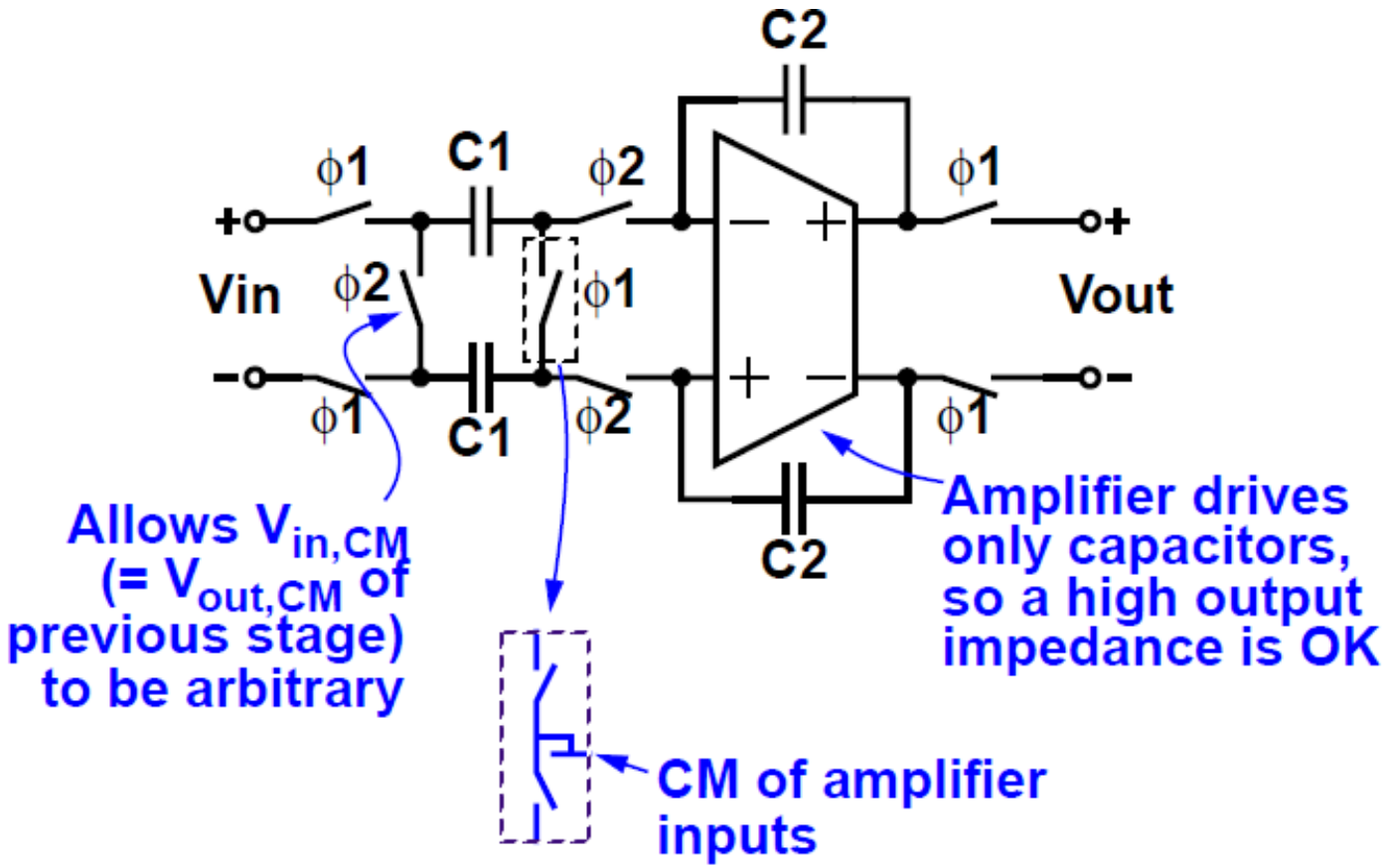


- **Adding an extra input branch accomplishes addition, with weighting**

1-bit DAC + Summation + Integration

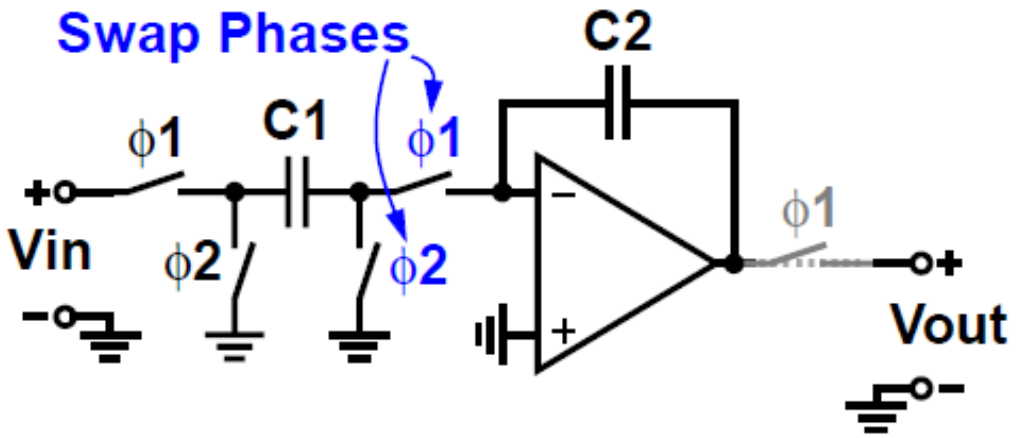


Fully-Differential Integrator

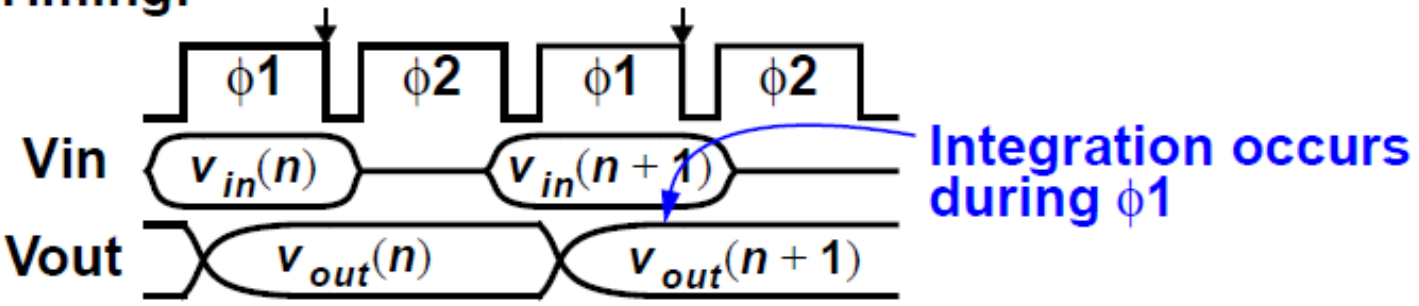


Non-Delaying Integrator

Single-ended circuit:

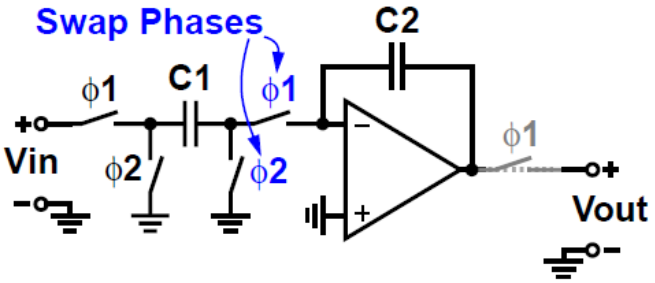


Timing:

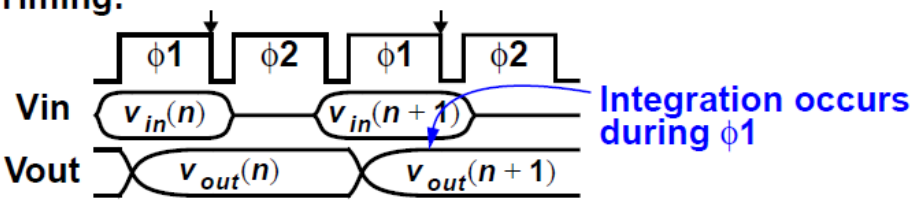


Non-Delaying Integrator contd.

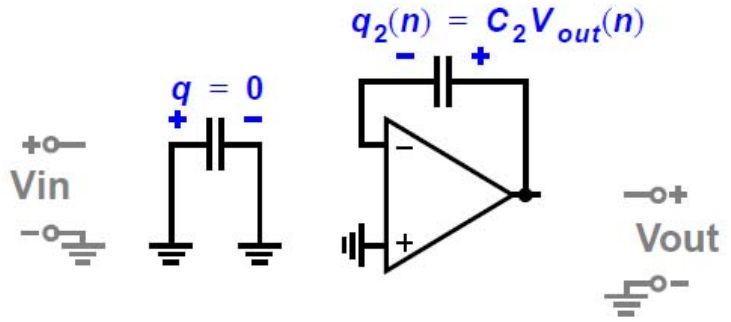
Single-ended circuit:



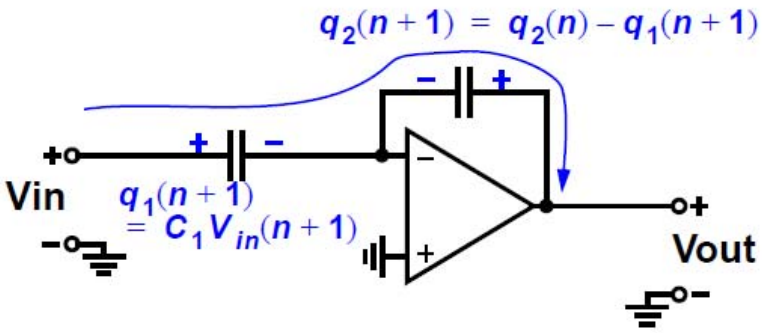
Timing:



ϕ2:



ϕ1:



Non-Delaying Integrator contd.

$$q_2(n+1) = q_2(n) - q_1(n+1)$$

$$z\,Q_2(z) = Q_2(z) - z\,Q_1(z)$$

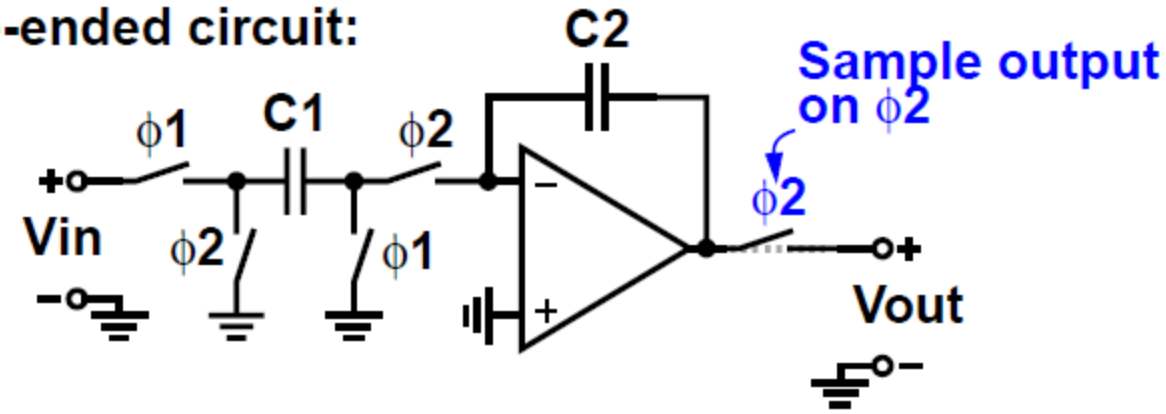
$$\frac{Q_2(z)}{Q_1(z)} = -\frac{z}{z-1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

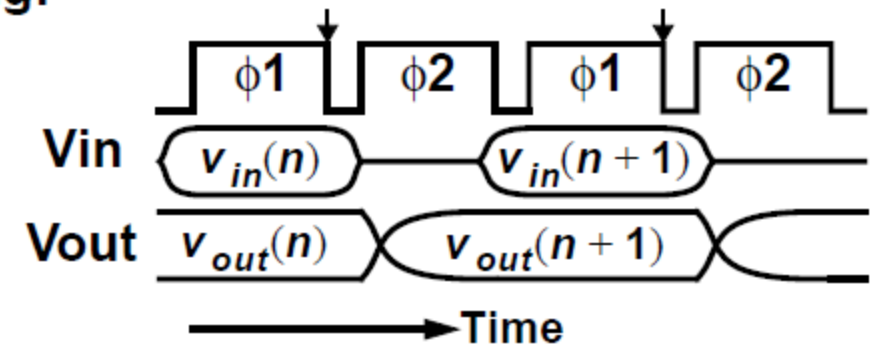
- **Delaying (and inverting) integrator**

Half-Delay Integrator

Single-ended circuit:



Timing:



Half-Delay Integrator

- **Output is sampled on a different phase than the input**
- **Some use the notation to denote the shift in sampling time**

$$H(z) = \frac{z^{-1/2}}{z-1}$$

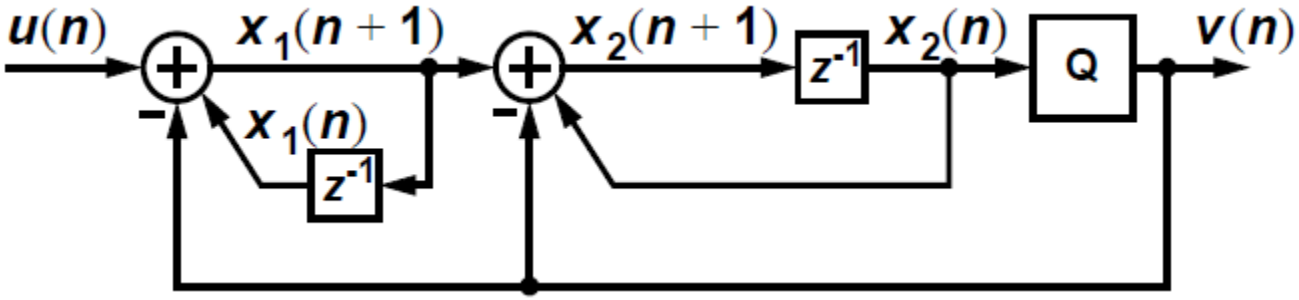
- **An alternative method is to declare that the border between time *n* *and n+1 occurs at the end* of a specific phase, say φ_2**

➢ **A circuit which samples on φ_1 and updates on φ_2 is non-delaying, i.e. *H(z) = z / (z – 1)***

whereas a circuit which samples on $\varphi 2$ and updates on φ_1 is delaying, i.e. *H(z) = 1 / (z – 1)*

Timing in a ΔΣ Modulator

- **The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations**
- **E.g. MOD2:**



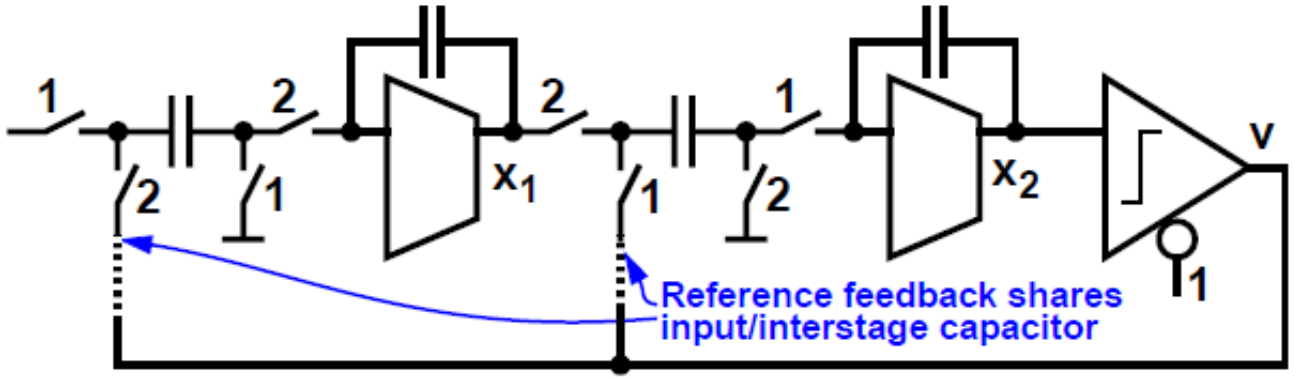
- **Difference Equations:**

$v(n) = Q(x_2(n))$

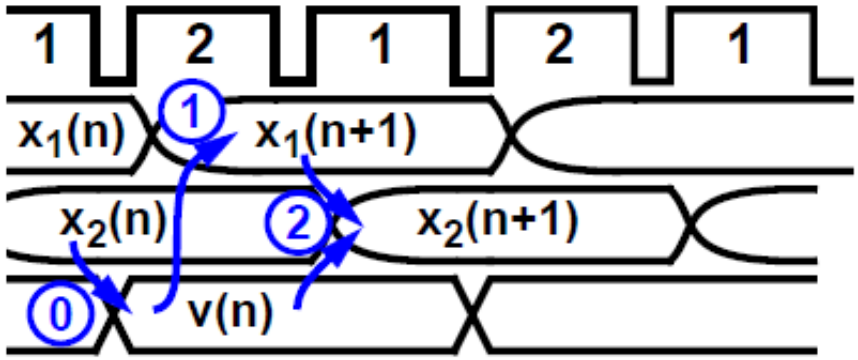
$x_2(n+1) = x_2(n) - v(n) + x_1(n+1)$

$x_1(n+1) = x_1(n) - v(n) + u(n)$

Switched-Capacitor Realization



Timing



Timing looks OK!

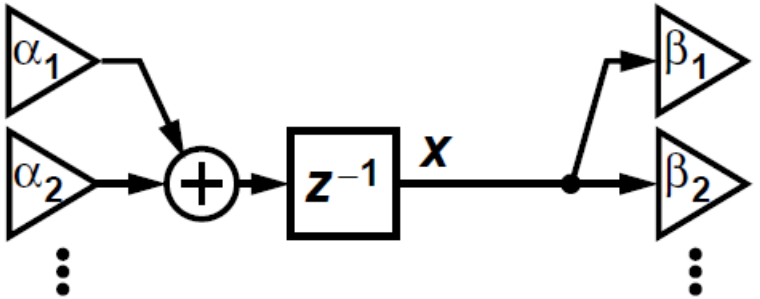
Signal Swing

- So far, we have not paid any attention to how much swing the op amps can support, or to the magnitudes of u, V_{ref}, x_1 and x_2
- For simplicity, assume:
  the full-scale range of u is ± 1 V,
  the op-amp swing is also ± 1 V and
  $V_{ref} = 1$ V
- We still need to know the ranges of x_1 and x_2 in order to accomplish *dynamic-range scaling*

Dynamic Range Scaling

- **In a linear system with known state bounds, the states can be scaled to occupy any desired range**

e.g. one state of original system:



state scaled by 1/*k*: