

Delta-Sigma Analog-to-Digital Converters

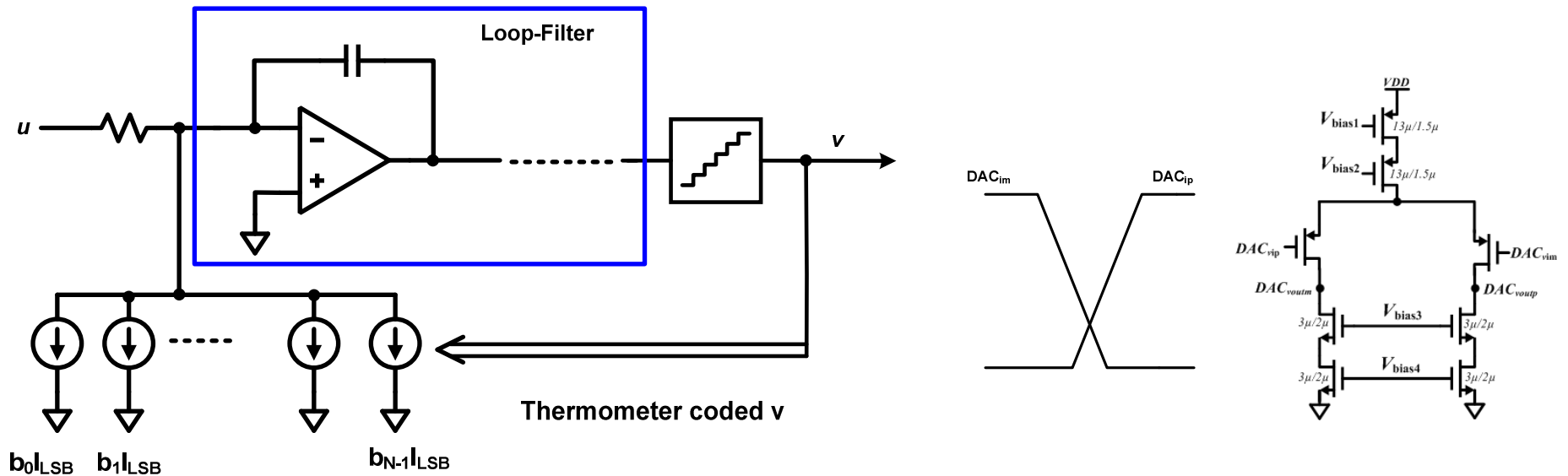
Feedback DAC Design

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Delta-Sigma ADC

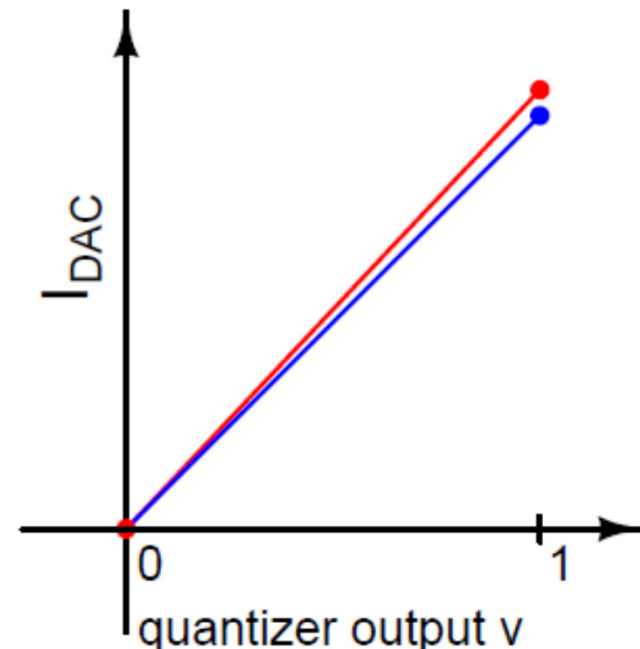
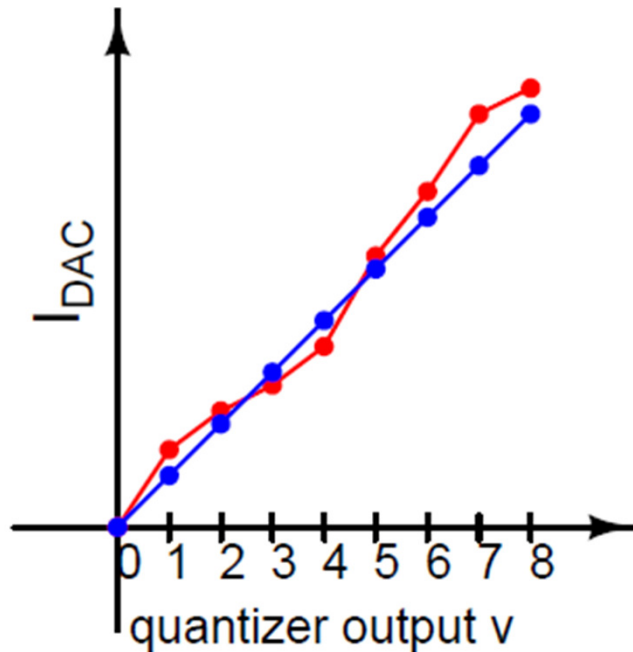
- ❑ Array of unit-weighted current steering DACs to pull and push current from the opamp current summing node
- ❑ Use high crossover pre-drivers to reduce DAC glitching noise

Feedback DAC Architecture



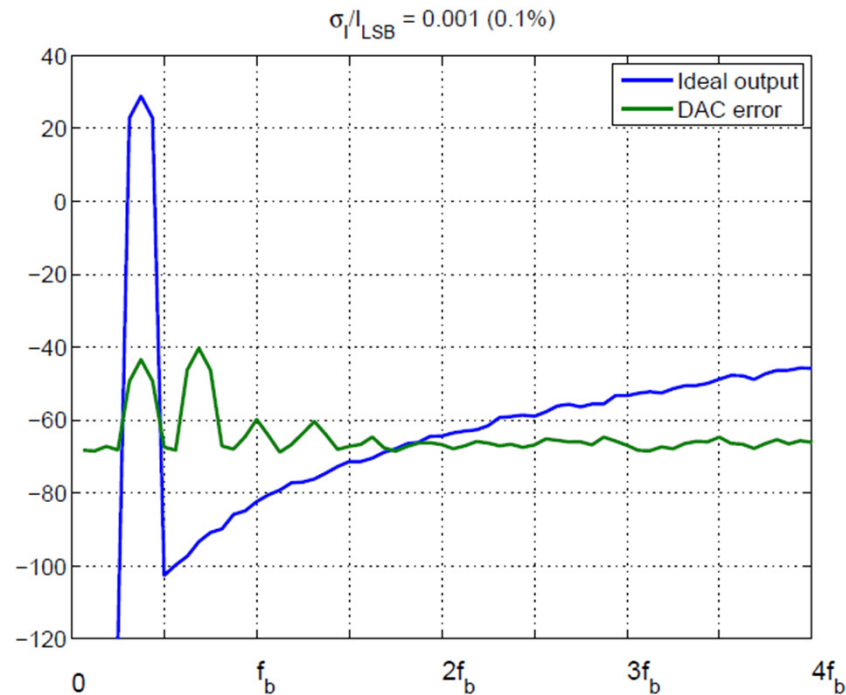
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Feedback DAC Nonlinearity



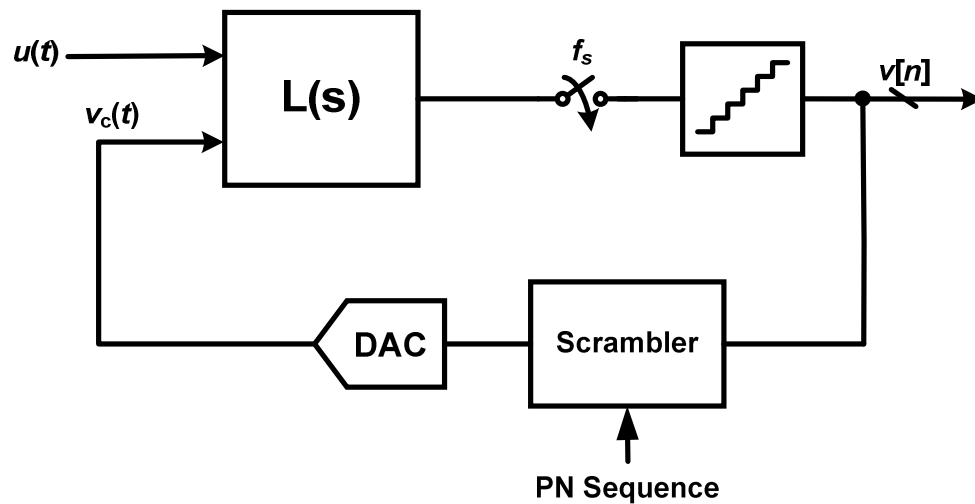
- In a multibit DAC, element mismatch leads to non-linearity
 - v is related to the input (u) by inverse non-linearity of the DAC
- A single-bit DAC is always linear

Feedback DAC Nonlinearity

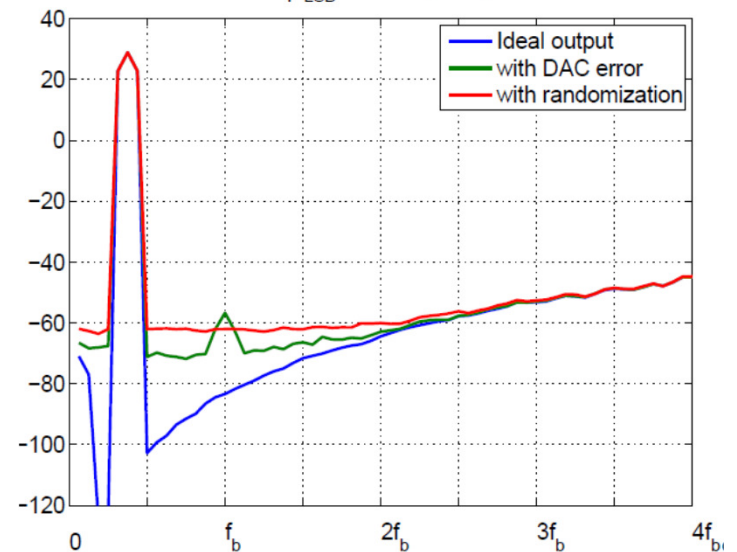
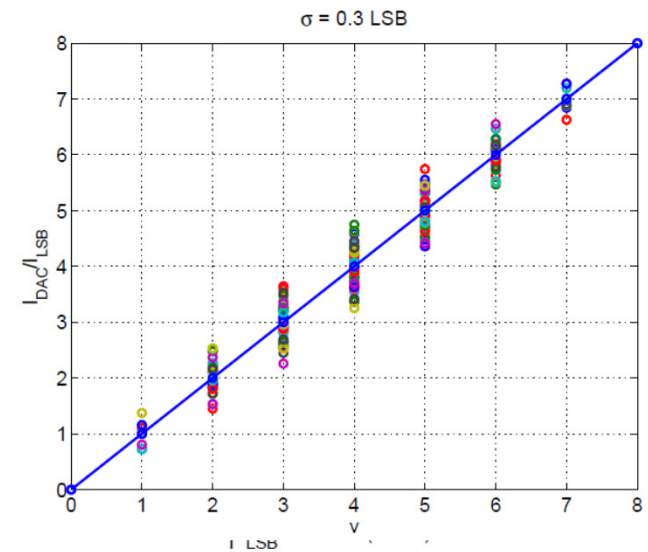


- Leads to distortion
- intermodulation of quantization noise into the signal band

Dynamic Element Matching (DEM)

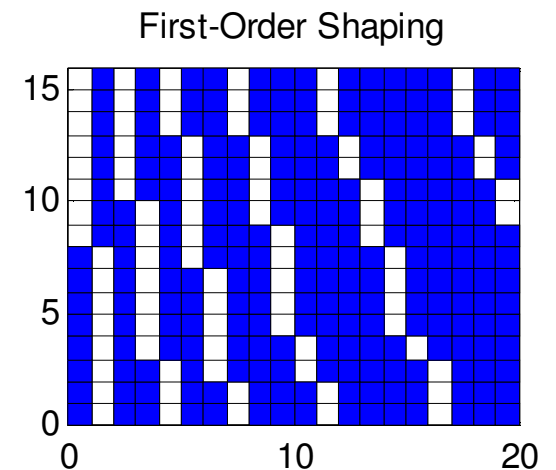
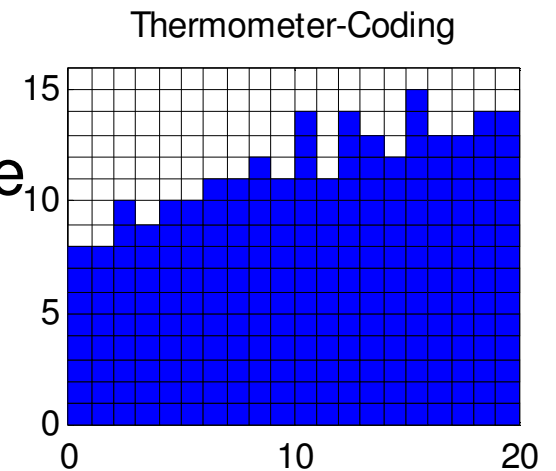
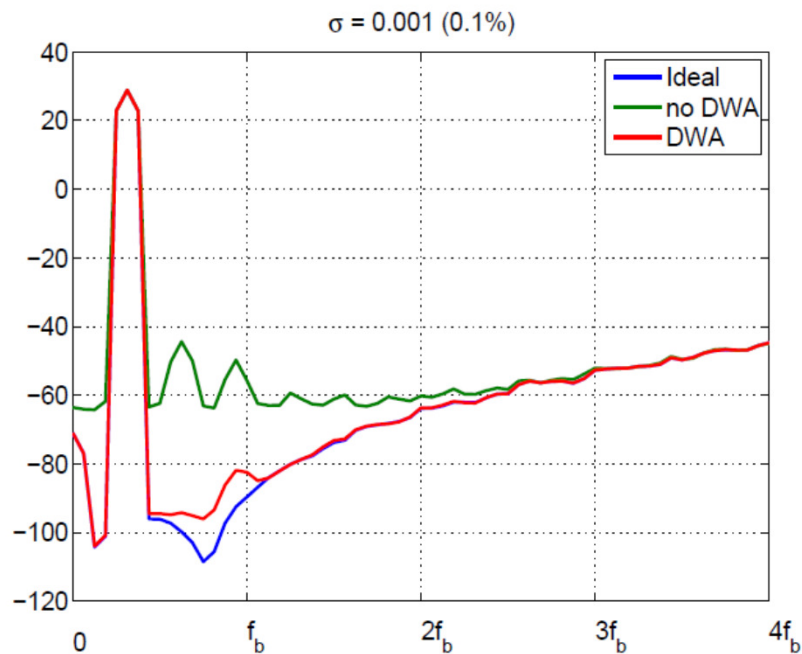


- Randomize the DAC elements
- Distortion components converted to noise
- Increased noise floor

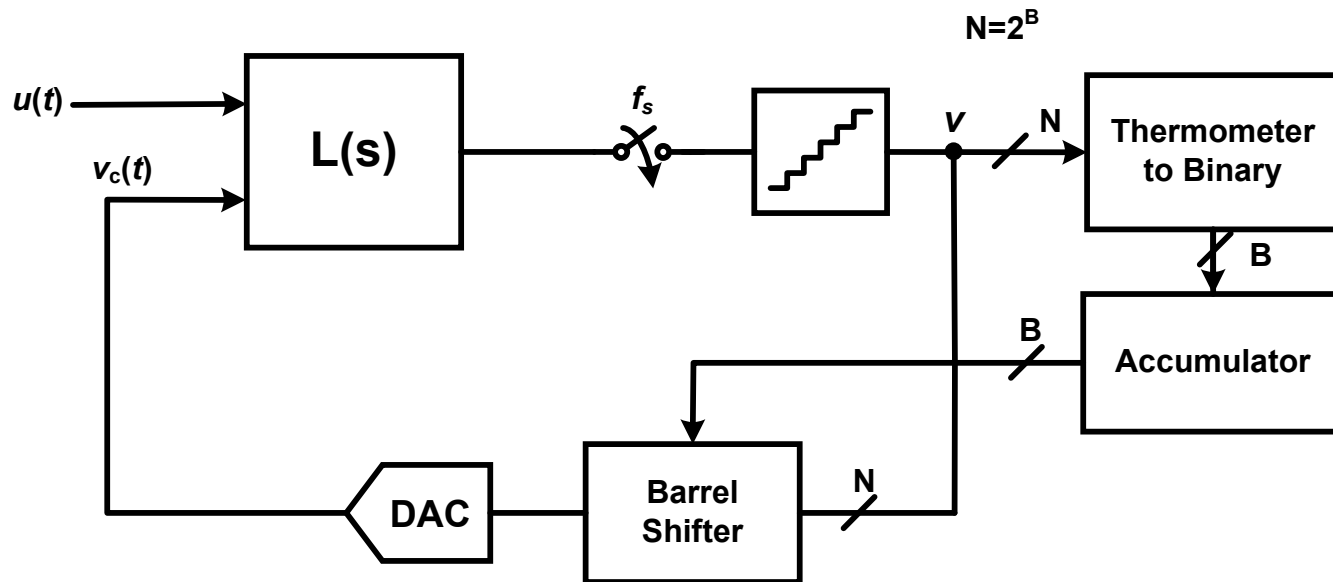


Data Weighted Averaging (DWA)

- Cycle through all the current elements as fast as possible
- Accumulate the input code and move the pointer
- First-order mismatch noise shaping



Data Weighted Averaging (DWA)

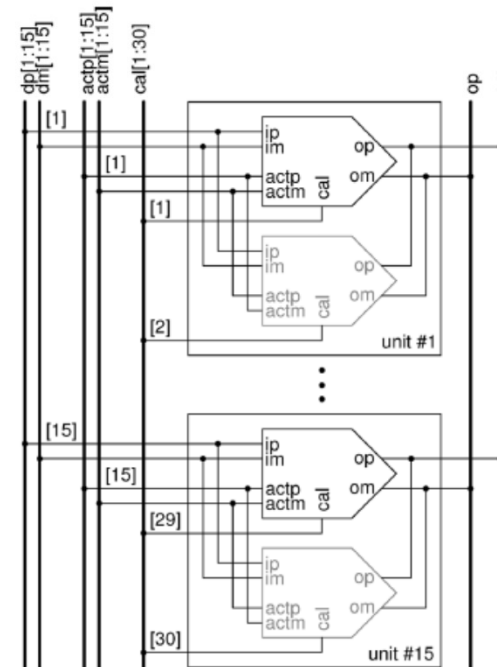
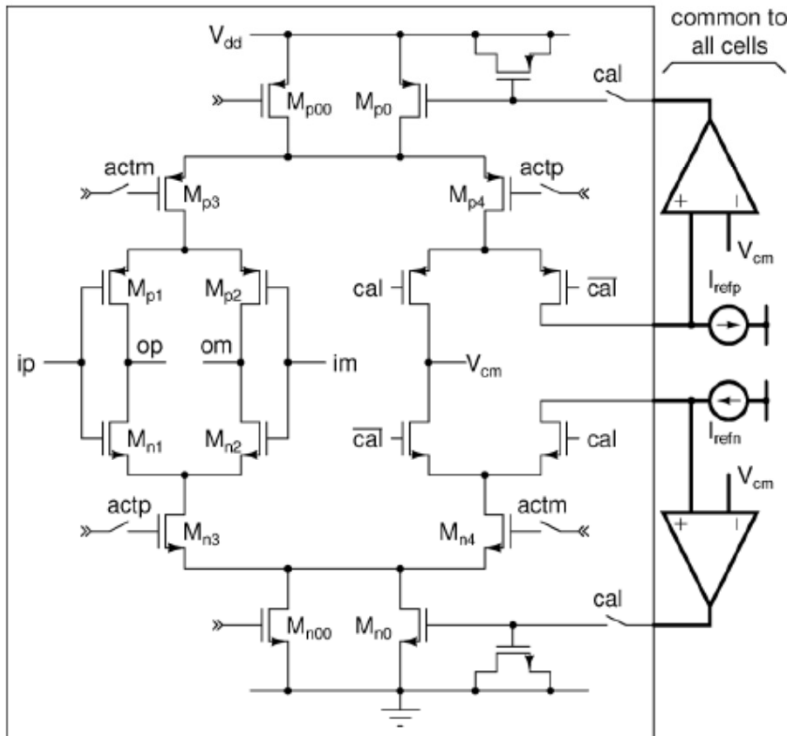


- Barrel shifter delay in the signal path increases loop delay
- Not viable at higher sampling rates (>400 MHz)

DAC Calibration

A 16 MHz BW 75 dB DR CT $\Delta\Sigma$ ADC Compensated for More Than One Cycle Excess Loop Delay

Vikas Singh, Nagendra Krishnapura, Shanthi Pavan, Baradwaj Vignraham, Debasish Behera, and Nimit Nigania



- Digital calibration – estimate element error and subtract from the output
 - Increased Decimation filter complexity
- Analog calibration – calibrate the elements with respect to a master
 - Need to calibrate at every cycle

References

1. R. Schreier, Matlab Delta-Sigma Toolbox, 2009 [[Online](#)].
2. S. Pavan, N. Krishnapura, EE658: Data Conversion Circuits Course at IIT Madras [[Online](#)].