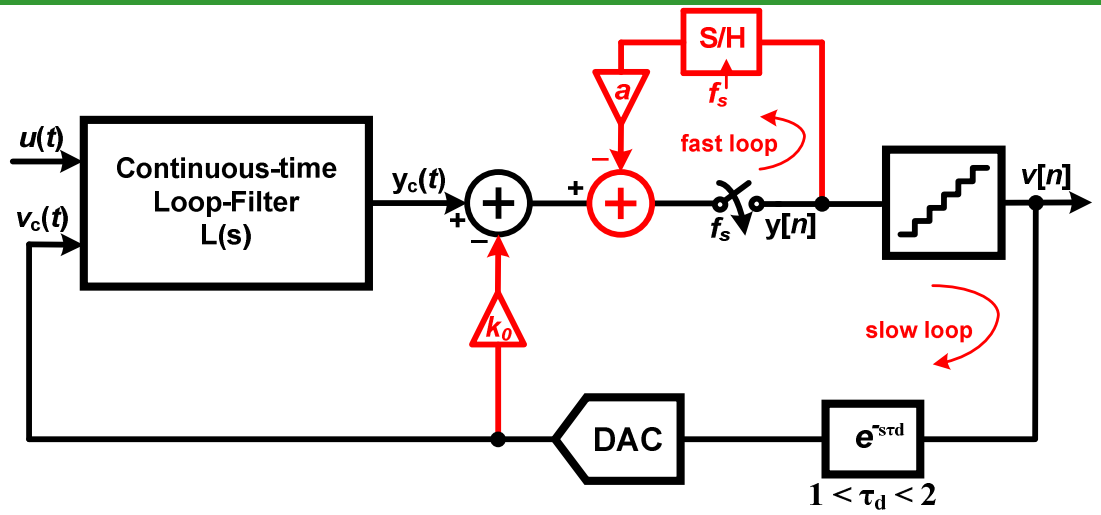
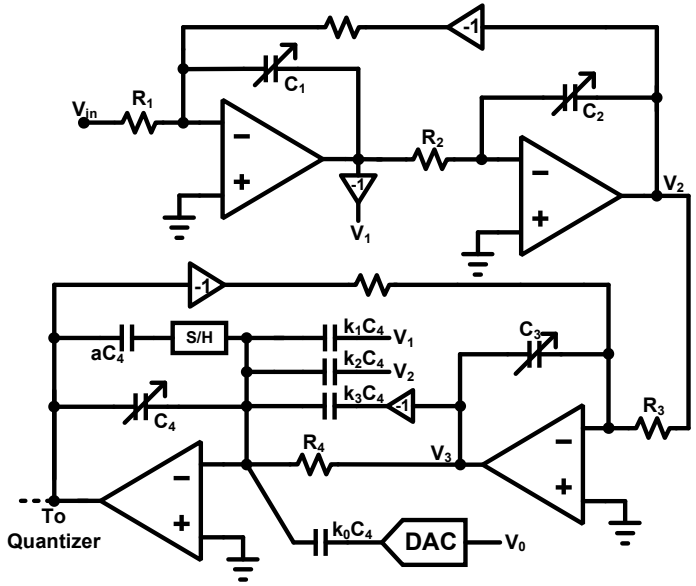
Delta-Sigma Analog-to-Digital Converters

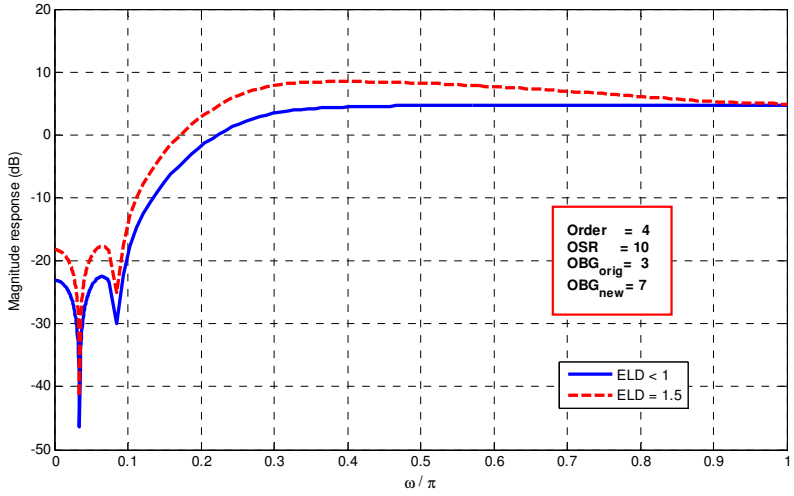
Recent Advances

Vishal Saxena, Boise State University
(vishalsaxena@boisestate.edu)

Employ Loop Delay > 1 Clock Cycle



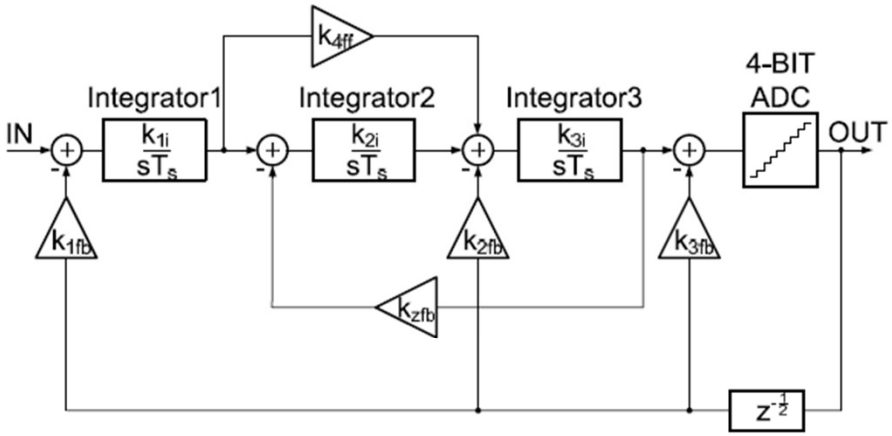


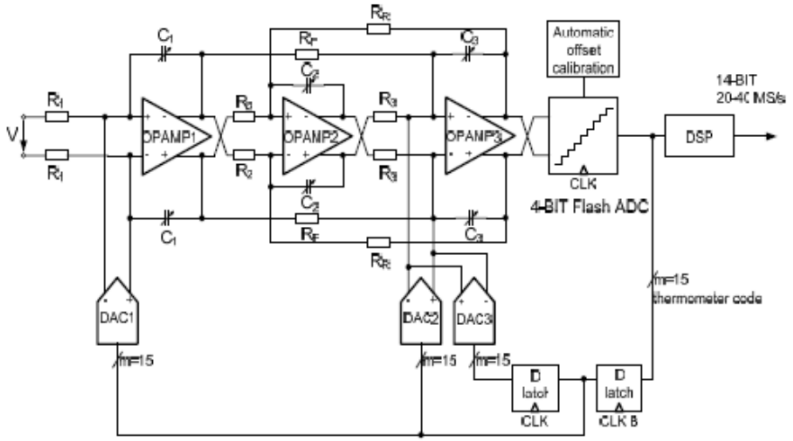


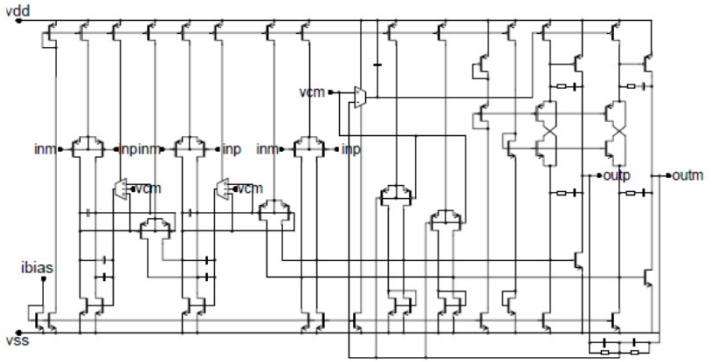
High-Performance CT-ΔΣ

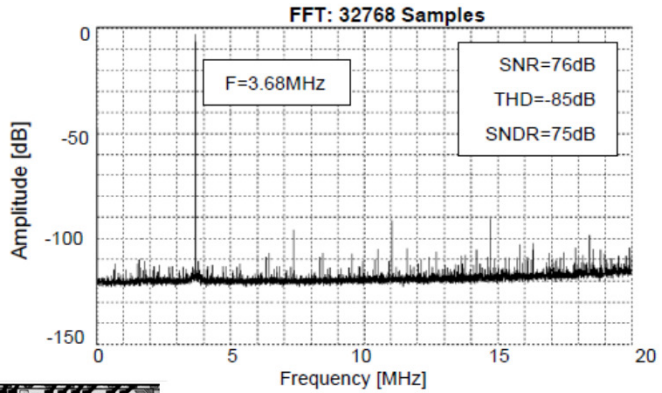
3.1 A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz Signal Bandwidth and 12b ENOB

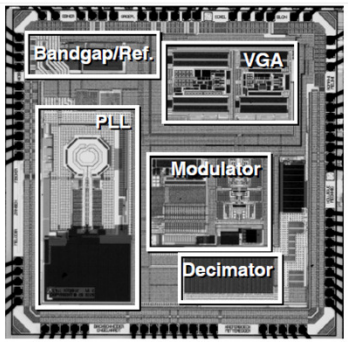
G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, E. Romani, A. Melodia, V. Melini









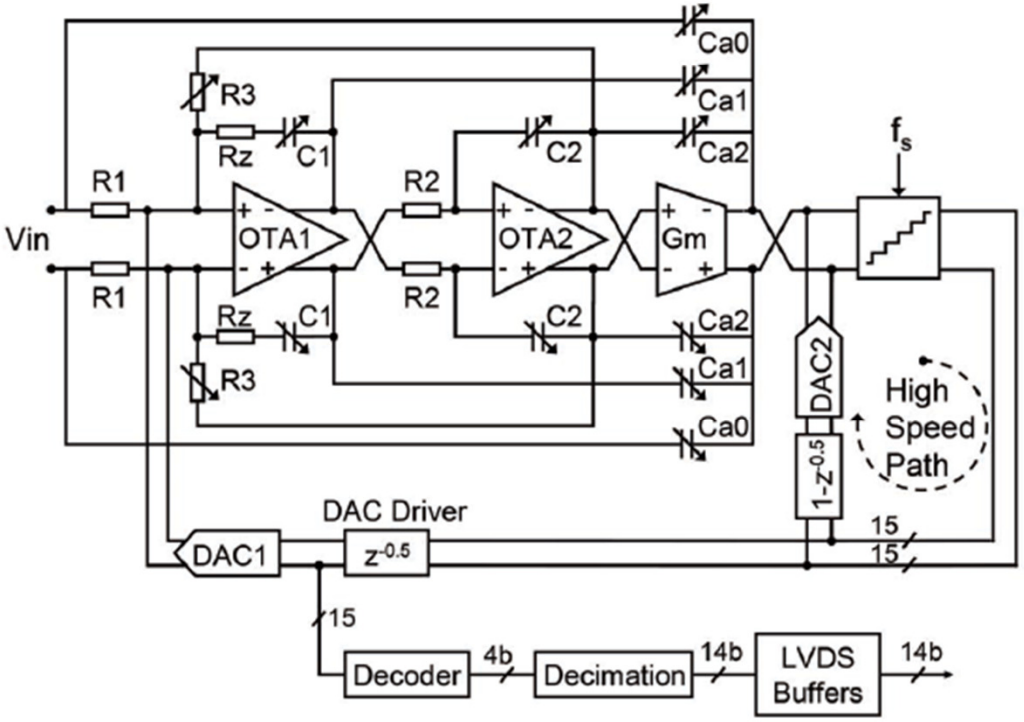


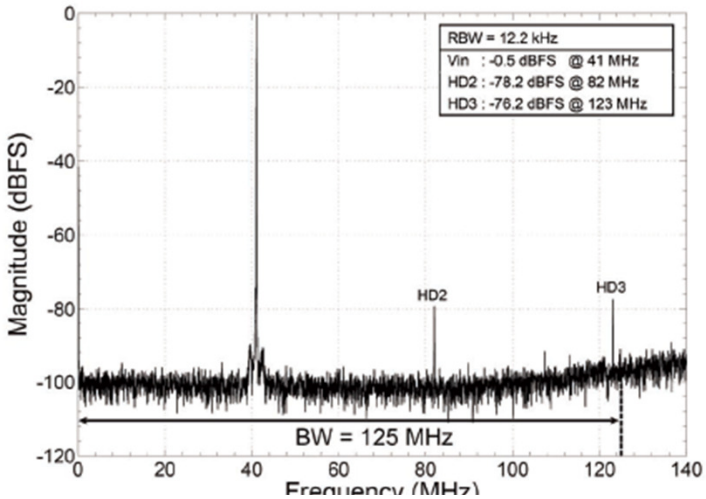
Sampling Frequency		640MHz
Conversion Rate		40MS/s
Signal Bandwidth		20MHz
Peak SNR @3.68MHz		76dB
THD@3.68MHz		-78dB
Peak SNDR@3.68MHz		74dB
Peak SNR @ 10MHz		76dB
THD@10MHz		-78dB
Peak SNDR @10MHz		74dB
ENOB		12
Power	Modulator 640MHz	20mW
	Decimator 40MS/s	18mW
	PLL 2.56GHz	12mW
	VGA	15mW
	I/O 1.8V	4mW
Power Supply		1.2V
Process		130nm 1P8M CMOS
Chip Area		8.6mm²

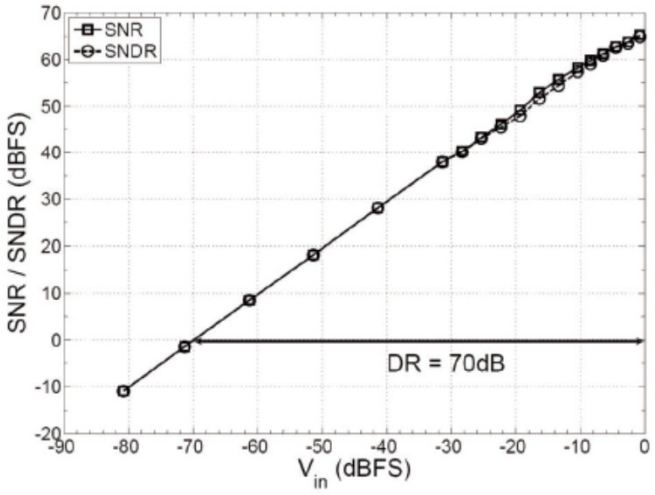
4 GHz Multi-bit CT-ΔΣ without DEM

27.1 A 4GHz CT ΔΣ ADC with 70dB DR and –74dBFS THD in 125MHz BW

Muhammed Bolatkale[1], Lucien J. Breems[1], Robert Rutten[1], Kofi A.A. Makinwa[2]





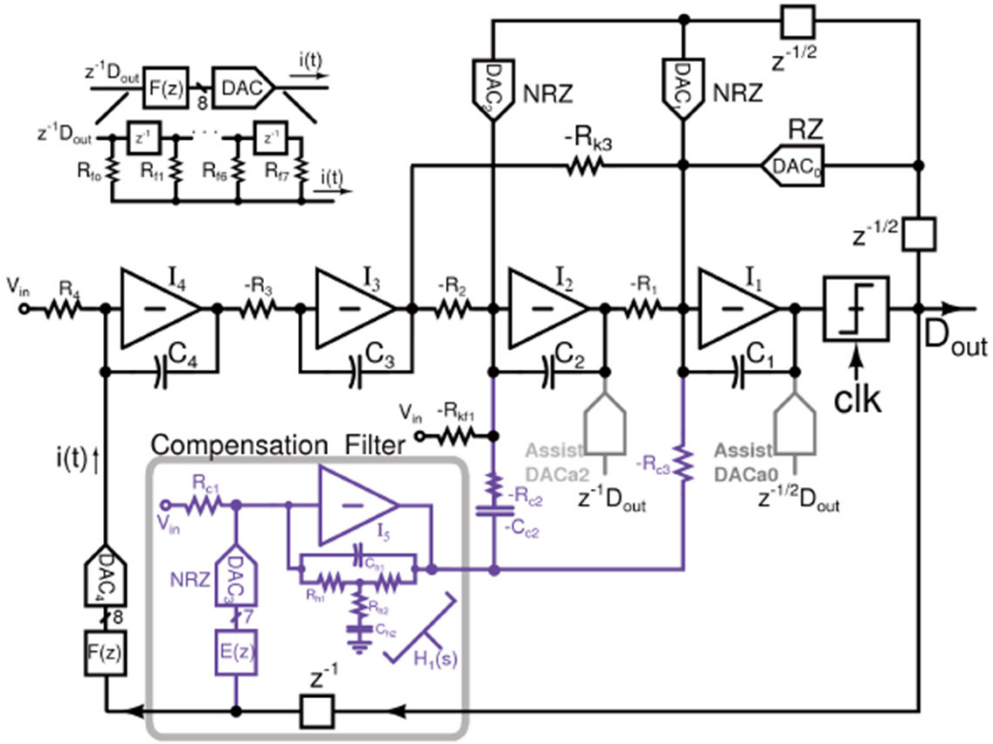


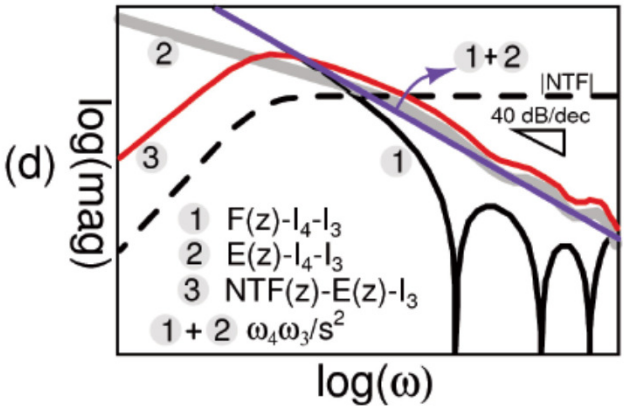
3.6 GHz Single-bit CT-ΔΣ with FIR DAC

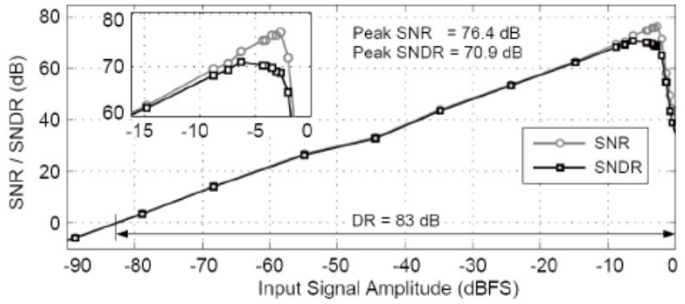
8.6 A 15mW 3.6GS/s CT-ΔΣ ADC with 36MHz Bandwidth and 83dB DR in 90nm CMOS

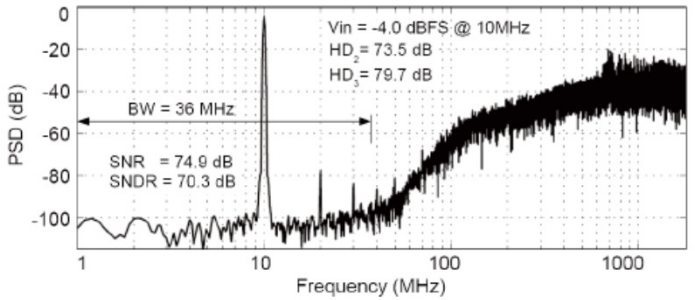
Pradeep Shettigar, Shanthi Pavan

Indian Institute of Technology, Madras, India





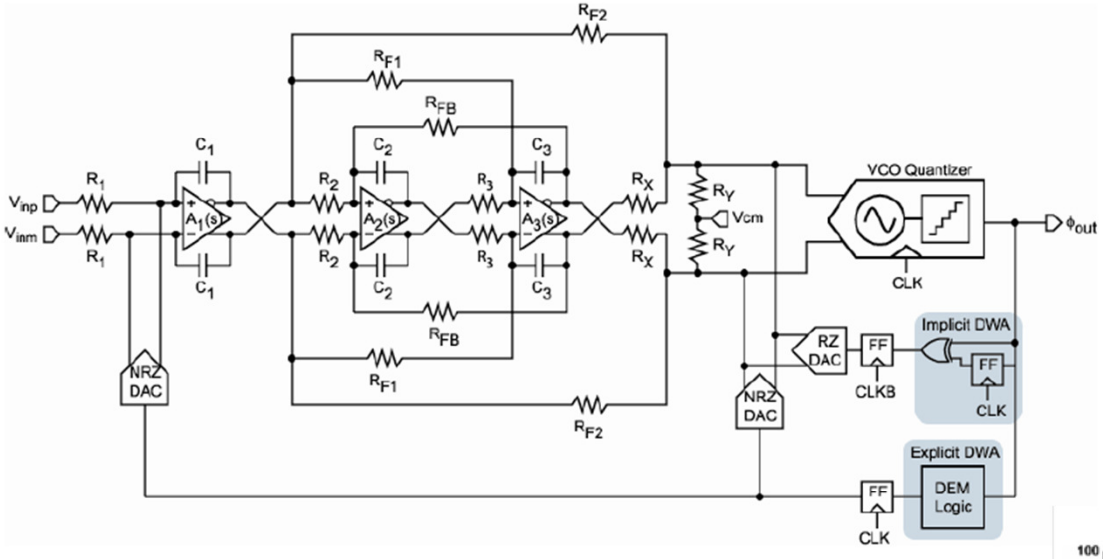


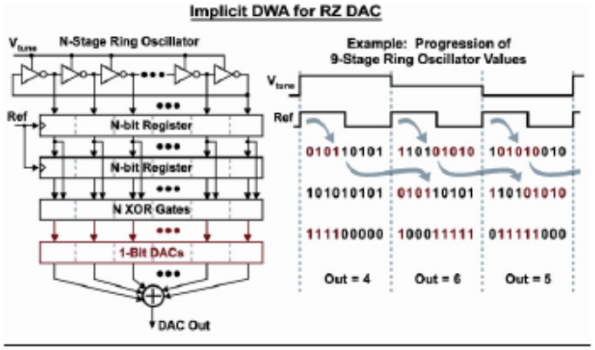


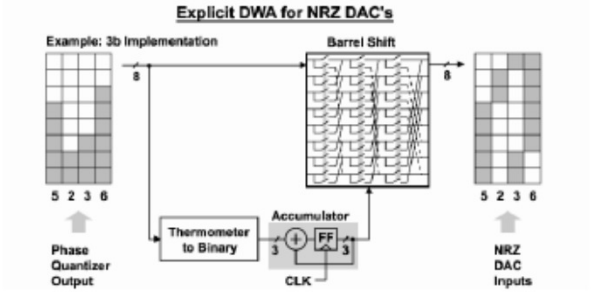
Phase-Domain Integrator and Quantizer

9.5 A 0.13µm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-Based Integrator and Quantizer

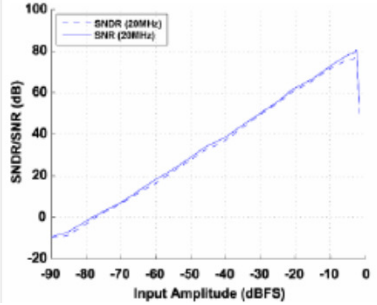
Matt Park[1], Michael Perrott[2]

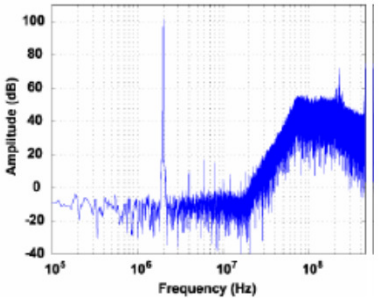






Specification	Value
Sampling Frequency	900MHz
Input Bandwidth	20MHz
Peak SNR	81.2dB
Peak SNDR	78.1dB
Analog Power	69mW (1.5V)
Digital Power	18mW (1.5V)
FOM = power/(2*BW*2^{ENOB})	330fJ/conv.
Active Area	0.45mm^2
Technology	0.13um IBM CMOS

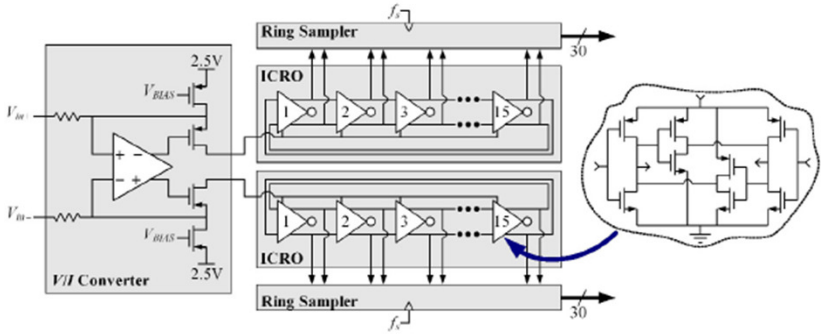


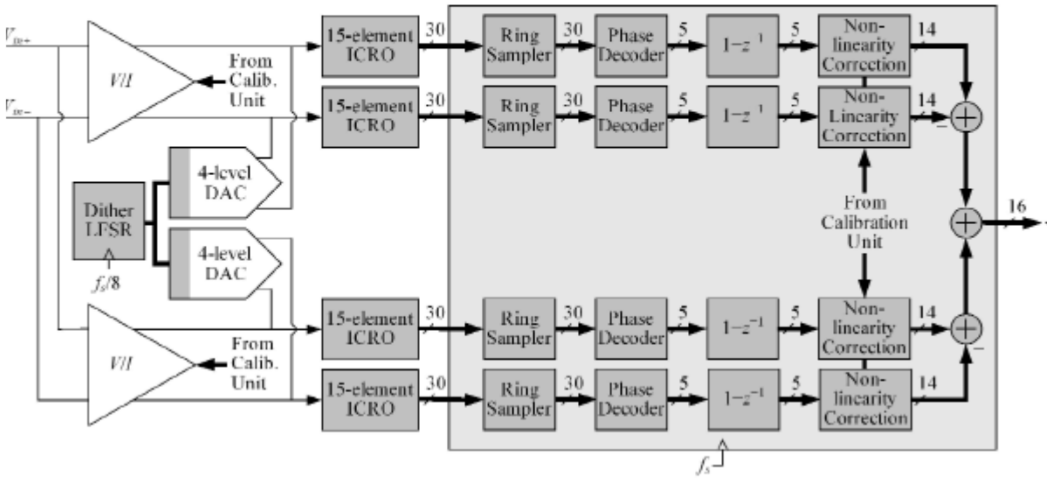


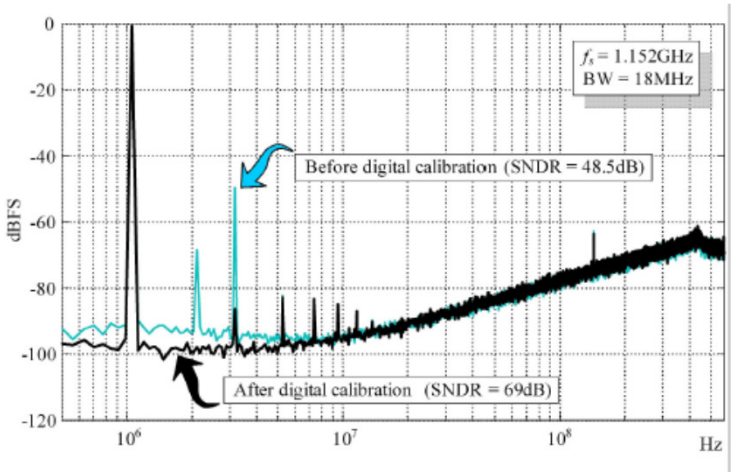
VCO Quantizer-based All-Digital ΔΣ

16.4 A Mostly Digital Variable-Rate Continuous-Time ADC ΔΣ Modulator

Gerry Taylor[1,2], Ian Galton[1]



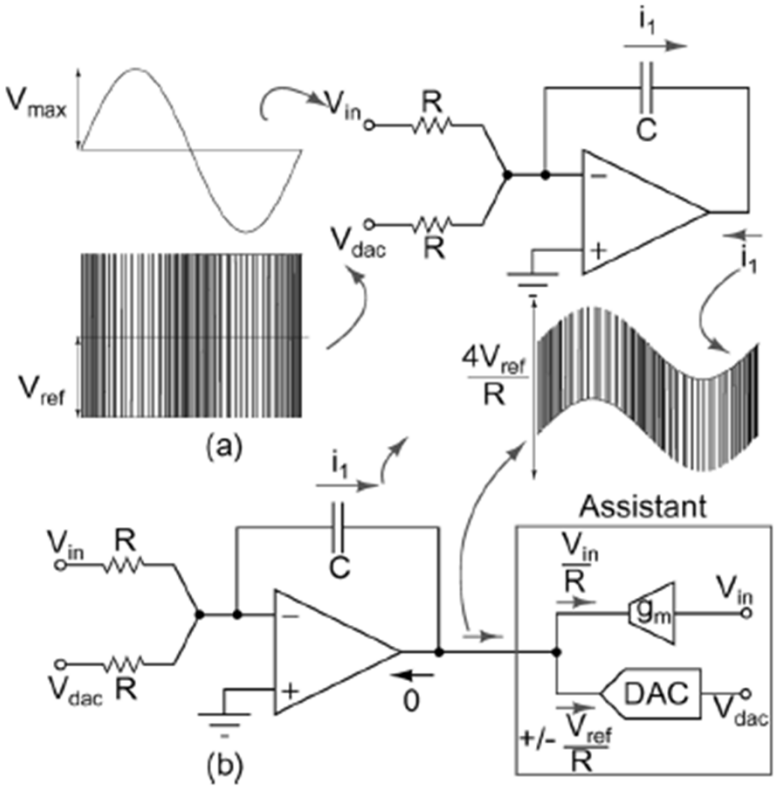


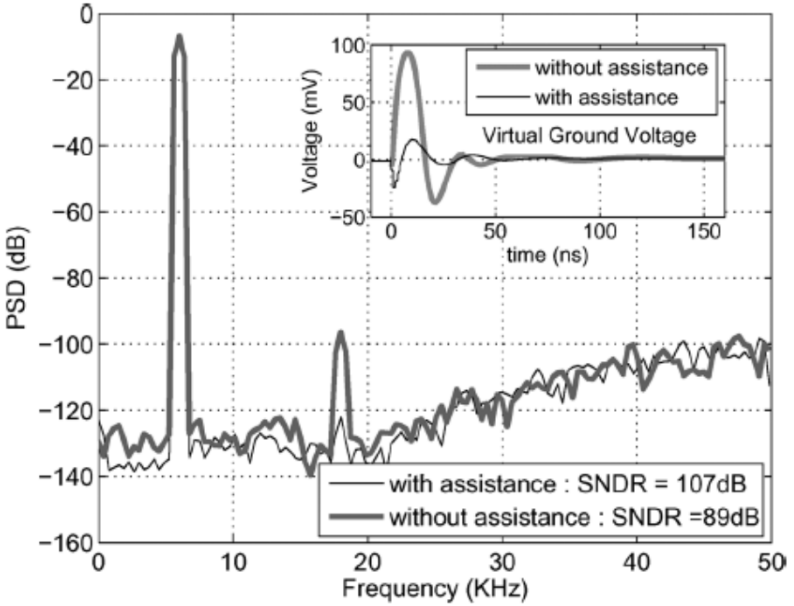


Assisted Opamp for Linearity Improvement

Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique

Shanthi Pavan, *Member, IEEE*, and Prabu Sankar

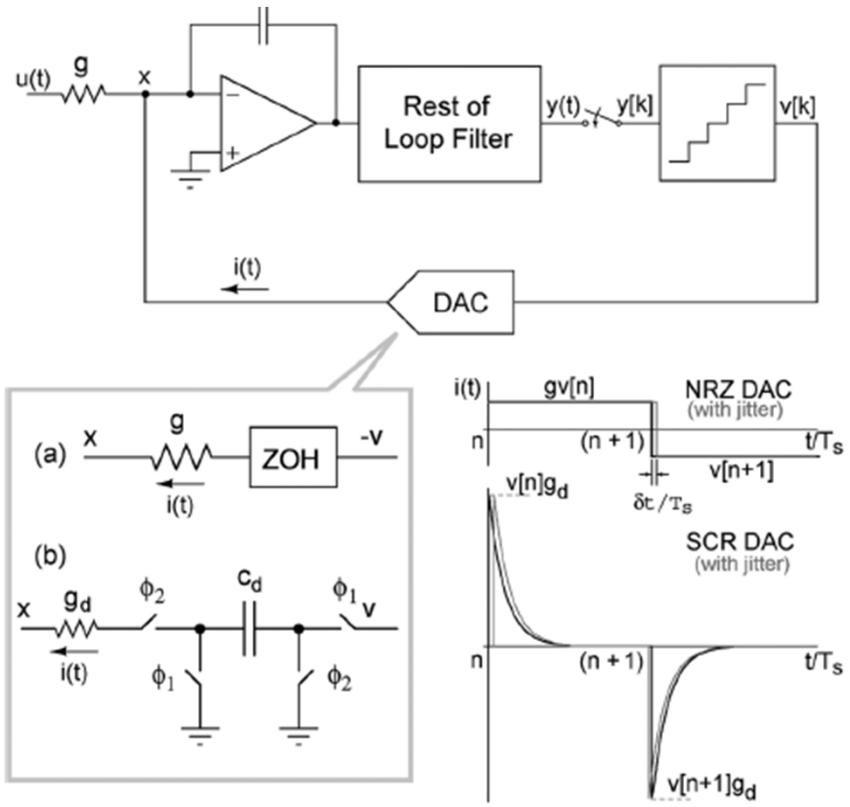


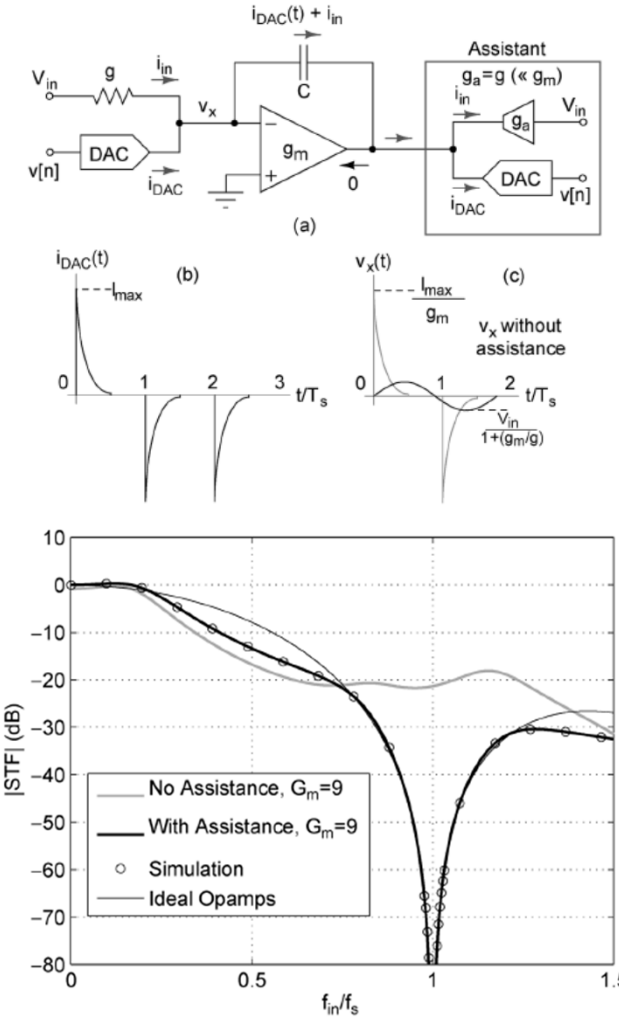


Assisted Opamp for SCR DAC CT-ΔΣ

Alias Rejection of Continuous-Time ΔΣ Modulators With Switched-Capacitor Feedback DACs

Shanthi Pavan, *Member, IEEE*

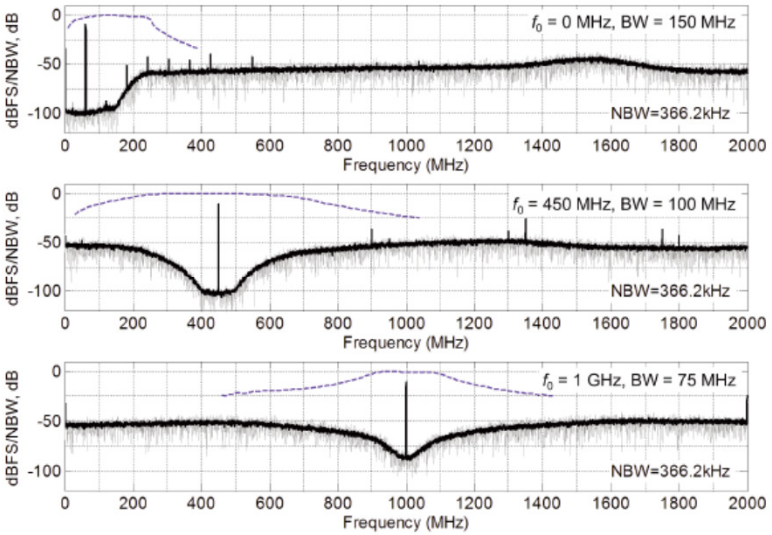


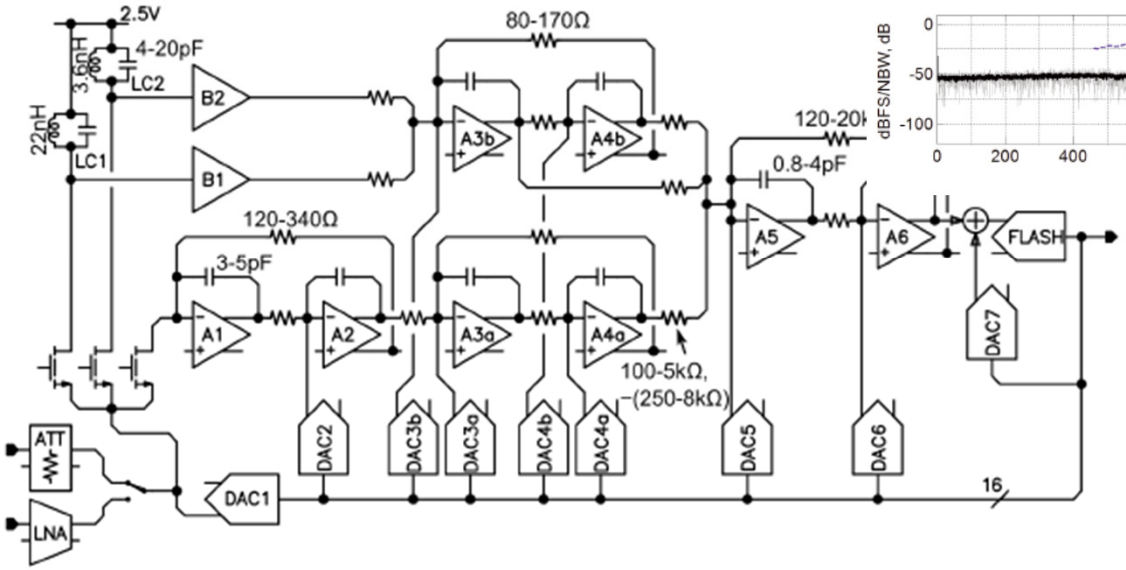


DC-RF Tunable ΔΣ ADC

8.3 A DC-to-1GHz Tunable RF ΔΣ ADC Achieving DR = 74dB and BW = 150MHz at f_0 = 450MHz Using 550mW

Hajime Shibata[1], Richard Schreier[1], Wenhua Yang[2], Ali Shaikh[2,3], Donald Paterson[2], Trevor Caldwell[1], David Alldred[1], Ping Wing Lai[2]





Future Looking Ideas in CT-ΔΣ ADCs

- CT-ΔΣ ADCs are in their infancy, and scope for innovation is great
- Direct RF-Digital Conversion
- Multi-band, Multi-Standard, Reconfigurable ADCs
- Cognitive Radios
- Cascaded (MASH) DSM: LP, BP and Quadrature
  - Digital Calibration of Circuit Errors
- Parallel ΔΣ ADC (Frequency Band Decomposition)
- VCO Quantizers and Time/Phase domain signal processing