Project 2

ECE 615 – Mixed Signal IC Design

Due on December 19, 2013.

1 Problem Statement

Design of a Continuous-time $\triangle\Sigma$ ADC: This project involves *realistic* design process for a $\triangle\Sigma$ ADC intended for audio applications. The design is to be implemented using a 180-nm mixed-mode CMOS process with a $V_{DD} = 1.8\,V$ supply voltage. The target specifications for the single-loop multi-bit audio $\triangle\Sigma$ modulator are as follows:

Table 1: $\triangle\Sigma$ ADC design specifications.

Parameter	Specified Value
Supply voltage, V_{DD}	1.8 V
Input signal bandwidth (f_B)	24 KHz
Resolution	$\geq$ 16 bits
Minimum Full-Scale (FS) input voltage	$0.6 \cdot V_{DD}$
Maximum sampling rate ($f_{s,max}$)	12.5 MHz
Quantizer Range (fully-differential)	3 $V_{pp,diff}$
Clock jitter (rms)	$1\,ps$
Chip-to-chip RC time-constant variation	$\pm$30%

2 $\triangle\Sigma$ Modulator Design

The following steps will guide you through the design and documentation process.

1. **Design Space Selection:** Determine the order (L), OSR, the number of quantizer levels (nLev) and the out-of-band gain (OBG). Provide reasons for your choice of design space (L, OSR, nLev, OBG) and argue why is your choice is optimal.

2. **NTF Design:** Determine a suitable NTF for your design. Plot the theoretical SNR, SNDR (in dB) vs amplitude (in dBFS), and mark peak-SNR, peak-SNDR, DR and SFDR on the plot (create a script).

3. **CT Loop-Filter Design:**

   (a) The loop-filter is implemented using fully-differential Active-RC circuits. Select a suitable DAC pulse shape for your design (*NRZ, RZ, Switched-RC, etc.*) with a reasonable ELD value (say $\tau = 0.1\,Ts$). Show relevant plots including $NTF(e^{j\omega})$ and $STF(j\omega)$ with the selected loop-filter topology (*FB*, *FF* or a hybrid type).

   (b) Find the loop-filter coefficients ($K = [k_0\, k_1\, k_2\, k_3 \ldots]^T$) and the resonator coefficient (γ_1). **Note:** In a practical design, this step is iterated upon using a systematic design centering

method [3] which accounts for the higher-order poles and zeros in the integrator opamps. You can skip systematic design this in this project.

(c) Use Thermal and Jitter noise analysis for the modulator and obtain the R and C values for the integrators after appropriate noise budgeting[**?**].

(d) Translate the designed loop-filter to a fully-differential Active-RC topology[2]. The opamps, current DACs and Quantizer (Flash A/D) are behavioral. Your opamp behavioral model should have f_{un} and A_{OL}.

(e) Neatly create the loop-filter schematic in Cadence Virtuoso using the behavioral models after time-scaling the design for the actual sampling rate (f_s). Make use of the config view to switch between different schematic cell views.

(f) Knowing that the op-amps in the integrators are linear for less than 50% of the V_{DD}, limit the integrator output range to 1.5 $V_{pp,diff}$ (peak-to-peak differential). Apply Dynamic Range Scaling (DRS) to ensure that the loop-filter states are bounded and the integrators don't saturate. This is achieved by scaling the integrator unity-gain frequencies (ω_j). Neatly tabulate the resulting loop-filter coefficients (K), integrator unity-gain frequencies ($[\omega_1\, \omega_2\, \omega_3 \ldots]$), resonator coefficient (γ_1) and the resulting R and C values. If needed, a very large value of resistor ($> 10\, M\Omega$) can be implemented using a T-circuit.

4. **Ideal Schematic Simulation:**

(a) Simulate the ideal CT loop-filter and compare its impulse response with the one simulated using MATLAB. Ensure that the simulated loop-filter impulse response behaves as expected. AC analysis in SpectreRF can also be used to simulate the frequency response of the CT loop-filter.

(b) Next, close the loop around the loop-filter and the quantizer and thus forming the modulator. Find the MSA using the slow-ramp input method and plot the results.

(c) By appropriately choosing an sinusoidal input frequency (i.e. $f_{in} = \frac{m}{N_{FFT}} f_s$), simulate the modulator schematic with an amplitude of $0.9\, MSA$. Plot the resulting modulator PSD with a 1024-point Hann window and compare the in-band SQNR with the results in part (3).

(d) Plot the waveforms at the output of each integrator (CT loop-filter states) and show that they don't go beyond the linear range (i.e. 1.5 $V_{pp,diff}$).

(e) Find the THD of the modulator for an input amplitude of -1 dB below MSA (i.e. 0.9 MSA).

5. **Schematic Simulation with Circuit Non-idealities:**

Discuss how will you optimize the overall power consumption of the designed modulator when implemented in the selected CMOS process. Set the appropriate values for your op-amp models (f_{un}, A_{OL}, etc.) . Make sure the 'golden' integrator in the loop-filter is appropriately designed. Repeat step (5) with this design model.

You may additionally model other circuit non-idealities like switch non-linearity, clock jitter, quantizer non-idealities, etc. A behavioral simulation model like **SIMSIDES** is usually used to verify system level performance of such designs [6].

3 Final Report

Submit your neatly typed report in a two-column IEEE transactions format [7]. Show neatly drawn schematics and block diagrams. You may download the Visio schematic symbols from the course website [8]. Provide relevant references in your report. Show the modulator overall ADC performance (peak SNR/SNDR, dynamic range, THD, etc.) in a neatly tabulated manner along with the conclusion.

References

[1] A 24-bit, 192 kHz Multi-bit Audio ADC: CS5430 Datasheet, Wesbite, Cirrus Logic, 2008.

[2] S. Pavan, N. Krishnapura, R. Pandarinathan and P. Sankar, "A Power Optimized Continuous-time Delta-Sigma Modulator for Audio Applications," IEEE JSSC, vol. 43, no. 2, pp. 351-360, Feb. 2008.

[3] S. Pavan, "Systematic Design Centering of Continuous-time Oversampling Converters." IEEE TCAS-II: Express Briefs, vol. 57, no. 3, pp. 158-162, 2010.

[4] S. Pavan and N. Krishnapura, "Automatic Tuning of Time-Constants in Continuous-Time Delta-Sigma Modulators," IEEE TCAS-II: Express Briefs, vol. 54, no. 4, pp. 308-312, Apr. 2007.

[5] Li, T. S. Fiez, "A 14-bit Continuous-Time Delta-Sigma A/D Modulator with 2.5 MHz Signal Bandwidth," IEEE JSSC, vol. 42, no. 9, pp. 1873-1883, Sept. 2007.

[6] SIMSIDES, SIMulink-based SIgma-DElta Simulator ," University of Seville. Available [Online].

[7] IEEE Transactions Templates. Available [Online].

[8] Visio Schematic Symbols. Available [Online].