

Project 1

ECE 615 – Mixed Signal IC Design

Due on November 21, 2013.

1 Problem Statement

Design of an Audio ADC: This project involves *realistic* design process for a $\Delta\Sigma$ ADC intended for audio recording devices. The design is to be implemented using a 180-nm mixed-mode CMOS process with a $V_{DD} = 1.8V$ supply voltage. The target specifications for the single-loop multi-bit audio $\Delta\Sigma$ modulator are as follows:

Table 1: $\Delta\Sigma$ ADC design specifications.

Parameter	Specified Value
Supply voltage, V_{DD}	1.8 V
Input signal bandwidth (f_B)	24 KHz
Resolution	≥ 18 bits
Minimum Full-Scale (FS) input voltage	$0.6 \cdot V_{DD}$
Output sample rate (after decimation)	48 KHz
Maximum clock speed (f_{CLK})	12.5 MHz
Quantizer Range (fully-differential)	$3 V_{pp,diff}$

For details on noise calculations in audio conversion systems refer to [2].

2 $\Delta\Sigma$ Modulator Design

The following steps will guide you through the design and documentation process. Also refer to the design example in Chapter 9 of the textbook.

1. **Design Space Selection:** Determine the order (L), OSR, the number of quantizer levels (nLev) and the out-of-band gain (OBG). Provide reasons for your choice of design space (L, OSR, nLev, OBG) and argue why is your choice is optimal.
2. **NTF Design:** Determine a suitable NTF for your design. Plot the theoretical SNR, SNDR (in dB) vs amplitude (in dBFS), and mark peak-SNR, peak-SNDR, DR and SFDR on the plot (create a script).
3. **Loop-Filter Design:** Select a loop-filter architecture to implement the designed NTF.
 - (a) The loop-filter is implemented using fully-differential discrete-time circuits. Knowing that the op-amps in the integrators are linear only for roughly 50% of the V_{DD} , limit the integrator output range to $1.5 V_{pp,diff}$ (peak-to-peak differential). Apply Dynamic Range Scaling (DRS) to ensure that the loop-filter states are bounded and the op-amps don't saturate.

- (b) Find the effective quantizer gain (k) using simulations and use this value to ensure that the STF is distortionless (e.g. $b_{N+1} = 1/k$). Also show that the modulator is stable with the quantizer gain variation (*Hint*: NTF root locus).
 - (c) Find the loop-filter coefficients and quantize them to a realizable capacitor ratio. To quantify the degradation due to coefficient quantization, compare the original NTF response with the final one. Neatly tabulate the original and final loop-filter coefficients, and the required capacitor ratios. Show relevant plots including $NTF(e^{j\omega})$ and $STF(e^{j\omega})$ with the selected loop-filter topology.
 - (d) Simulate the resulting modulator topology in MATLAB showing its performance. Show that the modulator states lie in the linear range when the input is within the stable input range.
4. **Switched-Capacitor Design:** Translate the designed loop-filter to a fully-differential switched-capacitor topology. The opamps and comparator are behavioral while the switches should be transistor-level.
- (a) Determine the required clock timing for the switches from the loop-filter difference equations.
 - (b) Use thermal noise analysis for the modulator and obtain the base capacitor value set by the kT/C noise with appropriate noise budgeting[3]. Select optimal switch sizing to minimize thermal noise and determine all the capacitor values required to implement the range-scaled loop-filter.
 - (c) Create a simple behavioral model for the op-amp to emulate the non-ideal behavior resulting from their transistor-level implementation. Your opamp behavioral model should have f_{un} and A_{OL} , while you can try to include non-idealities such as slewing and limiting behavior. Also, use a verilog-A model of the comparator/quantizer.
 - (d) Neatly create the loop-filter schematic in Cadence Virtuoso using the behavioral models. Make use of the config view to switch between different schematic cell views. You may use ideal non-overlapping clock phases (ϕ_1 and ϕ_2) with realistic rise and fall times. In this project, assume that the feedback DAC capacitors have no mismatch (no DEM/DWA in this design).
5. **Ideal Schematic Simulation:**
- (a) Simulate the ideal switched-capacitor loop-filter and compare its impulse response with the one simulated using MATLAB. Ensure that the simulated loop-filter impulse response behaves as expected. PSS analysis in SpectreRF can also be used to simulate the frequency response of the discrete-time loop-filter [4, 5].
 - (b) Next, close the loop around the loop-filter and the quantizer and thus forming the modulator. Find the MSA using the slow-ramp input method and plot the results.
 - (c) By appropriately choosing an sinusoidal input frequency (i.e. $f_{in} = \frac{m}{N_{FFT}} f_s$), simulate the modulator schematic with an amplitude of $0.9 MSA$. Plot the resulting modulator PSD with a 1024-point Hann window and compare the in-band SQNR with the results in part (3).

- (d) Plot the waveforms at the output of each integrator (loop-filter states) and show that they don't go beyond the linear range (i.e. $1.5 V_{pp,diff}$).
- (e) Find the THD of the modulator for an input amplitude of -1 dB below MSA (i.e. 0.9 MSA).

6. Schematic Simulation with Circuit Non-idealities:

Discuss how will you optimize the overall power consumption of the designed modulator when implemented in the selected CMOS process. Set the appropriate values for your op-amp models (f_{un} , A_{OL} , etc.) . Make sure the 'golden' integrator in the loop-filter is appropriately designed. Repeat step (5) with this design model.

You may additionally model other circuit non-idealities like switch non-linearity, clock jitter, quantizer non-idealities, etc. A behavioral simulation model like **SIMSIDES** is usually used to verify system level performance of such designs [6].

3 Final Report

Submit your neatly typed report in a two-column IEEE transactions format [7]. Show neatly drawn schematics and block diagrams. You may download the Visio schematic symbols from the course website [8]. Provide relevant references in your report. Show the modulator overall ADC performance (peak SNR/SNDR, dynamic range, THD, etc.) in a neatly tabulated manner along with the conclusion.

References

- [1] A 24-bit, 192 kHz Multi-bit Audio ADC: CS5430 Datasheet, Wesbite, Cirrus Logic, 2008.
- [2] Audio Conversion Systems Noise Calculations and Requirements, App. note AN263, Cirrus Logic, 2008.
- [3] R. Schreier, J. Silva, J. Steensgaard, G. C. Temes, "Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits," *IEEE TCAS-I*, vol. 52, no. 11, pp. 2358-2368, Nov. 2005.
- [4] K. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," *Designer's Guide Community* [Online].
- [5] K. Kundert, "Device Noise Simulation of Delta-Sigma Modulators," *Designer's Guide Community* [Online].
- [6] SIMSIDES, SIMulink-based SIGma-DELta Simulator , University of Seville. Available [Online].
- [7] IEEE Transactions Templates. Available [Online].
- [8] Visio Schematic Symbols. Available [Online].