On The Implementation of Input-Feedforward Delta–Sigma Modulators

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Abstract—This brief addresses some practical issues on the implementation of the input-feedforward delta–sigma modulators. First, the timing constraint imposed by the input-feedforward path is identified and a possible method to relax the constraint is proposed. Second, the drawbacks of the analog adder needed before the quantizer are explained and a method to eliminate the adder is proposed.

Index Terms—Analog-to-digital, delta–sigma($\Delta\Sigma$), input-feedforward, oversampling.

Fig. 1. General input-feedforward $\Delta\Sigma$ modulator.

I. INTRODUCTION

THE increasing demand for higher bandwidth and higher resolution *analog-to-digital converters* (ADCs) suitable for the deep submicrometer CMOS technologies has fueled the development of more *efficient delta–sigma* ($\Delta\Sigma$) modulator topologies for low *oversampling ratios* (OSRs) and low supply voltages. One of the problems of a low OSR is the low attenuation of nonidealities generated at the output of the integrator, such as opamp distortion, which can be as low as 8 dB for an OSR of 8 [1]. Therefore, to achieve high *signal-to-noise-plus-distortion ratio* (SNDR), the first opamp must have high linearity. This is further complicated by the low supply voltage which imposes severe limitations on the headroom of the opamps.

The input-feedforward path in $\Delta\Sigma$ modulators is a method of relaxing the requirements on analog blocks [1]. It is illustrated in Fig. 1 for a general loop filter $H(z)$.

Analysis of the linearized system shows that the $\Delta\Sigma$ modulator with the input-feedforward path has the following *signal transfer function* (STF) and *noise transfer function* (NTF) assuming an ideal *digital-to-analog converter* (DAC)

$$\text{STF} = \frac{y}{x} = 1 \tag{1}$$

$$\text{NTF} = \frac{y}{q} = \frac{1}{1 + H(z)} \tag{2}$$

where q is the quantization noise from the ADC. Also, the input to the loop filter is

$$u = -\frac{1}{1 + H(z)}q. \tag{3}$$

Note that the loop filter $H(z)$ has to process the quantization noise only. On the other hand, without the input feedforward, the loop filter has to process the quantization noise in addition to the input signal. The removal of the input signal component reduces the swing at the internal nodes of the modulator which relaxes the headroom requirements, and allows for more efficient opamp architectures to be used. Also, distortion becomes independent of the input signal, which relaxes linearity requirements [1]. However, the input-feedforward path presents a couple of complications, namely the reduced processing time and the analog adder at the quantizer input.

It is important to note that a unity STF does not guarantee improved headroom and linearity requirements. For example, a second-order modulator constructed from two nondelaying integrators results in a unity STF [2]. It can be also shown that the output of both integrators contain an unshaped input-signal component.

The outline of this brief is as follows. Section II explains the origin of the timing constraint introduced by the input-feedforward path. Section III proposes a method to eliminate the timing constraint. Section IV discusses the practical issues of the summation at the quantizer input and proposes a method to eliminate it. Finally, conclusions are presented in Section V.

II. INPUT-FEEDFORWARD TIMING ISSUES

The input-feedforward path imposes a timing constraint that complicates its implementation, especially for high-speed multi-bit modulators. The constraint is due to the delay free loop starting from the input, through the input-feedforward path to the quantizer, and finally through the DAC back to the loop filter input. Although it is still possible to implement using switched-capacitor circuits [1], it limits the speed of the modulator. The problem becomes worse with the use of a multi-bit quantizer with *dynamic element matching* (DEM) algorithms. To understand where the speed limitation comes from, a typical first-order switched-capacitor $\Delta\Sigma$ modulator implementation
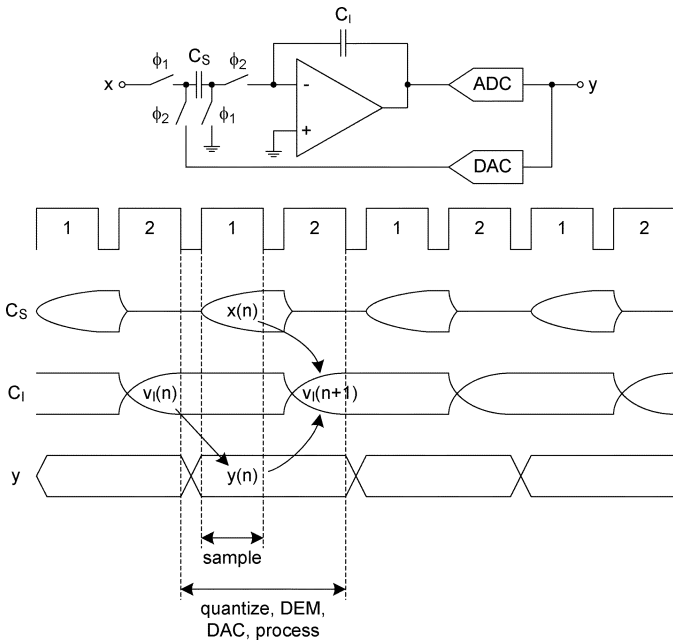
Fig. 2. First-order switched-capacitor $\Delta\Sigma$ modulator without input feedforward and its timing diagram.
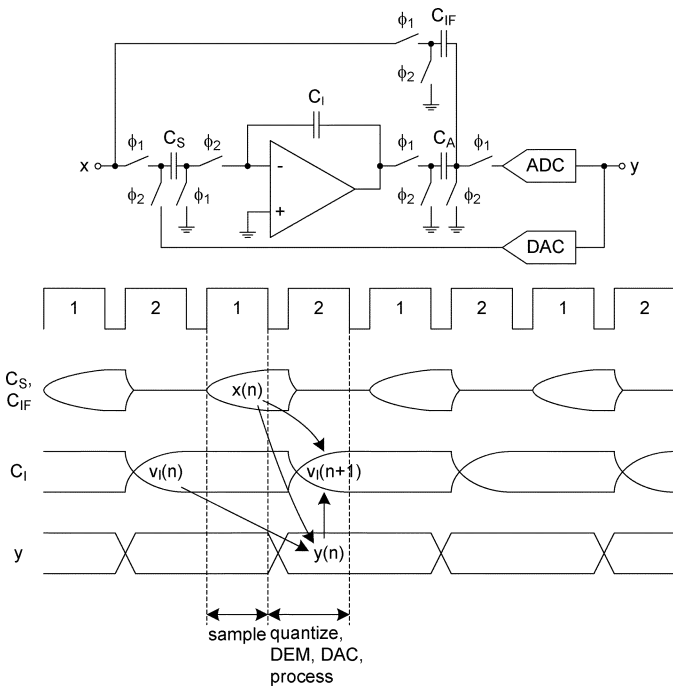

Fig. 3. First-order switched-capacitor $\Delta\Sigma$ modulator with input feedforward and its timing diagram.

(without input feedforward) and its timing diagram are shown in Fig. 2.

Also, a typical first-order switched-capacitor $\Delta\Sigma$ modulator implementation with input feedforward and its timing diagram are shown in Fig. 3.

The *process* operation refers to the subtraction and integration functions in the modulator and can not start before the beginning of phase 2. This is not explicitly indicated in the timing diagram

to emphasize the fact that quantization, DEM, and DAC can extend into phase 2.

Without input feedforward, the quantizer only needs $v_I(n)$ to generate the output y(n), where $v_I(n)$ is the voltage at the integrator output. Since $v_I(n)$ is available at the end of the previous ϕ_2 and held by the integrator throughout ϕ_1, there is an entire phase (ϕ_1) to perform quantization, DEM, and DAC. Therefore, the entire ϕ_2 can be allocated for the integrator to settle to the required accuracy as shown in Fig. 2.

On the other hand, with input feedforward, the quantizer needs $v_I(n)$ and x(n) to generate y(n), where y(n) is needed during the same period by the integrator. Since x(n) is only available at the end of ϕ_1, there is about one phase to perform quantization, DEM, DAC, and processing as shown in Fig. 3. This reduces the time available for the opamp to settle to the required accuracy. For example, consider a $\Delta\Sigma$ modulator with a 4-bit internal quantizer and with 100-MHz sampling frequency. This gives the input-feedforward modulator about 5 ns to perform quantization, DEM, DAC, and processing. Most high-speed $\Delta\Sigma$ modulators utilize *data weighted averaging* (DWA) to linearize their DAC [3]. Also, a well designed DWA only adds a shifter into the modulator loop; and the pointer update logic is done outside the loop [4]. A typical 4-bit barrel shifter in 0.18-μm CMOS technology requires 0.9 ns.[1] Therefore, DWA alone requires about 20% of the available time; this means that the opamp requires more power to settle to the same accuracy.

One method to relax the timing constraint is to sample the input on the feedforward capacitor C_{IF} one phase earlier than the sampling capacitor C_S.[2] Therefore, the quantizer inputs are available at the end of the previous ϕ_2. This gives the topology of Fig. 3 a full period to perform the required operations just like the topology of Fig. 2. Mathematically, sampling C_{IF} one phase earlier than C_S is equivalent to multiplying the feedforward coefficient by half a unit delay. To investigate the effect of this delay on the modulator, the linearized system of Fig. 1 (with $z^{-1/2}$ in the feedforward path) for a pure differentiator type NTFs of order L is used, and the analysis revels the following results:

$$
\begin{aligned}
H(z) &= \text{NTF}^{-1} - 1 \\
&= (1 - z^{-1})^{-L} - 1 \tag{4} \\
y &= \left(1 - \left(1 - z^{-1/2}\right)\text{NTF}\right)x + \text{NTF}q \\
&= \left(1 - \left(1 - z^{-1/2}\right)(1 - z^{-1})^L\right)x + (1 - z^{-1})^L q \tag{5} \\
u &= \left(\left(1 - z^{-1/2}\right)\text{NTF}\right)x - \text{NTF}q \\
&= \left(\left(1 - z^{-1/2}\right)(1 - z^{-1})^L\right)x - (1 - z^{-1})^L q. \tag{6}
\end{aligned}
$$

There are two important observations: there is a signal component at the input of the loop filter and the STF is modified.

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[1]The 4-bit barrel shifter was coded in Verilog and synthesized using Synopsys with the standard 0.18-μm CMOS digital library provided by the Canadian Microelectronics Corporation (CMC). The 0.9-ns time does not include the buffers required to drive the switches.

[2]It is also possible to feedback a past value of the output $y(n - 1)$ to the modulator, effectively adding a delay to the feedback path. This would change the poles of the STF and NTF and is undesirable.

Fig. 5. Relaxed timing input-feedforward architecture using only the sampling capacitors.
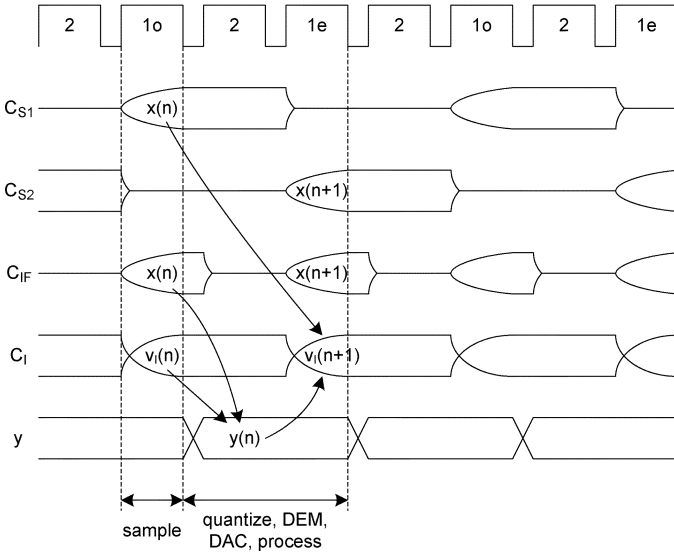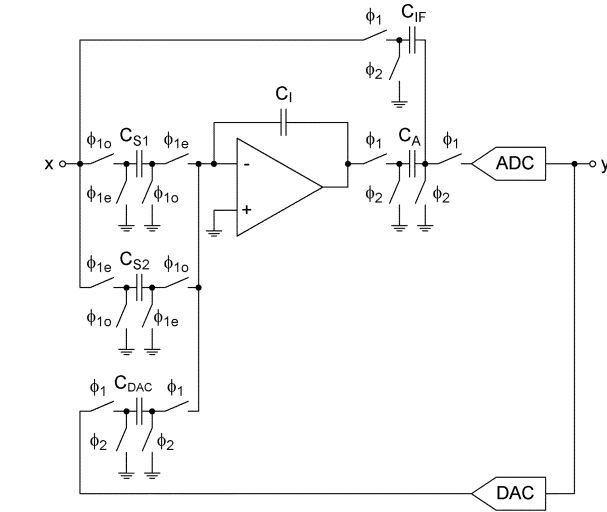

Fig. 4. Proposed relaxed timing input-feedforward architecture and its timing diagram.

The input signal component into the loop filter is noise shaped. Therefore, the signal component at the output of the integrators is small and usually not a problem. This means that headroom and linearity requirements are still relaxed. The modified STF has a unity gain at dc and larger gain at half the sampling frequency (fs/2). The high-frequency boost makes this solution undesirable because it represents a potential instability problem.

III. RELAXED TIMING INPUT-FEEDFORWARD ARCHITECTURE

To relax the timing constraint presented by the input-feedforward path, it is desirable to extend the time available for quantization, DEM, and DAC. A method to accomplish this is to sample the input one phase earlier than required, hold it for one phase, and process it during a third phase. During the holding phase, the quantizer can be strobed since both inputs $x(n)$ and $v_I(n)$ are available for the duration of the phase. The process implies that the sampling capacitor is busy for three phases; on
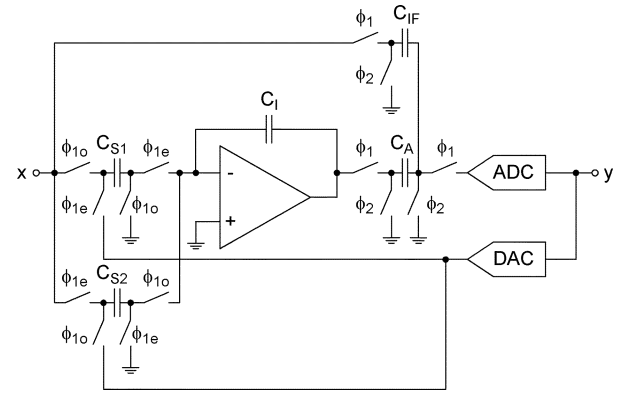
the other hand, one sample must be taken per period. This conflict can be resolved by introducing another sampling capacitor. Effectively, there are two sampling capacitors and each one samples the input once every two periods. One capacitor (C_{S1}) samples during odd phases (ϕ_{1o}) and another capacitor (C_{S2}) samples during even phases (ϕ_{1e}) as shown in Fig. 4. Note that the process (subtract and integrate) operation can not start before the beginning of phase 1.

The cost of the proposed solution is an increase in area due to the second sampling capacitor. The proposed implementation in Fig. 4 uses a separate capacitor (C_{DAC}) to feedback the quantized signal. It is also possible to use the sampling capacitors to feedback the quantized signal as shown in Fig. 5. The implementation of Fig. 4 allows easy scaling of the feedback signal relative to the input signal and it draws signal independent current from voltage reference supply [5]. The implementation of Fig. 5 has power saving advantage because there are less kT/C noise and larger feedback factor. Another important issue to consider when comparing the two implementations is the sampling capacitors mismatch.

The mismatch issue was investigated using ideal building blocks in Spectre. A third-order input-feedforward $\Delta\Sigma$ modulator with a 3-bit internal quantizer and an OSR of 64 was used for the investigation. The traditional implementation (Fig. 3) achieves a *signal-to-noise ratio* (SNR) of 119 dB but as mentioned above, has a difficult timing requirement. With ideal capacitor matching, the implementations of Figs. 4 and 5 also both achieve 119-dB performance but have much relaxed timing requirements. However, when capacitor mismatch of 0.1% is introduced, the implementation of Fig. 4 maintains a performance of 118 dB while that of Fig. 5 reduces significantly to only 81 dB. The reason for the large degradation in SNR for the circuit of Fig. 5 is due to large out-of-band quantization noise near fs/2 being aliased back in-band which is a similar problem that occurs in double sample modulators [6]. This effect does not occur in the circuit of Fig. 4 since only the input signal is double sampled and the input signal likely has little signal energy near fs/2. However, since the circuit of Fig. 5 does have better kT/C noise performance than that of Fig. 4, if one chooses to make use of the Fig. 5 circuit, the noise folding problem can be mitigated by adding an extra zero at fs/2 into the noise transfer function [7]. In addition, capacitor mismatch
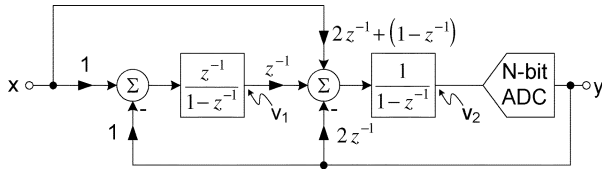
Fig. 6.   Proposed CIFB-CIF topology.

Fig. 7.   Switched-capacitor implementation of CIFB-CIF.

in the circuits of Figs. 4 and 5 results in an out-of-band tone to occur near $fs/2$. Fortunately, this tone is of little consequence as it will be removed by the decimation filter.

IV. INPUT-FEEDFORWARD TOPOLOGIES WITHOUT THE ADDER AT THE QUANTIZER INPUT

The summation at the quantizer input creates another complication for input-feedforward $\Delta\Sigma$ modulators. The disadvantage is the increased circuit complexity and power dissipation. In some implementations, this adder is done passively. However this approach reduces the signal level into the quantizer which can also result in a power increase since smaller quantization levels must now be resolved.

The *cascade of integrators with distributed feedback* (CIFB) topology can be modified to eliminate the adder at the quantizer input. Fig. 6 illustrates the proposed *CIFB* topology with *capacitive input feedforward* (CIFB-CIF) as shown for a second-order modulator. The $(1 - z^{-1})$ term in the feedforward path can be implemented by a simple capacitor.

Analysis of the linearized system leads to the following results:

$$\text{STF} = \frac{y}{x} = 1 \tag{7}$$

$$\text{NTF} = \frac{y}{q} = (1 - z^{-1})^2 \tag{8}$$

$$v_1 = -z^{-1}(1 - z^{-1})q \tag{9}$$

$$v_2 = x - z^{-1}(2 - z^{-1})q \tag{10}$$

where q is the quantization noise from the ADC. The STF exhibits an all-pass response and the NTF provides a second-order pure differentiator type high-pass response. Signal v_1 is free of the input-signal while v_2 contains a signal component. Therefore, unlike the CIFB topology, when input feedforward is used, the output of the second integrator contains input signal. However, any nonidealities at this point are second-order noise shaped when referred back to the input and their effects are less important, which is even more significant if a higher order modulator is used.

The CIFB-CIF model in Fig. 6 can be implemented using switched-capacitor circuits as shown in Fig. 7 in the single-ended form for simplicity. The negative capacitor can be easily implemented in a fully differential circuit.

The CIFB-CIF topology was simulated using MATLAB and Simulink. A sample output spectrum including opamp third-order distortion in both opamps corresponding to 1% third-order harmonic distortion for a full scale signal is shown in Fig. 8. There is no harmonic components in the output spectrum with the input-feedforward path $\left(2z^{-1} + (1 - z^{-1})\right)$ as shown in (a). However, with the input-feedforward path removed, third-harmonic signal appears at the output as shown in (b). The effect of
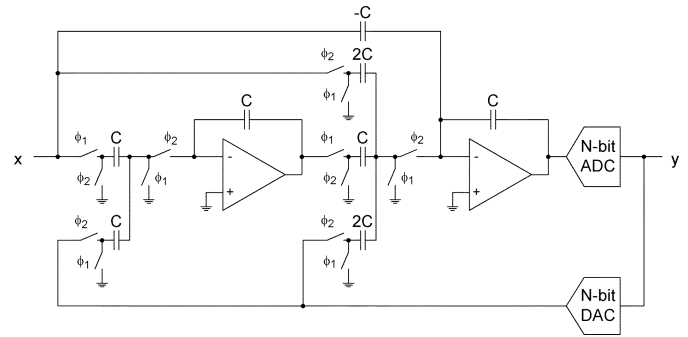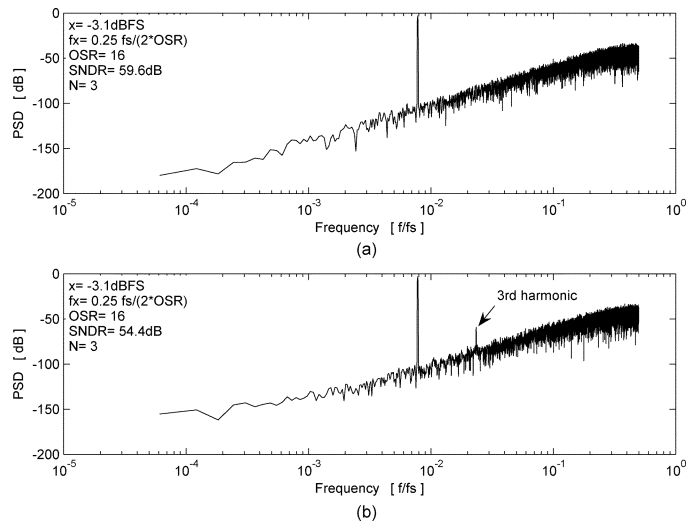

Fig. 8.   Sample output spectrum: (a) with input feedforward, and (b) without input feedforward.
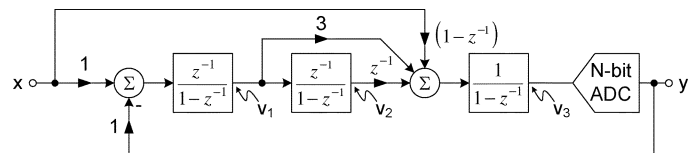

Fig. 9.   Proposed CIFF-CIF topology.

capacitor mismatch in the CIFB-CIF topology was investigated using Monte Carlo analysis in MATLAB. Mismatches have the same effect on the SNR for both CIFB and CIFB-CIF topologies. Therefore, the new topology has the same sensitivity to component mismatches as the CIFB.

The capacitive feedforward concept can be extended to the *cascade of integrators with weighted feedforward summation* (CIFF) topology. Unfortunately, the classical CIFF topology requires an adder before the quantizer to perform the weighted feedforward summation. Therefore, using the capacitive feedforward technique is not very helpful. However, a modified CIFF topology that eliminates this adder, except for the input-feedforward adder, was presented in [3]. The modified *CIFF* topology with *capacitive input feedforward* (CIFF-CIF) is shown for a third-order modulator in Fig. 9.

The STF exhibits an all-pass response and the NTF provides a third-order pure differentiator type high-pass response. Sig-

nals v_1 and v_2 are free of the input-signal while v_3 contains a signal component. As pointed out earlier, any nonidealities at the output of the third integrator are less important because they are third-order noise shaped when referred back to the input.

V. CONCLUSION

Input-feedforward modulators are attractive for implementation in low OSR and low supply voltage environment. However, the input-feedforward path introduces a timing constraint that limits its speed. A technique to relax the timing constraint was proposed. Also, a method to eliminate the adder at the quantizer input was proposed for CIFB and CIFF topologies. The capacitive-input-feedforward method reduces circuit complexity and power consumption by eliminating the problematic adder while maintaining low distortion and low signal swing performance at the important nodes.

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