

# A 0.6-V 82-dB Delta-Sigma Audio ADC Using Switched-RC Integrators

Gil-Cho Ahn, *Student Member, IEEE*, Dong-Young Chang, *Member, IEEE*, Matthew E. Brown, *Member, IEEE*, Naoto Ozaki, Hiroshi Youra, Ken Yamamura, Koichi Hamashita, Kaoru Takasuka, *Member, IEEE*, Gábor C. Temes, *Life Fellow, IEEE*, and Un-Ku Moon, *Senior Member, IEEE*

**Abstract**—A 0.6-V 2-2 cascaded audio delta-sigma ADC is described. It uses a resistor-based sampling technique which achieves high linearity and low-voltage operation without subjecting the devices to large terminal voltages. A low-distortion feed-forward topology combined with nonlinear local feedback results in enhanced linearity by reducing the sensitivity to opamp distortion, and allows increased input amplitude, resulting in higher SNDR. The modulator achieves 82-dB dynamic range and 81-dB peak SNDR in the A-weighted audio signal bandwidth with an OSR of 64. The total power consumption of the modulator is 1 mW from a 0.6-V supply. The prototype occupies 2.9 mm<sup>2</sup> using a 0.35- $\mu$ m CMOS technology.

**Index Terms**—Delta-sigma ADC, low voltage, switched-RC.

## I. INTRODUCTION

CMOS technology is continuously scaled down to achieve low-cost, high-density, low-power and high-speed digital systems. With the ever-increasing demand for portable devices used in applications such as wireless communication, mobile computing, consumer electronics, etc., the scaling down of the CMOS process to deep-submicron dimensions becomes even more important. However, this downscaling also requires similar shrinking of the supply voltage to insure device reliability [1]. The International Technology Roadmap for Semiconductors [2] predicts a maximum supply voltage equal to 0.8 V for 2007, and only 0.7 V for 2010 for state-of-the-art CMOS digital technology. This aggressive supply scaling requires low-voltage operation for the on-chip interface circuitry (analog-to-digital and digital-to-analog data converters) as well.

Low-voltage operation of ADCs poses three major challenges. First, the floating switches required in conventional switched-capacitor implementations are not operational for very low supply voltages. Since the threshold voltage is not proportionally scaled with supply voltage, the floating switch severely limits the signal range. Furthermore, excess gate overdrive voltage of the floating switch may violate the reliability constraints of the technology. This consideration prevents the use of voltage multiplication to drive these switches. Second,

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G.-C. Ahn, D.-Y. Chang, M. E. Brown, G. C. Temes, and U. Moon are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331-5501 USA (e-mail: moon@eecs.oregonstate.edu).

N. Ozaki, H. Youra, K. Yamamura, K. Hamashita, and K. Takasuka are with Asahi Kasei Microsystems, Atsugi, Kanagawa 243-0021, Japan.

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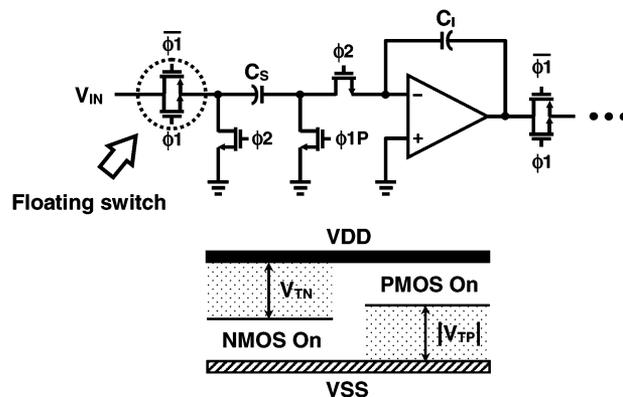


Fig. 1. Conventional switched-capacitor integrator with the floating switches.

device noise due to both sampling switches and amplifiers poses a difficult design challenge at low supply voltage if high SNR must be achieved. Finally, amplifier distortion also limits the overall performance. In low-distortion applications, signals can be scaled down at the expense of lower signal power. However, with sub-1-V supply, the conflicting requirements of large signal swing and low distortion make a challenging design task. The main purpose of this work is to introduce low-voltage design techniques that enable high-performance analog circuit operation in deep-submicron processes. Architectural and circuit design techniques are presented for switched-RC circuits operating under very low supply voltage conditions. To demonstrate the proposed techniques, a wide-dynamic-range audio delta-sigma ADC with sub-1-V supply and low (1 mW) power consumption is designed. While the realization is demonstrated in a 0.35- $\mu$ m CMOS technology, the key principles of the proposed techniques, which depend on the relative voltages of transistor threshold and supply, are directly migratable to finer linewidth submicron CMOS processes.

Section II describes the problems associated with floating switches in low-voltage switched-capacitor (SC) circuits, and the proposed solution using switched-RC branches. Section III discusses the architecture chosen for the audio ADC, and Section IV describes the details of the circuit implementation. The experimental results are shown in Section V. Finally, Section VI summarizes the conclusions drawn from the project.

## II. SWITCHED-RC TECHNIQUE

The switched-capacitor (SC) technique provides an accurate and robust way of designing CMOS analog circuits. However, the realization of a low-voltage SC circuit becomes difficult, since

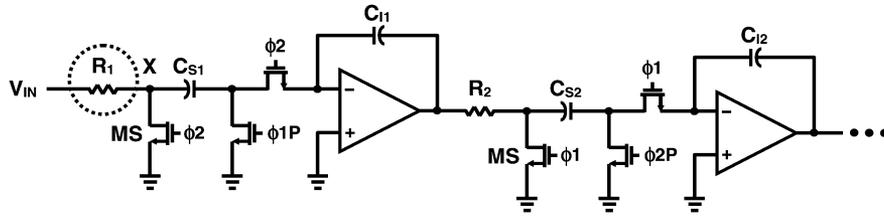


Fig. 2. Low-voltage integrator with switched-RC input branch.

the floating switches required in conventional SC circuits are not operational for very low supply voltages. Fig. 1 shows a typical SC integrator with its floating input and output switches. Limited gate voltage under low supply restricts the operating range of these switches. For example, the NMOS switches are “on” only when the input signal is lower than  $V_{DD} - V_{TN}$ . Similarly, the PMOS switches are “on” only when the input signal is higher than  $|V_{TP}|$ . Both transistors turn off in the mid-input signal range. For proper operation, the gate overdrive voltage must be larger than the sum of the CMOS switch threshold voltages and the input signal amplitude. Thus, higher gate overdrive voltage has been used in previous low-voltage SC circuits, using global clock boosting or bootstrapping by voltage multiplication for the clock signals [1], [3], [4]. However, both techniques require extra circuitry and need careful design to avoid reliability problems. There are several circuit techniques which are fully compatible with low-voltage submicron CMOS processes, such as switched-opamps (SO) [5]–[9] and the opamp-reset switching technique (ORST) [10]–[12]. However, SO circuits face a tradeoff between speed and accuracy due to slow transients, while ORST stages have higher power consumption and settling issues due to unity gain feedback during the reset phase.

In this work, a different solution based on the switched-RC technique is proposed, and is applied to the design of an audio delta-sigma ADC. The basic concept is illustrated in Fig. 2. As shown, the input SC branch of the conventional structure is replaced by a switched-RC branch, in which the floating switch of the conventional integrator is replaced by a resistor  $R_1$ . This modification results in two advantages. First, it obviates the need for the floating switch, and second, the linearity of the input sampling is improved. The operation of this circuit is as follows. During the  $\phi_1$  phase, the signal is sampled into the capacitor  $C_{S1}$  through resistor  $R_1$ . During the following  $\phi_2$  phase, the signal charge is transferred to the integrating capacitor  $C_{I1}$  by connecting the bottom plate of  $C_{S1}$  to ground through switch  $MS$ . During this phase, the voltage  $V_X$  at node  $X$  is determined by the ratio of the ON resistance  $R_{ON}$  of the  $MS$  switch and the resistor  $R_1$

$$V_X \left( n + \frac{1}{2} \right) = \frac{R_{ON}}{R_1 + R_{ON}} V_{IN} \left( n + \frac{1}{2} \right). \quad (1)$$

The output voltage of the integrator can be found from charge conservation as

$$V_{OUT} \left( n + \frac{1}{2} \right) = V_{OUT}(n) + \frac{C_{S1}}{C_{I1}} V_{IN}(n) - \frac{C_{S1}}{C_{I1}} \frac{R_{ON}}{R_1 + R_{ON}} V_{IN} \left( n + \frac{1}{2} \right). \quad (2)$$

The gain error due to the ON resistance of switch  $MS$  is the last term in (2). For sufficiently high oversampling ratio (OSR),  $V_{IN}(n + (1/2))$  will be very close to  $V_{IN}(n)$ , and the error can then be approximated by

$$\text{Gain Error} = \frac{C_{S1}}{C_{I1}} \frac{R_{ON}}{R_1 + R_{ON}}. \quad (3)$$

Note that the gain error introduced by the nonideal ground at node  $X$  does not necessarily result in large distortion, as shown next. In (3),  $R_{ON}$  is the only nonlinear term, and hence the sole source of nonlinearity. Its value is given in (4), which shows that  $R_{ON}$  is a function of  $V_{DS} = V_X$ :

$$R_{ON} = \frac{1}{\mu_n C_{OX} (W/L) [(V_{GS} - |V_{TH}|) - V_{DS}]}. \quad (4)$$

Even though  $V_X$  changes with the input signal, the signal variation at node  $X$  is attenuated by the ratio of  $R_1$  and  $R_{ON}$  [see (1)], and hence, the change in  $R_{ON}$  is small compared to that of a floating switch. Both the nonlinearity of the input sampling and the gain error can be reduced by making the linear resistor  $R_1$  much larger than the variable ON resistance of the reset switch  $MS$ . However, there is a tradeoff. Larger  $R_1$  results in improved gain accuracy and lower distortion during the  $\phi_2$  phase, but during the  $\phi_1$  phase, a large  $R_1 C_{S1}$  time constant degrades the sampling accuracy. Thus,  $R_1$  should be small enough to satisfy the settling requirement during the sampling phase.

The gain of the opamp in a switched-RC (SRC) integrator changes significantly between the phases. During the  $\phi_1$  phase, the amplifier drives the resistive load  $R_2$ , which results in a low DC gain due to the low load impedance. However, during this reset phase, the charge stored in  $C_{I1}$  will be preserved, and the output voltage of the integrator will be recovered in the following  $\phi_2$  phase, when the gain of amplifier returns to its high value as its resistive load is removed. The virtual ground voltage therefore also returns to its low value needed for the charge transfer. Hence, the effective DC gain of the amplifier in an SRC integrator can be the same as in a conventional SC one. Note also that the voltage between any two nodes is always less than the supply voltage, and therefore this technique is free from device reliability problems.

As illustrated in Fig. 2, the phasing of the clock signals in adjacent SRC integrators must be shifted. Thus, there is a  $T/2$  delay between the input and the output of the integrator, where  $T = 1/f_{clk}$  is the clock period.

### III. MODULATOR ARCHITECTURE

As discussed in Section I, there are three main problems in low-voltage analog IC design. A circuit solution is proposed in



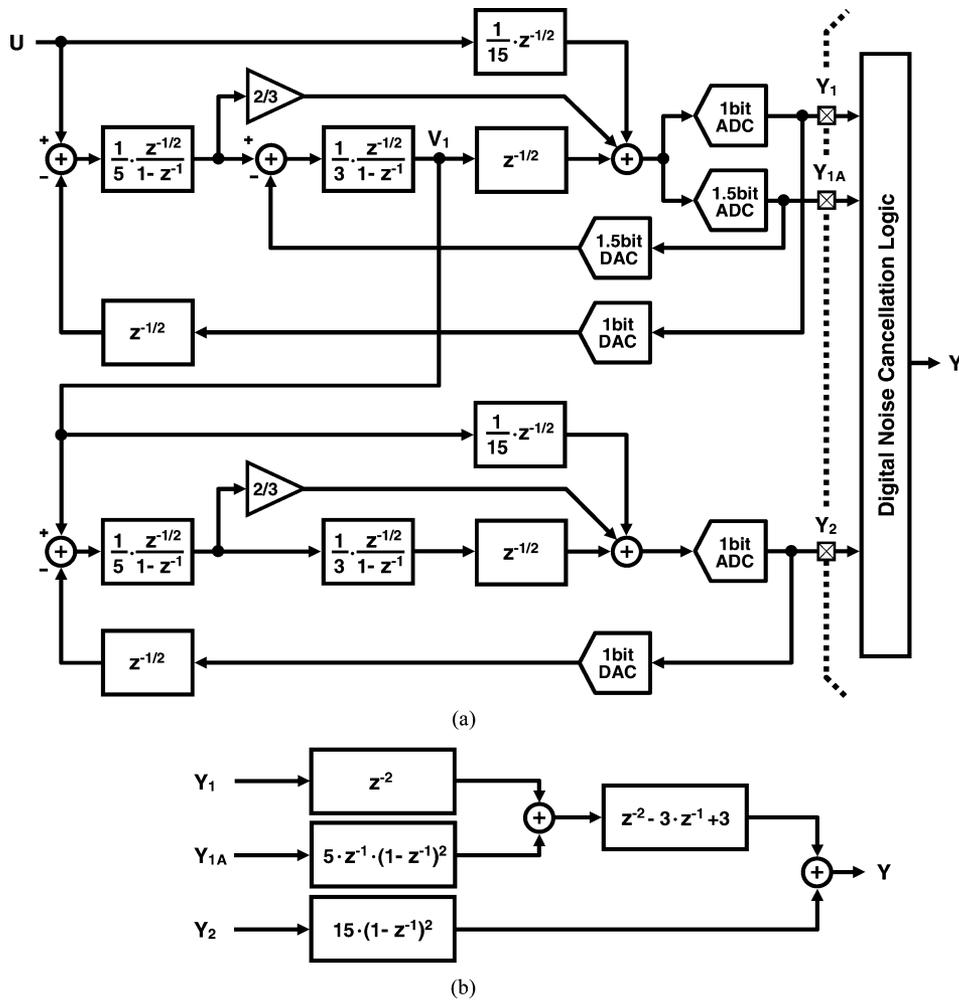


Fig. 4. (a) Block diagram of two-stage cascaded delta-sigma modulator. (b) Digital noise cancellation logic.

matching indicate higher than 100-dB SFDR of the complete converter. More than 1.5-dB improvement in the permissible peak input signal due to local feedback is also observed in these simulations.

#### IV. CIRCUIT IMPLEMENTATION

While the principle of the SRC circuit has been described in Section II, its actual implementation in our ADC is somewhat different, since the input branches are also used for common-mode adjustments and feedback. The implemented circuits will be discussed next.

##### A. Split Switched-RC Input Branch

In a low-voltage integrator, it is desirable to set the common-mode (CM) level of the input and output at the middle of the supply voltage, i.e.,  $V_{CM} = (V_{DD} + V_{SS})/2$ , to maximize signal swing. At the same time, any DC bias voltage connected to the sampling capacitors must be close to  $V_{DD}$  or  $V_{SS}$  in order to avoid any floating switching problem. For this reason, two different input common-mode levels were applied to the integrator during the sampling and the integrating phases. Such use of two different input CM voltages resulted in a large amount

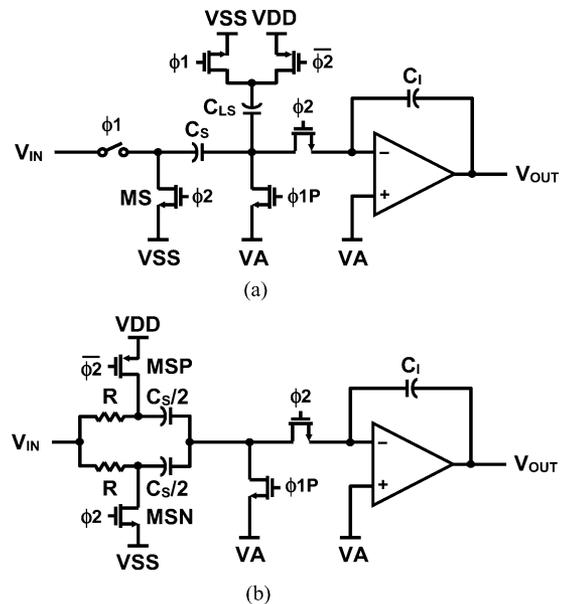


Fig. 5. (a) Traditional low-voltage switched-capacitor integrator. (b) Low-voltage integrator with split switched-RC technique.

of common-mode charge injection. Thus, the input or inter-stage branches of all integrators should also perform a level

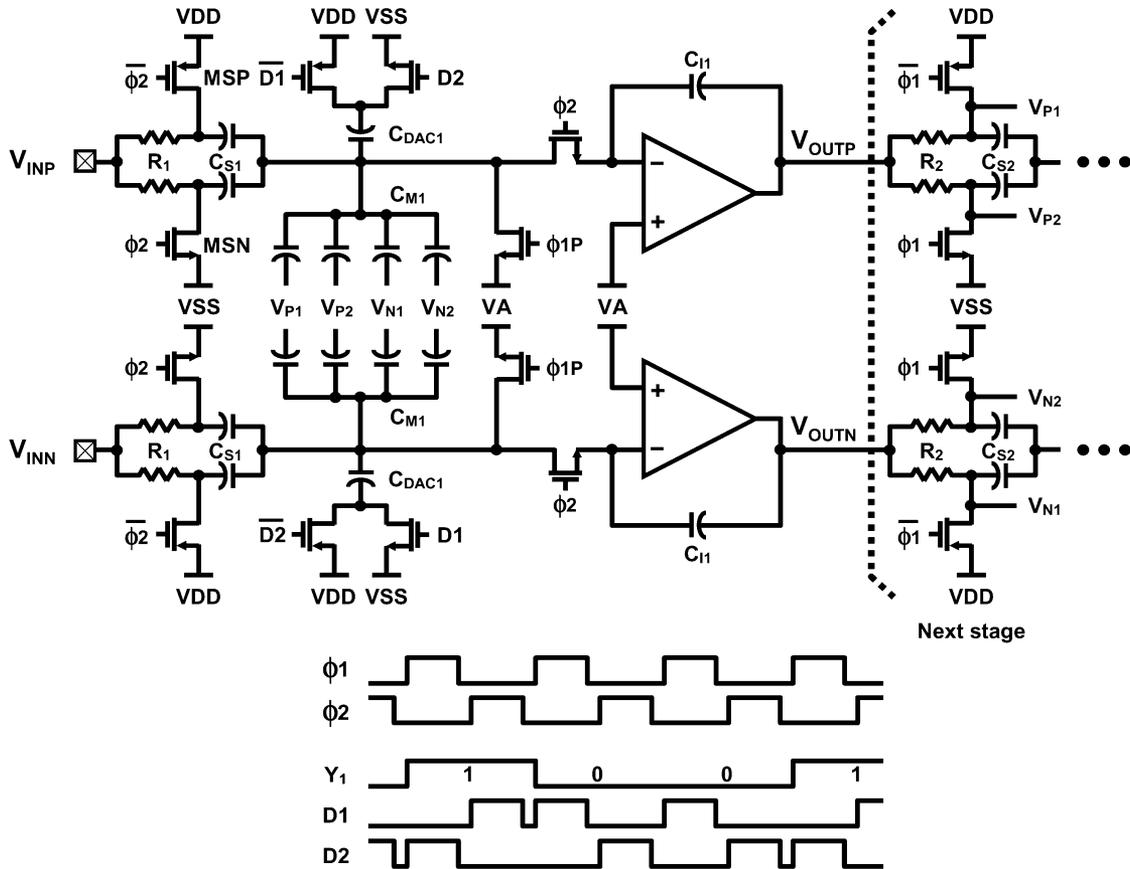


Fig. 6. Schematic of pseudo-differential low-voltage integrator with switched-RC technique.

shifting operation, in addition to sampling and transfer/amplification of the input signal. Fig. 5(a) shows an earlier implementation of this level shifting in a low-voltage SC integrator [7]. A level-shifting capacitor  $C_{LS}$  is used to cancel the common-mode charge injection, by providing an opposite polarity charge. However, this added SC branch adds more  $kT/C$  noise and also increases the opamp noise gain.

In our implementation, a split input switched-RC branch is used to keep constant CM level of the integrator, as shown in Fig. 5(b). During the integrating phase, one half of the sampling capacitor is connected to  $V_{DD}$ , while the other half is connected to  $V_{SS}$ . This results in a constant input common-mode level of  $V_{DD}/2$  for the integrator during both phases, obviating the need for an additional level-shifting capacitor without any noise penalty.

### B. Pseudo-Differential Integrator Using Switched-RC Technique

Fig. 6 shows the complete schematic of a pseudo-differential integrator using the switched-RC technique, and an example timing diagram. Split switched-RC input branches are used to maintain a constant input common-mode voltage. The effective DAC reference voltage is doubled by alternating the connection of the DAC capacitors  $C_{DAC1}$  from  $V_{DD}$  to  $V_{SS}$  or *vice versa*, depending on the comparator's output. This helps to reduce the size of  $C_{DAC1}$  resulting in lower noise. This is because the input-referred  $kT/C$  noise due to  $C_{DAC1}$  is scaled by  $C_{S1}^2$ , and the opamp noise will be amplified by the ratio of  $C_{S1}$  and the total capacitance connected to the virtual ground node.

A pseudo-differential architecture is used to circumvent challenging design issues associated with low-voltage common-mode feedback circuit design. Capacitors  $C_{M1}$ s, connected to the switched-RC branches of the next stage, are used for the common-mode feedback. The basic operation of the switched-RC common-mode feedback is similar to that proposed for pseudo-differential circuits earlier in [16], except for the use of switched-RC branches. Fig. 7 shows the operation during two different phases of common-mode feedback loop formed with the following stage switched-RC branches. During  $\phi1$ , the desired output common-mode reference  $V_{CM}$  is sampled onto capacitors  $C_{M1}$  by connecting half of them to  $V_{DD}$  and the other half to  $V_{SS}$ . During the following  $\phi2$  phase, the difference between  $V_{CM}$  and the actual output common-mode voltage is fed to all opamp inputs, and integrated in both pseudo-differential paths. This forces the output CM of all opamps to  $V_{CM}$ .

Fig. 8 shows the complete schematic of the first-stage modulator, implemented in a pseudo-differential architecture. To insure less than  $-85$ -dB  $kT/C$  noise level, a total of 4.8-pF input sampling capacitance is used and 8-k $\Omega$   $R_1$  is used to guarantee linear input signal sampling. The 1.5-bit DAC needed for local feedback uses two capacitors  $C_{DAC2}$  to double the effective DAC reference voltage, each one acting as a 1-bit delay-free DAC. During the  $\phi2$  phase, each capacitor is charged to  $V_{DD}$  or  $V_{SS}$ . During the following  $\phi1$  phase, depending on the output ( $-1$ , 0, or 1) of the 1.5-bit local feedback quantizer, the voltage at the bottom plate of the  $C_{DAC2}$  capacitors will be changed. If output is " $-1$ ", then the capacitor earlier connected to  $V_{DD}$  will

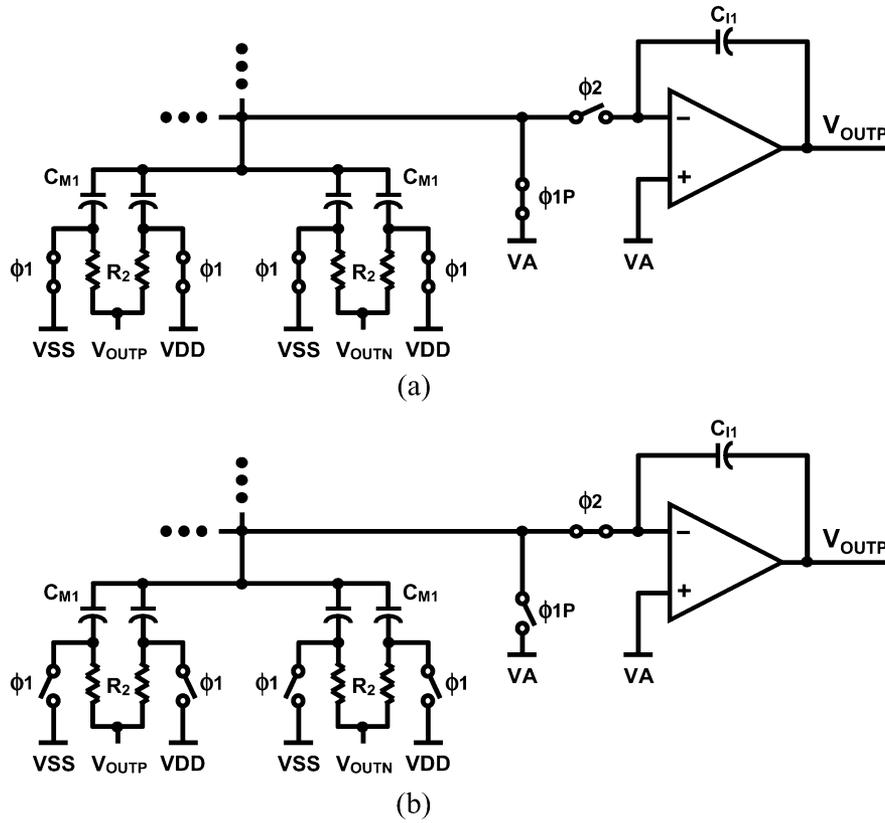


Fig. 7. Common-mode feedback with switched-RC technique. (a)  $\phi_1$  phase. (b)  $\phi_2$  phase.

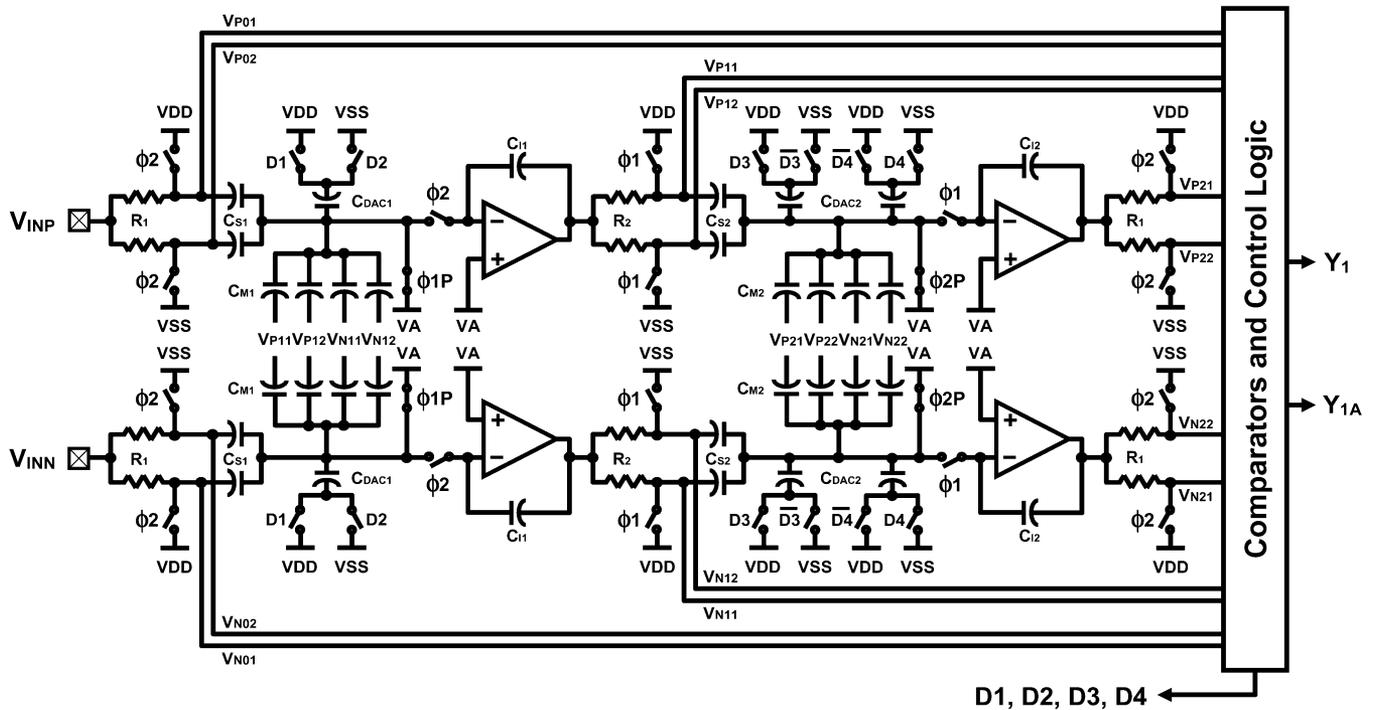


Fig. 8. First-stage delta-sigma modulator.

be reconnected to  $V_{SS}$ . If it is “1”, then the capacitor connected to  $V_{SS}$  will be switched to  $V_{DD}$ . However, if the quantizer output is “0”, then the connection of the  $C_{DAC2}$  capacitors will not be changed.

The gain coefficients of the feed-forward paths from the ADC input and from the output nodes of each integrator to the quantizer input are realized simply by scaling the capacitors in the comparators, as shown in Fig. 9. The switched-RC

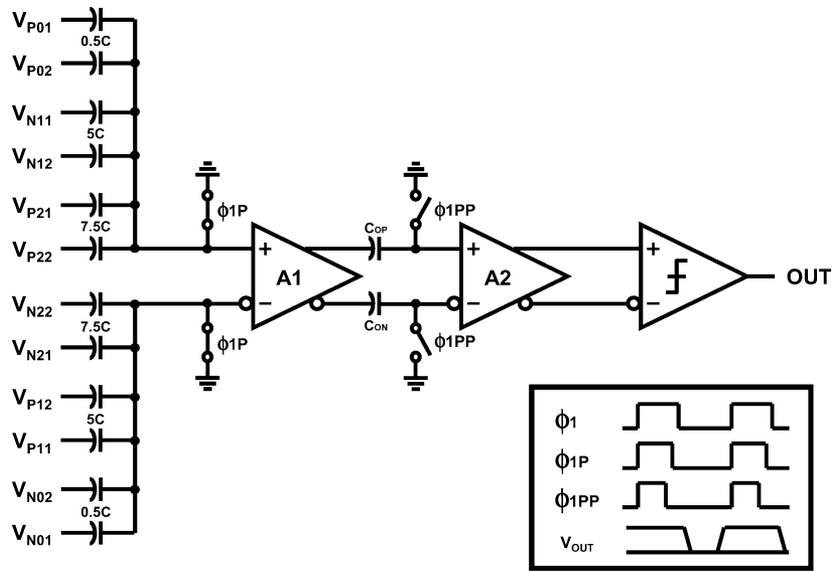


Fig. 9. Schematic of the comparator.

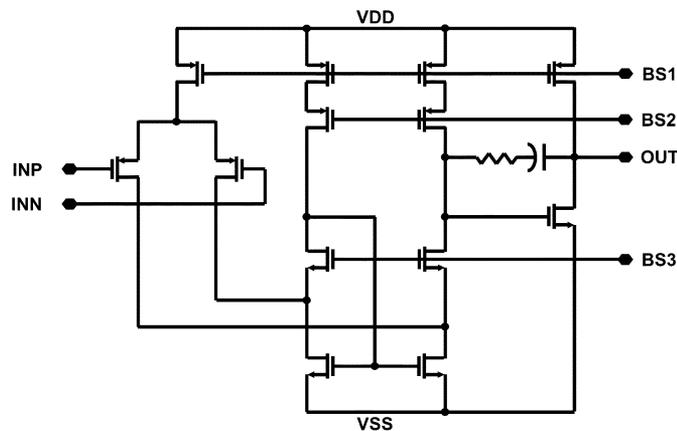


Fig. 10. Schematic of the amplifier.

output branches of the integrators are shared with the comparators' input sampling branches. Because of this, the input common-mode level of the comparators is also kept constant, together with the output CM level of the integrators.

Using a low-offset comparator is important to achieve a large signal range in low-voltage delta-sigma modulator design. Depending on the comparator offset, the center of the integrator output histogram can move out from the middle of the supply voltage range, resulting in overloading. The offset cancellation of the comparators is performed at the output of amplifier A1, while amplifier A2 is used as a preamplifier, to suppress the kickback from the latch. The output voltages  $V_{P21}$ ,  $V_{P22}$ ,  $V_{N21}$ , and  $V_{N22}$  of the second integrator drive the second stage of the MASH directly.

C. Amplifier Circuitry

To achieve high gain and large output swing, internally compensated two-stage amplifiers are used. Their circuit diagram is shown in Fig. 10. The amplifiers contain a folded-cascode first stage and a common-source second stage. The simulation

TABLE I  
SIMULATED PERFORMANCE OF THE AMPLIFIER

Power supply voltage	0.6 V
DC gain	60 dB
Unity gain frequency	10 MHz
Phase margin	65 °
Slew rate	10 V/ $\mu$ s

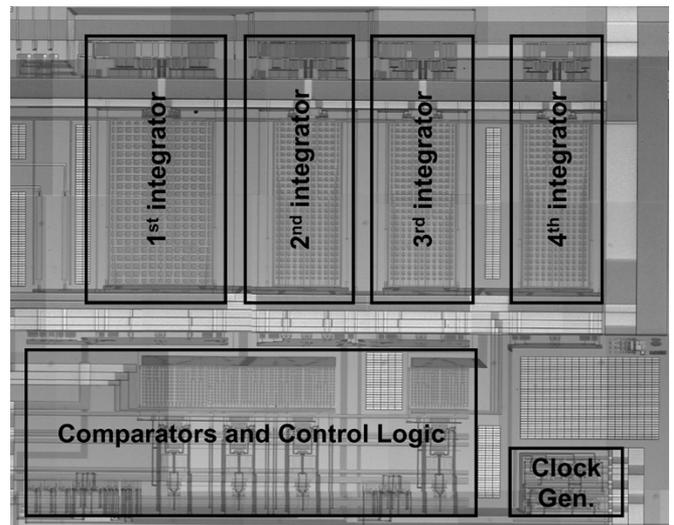


Fig. 11. Die photograph.

result shows more than 60-dB SFDR with full-scale output swing (0.8-V<sub>pp</sub> fully differential) under 0.6-V supply voltage. Though this amplifier provides relatively modest linearity under low-supply voltage operation, its nonlinearity error is reduced by the architectural features of the modulator, as explained in Section III. The main performance parameters of the opamp are given in Table I.

TABLE II  
PERFORMANCE SUMMARY

Power supply voltage	0.6 V
Signal bandwidth	24 kHz
Clock frequency	3.072 MHz
Oversampling ratio	64
Total power consumption	1 mW (including digital and I/O)
Input range	0.8 V <sub>pp</sub> (differential)
Peak SNR	77 dB @ BW = 24 kHz 78 dB @ BW = 20 kHz 81 dB @ BW = 20 kHz, A-weighted
Peak SNDR	77 dB @ BW = 24 kHz 78 dB @ BW = 20 kHz 81 dB @ BW = 20 kHz, A-weighted
Dynamic range	78 dB @ BW = 24 kHz 79 dB @ BW = 20 kHz 82 dB @ BW = 20 kHz, A-weighted
Active die area	1.8 X 1.6 mm <sup>2</sup>
Technology	0.35 $\mu$ m CMOS ( $V_{TN}=0.34$ V, $V_{TP}=-0.31$ V)

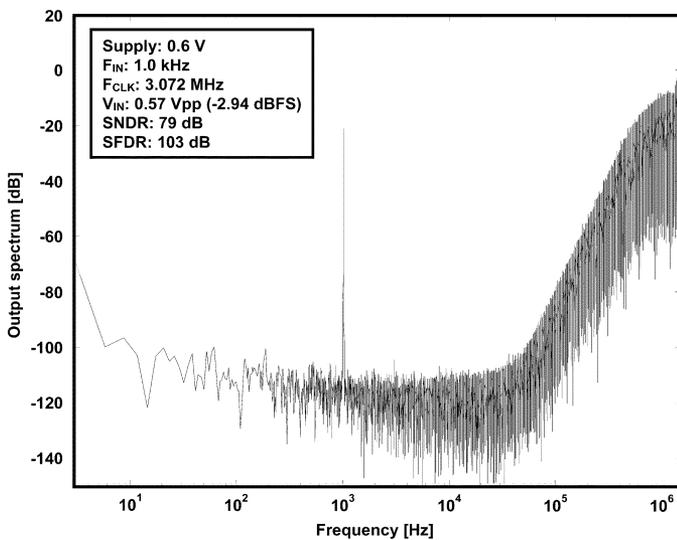


Fig. 12. Measured output spectrum.

### V. EXPERIMENTAL RESULTS

The prototype ADC was fabricated in a 0.35- $\mu$ m CMOS technology, with double-poly and triple-metal layers. Fig. 11 shows the die photograph of the prototype IC. The core area, excluding bonding pads, is  $1.8 \times 1.6$  mm<sup>2</sup>. Fig. 12 shows the measured power spectrum of the output for a 1-kHz 0.57-V peak-to-peak differential input sine wave, with a 0.6-V power supply. 79-dB SNDR and 103-dB SFDR is achieved over the audio band, largely due to the proposed switched-RC technique and the low-distortion loop. The SNDR versus input amplitude curve is illustrated in Fig. 13. This result indicates linear operation, up to a  $-1$ -dBFS input level. The measured performance is summarized in Table II. In the A-weighted audio band, the prototype achieves 81-dB peak SNDR and 82-dB dynamic range with a 0.6-V supply voltage and 1-mW

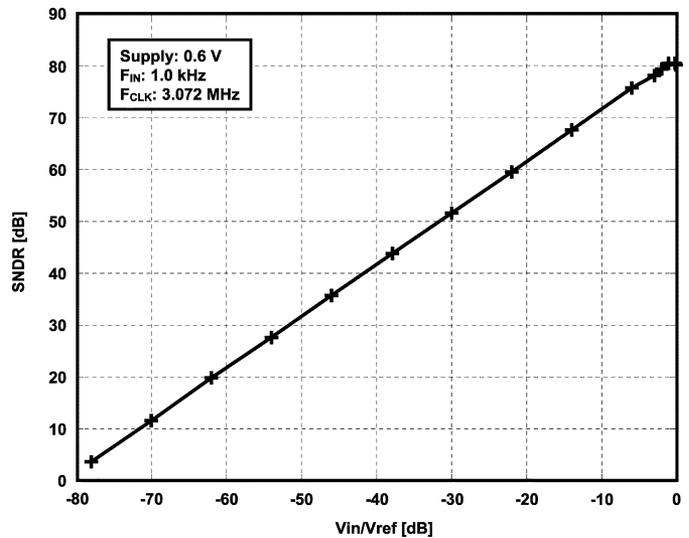


Fig. 13. Measured SNDR.

power consumption. A 3.072-MHz clock frequency is used, resulting in an OSR of 64. Fig. 14 shows the SFDR and SNDR versus power-supply voltage curves (signal reference/swing fixed). The performance is unaffected by the variation of the supply voltage from 0.6 to 1.8 V.

### VI. CONCLUSION

Design techniques are proposed for low-voltage analog CMOS integrated circuits. They do not affect the reliability of fine-linewidth devices by overstressing their gate oxides. Using the proposed techniques, a 2-2 MASH delta-sigma audio ADC operating with a 0.6-V supply is designed and implemented. In the device, linear and large input signal sampling is achieved with switched-RC technique. The overall linearity of the modulator is improved by applying a low-distortion feed-forward

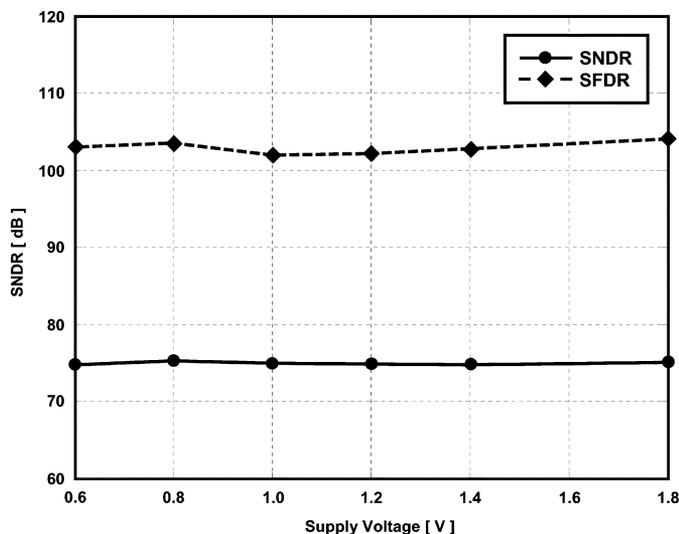


Fig. 14. SNDR and SFDR versus supply voltage.

topology, while the peak SNDR is enhanced by increasing the input signal range using quantized local feedback. The measured results of prototype IC fabricated in a 0.35- $\mu\text{m}$  CMOS technology verify the validity of the proposed design techniques for low-voltage and high-performance operation.

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**Gil-Cho Ahn** (S'94) received the B.S. and M.S. degrees in electrical and electronics engineering from Sogang University, Seoul, Korea, and the Ph.D. degree in electrical engineering and computer science at Oregon State University, Corvallis, in 1994, 1996, and 2005, respectively.

From 1996 to 2001, he was a Design Engineer with Samsung Electronics, Kiheung, Korea, working on mixed analog-digital integrated circuits. In 2005, he joined Broadcom, Irvine, CA, as a Staff Scientist. His current research interests include high-speed, high-resolution data converters and low-voltage, low-power mixed-signal circuits design.

Dr. Ahn received the Analog Devices Outstanding Student Designer Award in 2003.



**Dong-Young Chang** (S'00–M'04) received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, and the Ph.D. degree in electrical and computer engineering from Oregon State University, Corvallis, in 1995, 1997, and 2002, respectively.

He joined Samsung Electronics, Kiheung, Korea, in 1997, where he was engaged in the design of analog front-end systems for CCD/CMOS image sensors and LCD displays. During the summer of 2000, he was with Lucent Technologies, Bell Laboratories, Allentown, PA, where he investigated various low-voltage data converters. From January 2003 to March 2005, he was with Texas Instruments Incorporated, Tucson, AZ, working on low-power high-speed ADC products. In 2005, he joined Engim Inc., Acton, MA, as a Senior Analog Engineer. His research has been focused on low-voltage and low-power analog and mixed-mode integrated circuits. He holds three U.S. patents.

Dr. Chang received the Outstanding Student Paper Award from the IEEE Solid-State Circuits Seoul Chapter in 1998 and the Analog Devices Outstanding Student Designer Award in 2000.



**Matthew E. Brown** (M'99) was born in Santa Barbara, California. He received the B.Sc. degree in electrical and electronics engineering from Oregon State University, Corvallis, in 2001. He is presently working toward the M.S. degree in electrical engineering and computer science at Oregon State University.

From 2001 to 2004, he was a Graduate Research Assistant in the Analog Group at Oregon State University, where he worked on the design of low-voltage circuits including switched-capacitor data converters and low-noise programmable-gain audio amplifiers. Since 2004, he has worked as an R&D Engineer for the Process and Device Integration Group, Hewlett-Packard Company, Corvallis, OR.



**Naoto Ozaki** was born in Niigata, Japan, in 1968. He received the B.S. and M.S. degrees in electronics engineering from Nagaoka University of Technology, Japan, in 1992 and 1994, respectively.

In 1994, he joined the LSI Design and Development Center of Asahi Kasei Microsystems, Kanagawa, Japan. Since then, he has been engaged in the development of CMOS mixed-signal LSIs for digital audio. His current interest is in the development of low-power delta-sigma A/D and D/A converters for digital audio.



**Hiroshi Youra** was born in Yamaguchi, Japan, in 1971. He received the B.S. degree in engineering science from University of Osaka, Osaka, Japan, in 1994 and the M.S. degree in information science from Nara Institute of Science and Technology, Nara, Japan, in 1996.

He subsequently joined the Design and Development Center of Asahi Kasei Microsystems, Kanagawa, Japan. Since then, he has been engaged in the research and development of mixed-signal CMOS LSIs for digital audio. His current interest

is in the development of low-power and high-resolution delta-sigma A/D and D/A converters for digital audio.



**Ken Yamamura** was born in Osaka, Japan, on March 31, 1958. He received the M.S. degree in instrumentation engineering from Keio University, Japan, in 1982.

In 1982, he joined Asahi Kasei Chemical, developed medical analyzing systems. Since 1983, he has been with Asahi Kasei Microsystems, Kanagawa, Japan, developing audio data converter LSIs. His current research interests include high-resolution, low-power data converters and audio circuit design and integration.



**Koichi Hamashita** (M'89) was born in Ishikawa, Japan, in 1957. He received the B.S. and M.S. degrees in mechanical engineering from Kyoto University, Kyoto, Japan, in 1979 and 1981, respectively.

He joined Asahi Kasei in 1981. Since 1985, he has been engaged in the design of CMOS LSIs, especially in the field of delta-sigma ADCs and DACs. He is currently Director-Chief Design and Development Officer of Asahi Kasei Microsystems, Atsugi, Japan.



**Kaoru Takasuka** (M'99) was born in Hiroshima, Japan, in 1947. He received the B.S. and M.S. degrees in instrumentation engineering from the Kyushu Institute of Technology, Kitakyushu, Japan, in 1970 and 1972, respectively.

He joined Asahi Kasei in 1972. Since 1983, he has been engaged in the design of custom CMOS LSIs. He is currently the Vice President-CTO of Asahi Kasei Microsystems, Tokyo, Japan.

Mr. Takasuka was a corecipient of the Award for Technical Excellence from the Society of Instrument and Control Engineers of Japan in 1986 and the Institute of Electrical Engineers of Japan Millennium Best Paper Award in 2001.



**Gábor C. Temes** (SM'66-F'73-LF'98) received the undergraduate degrees from the Technical University of Budapest and Eötvös University, Budapest, Hungary, in 1952 and 1955, respectively. He received the Ph.D. degree in electrical engineering from the University of Ottawa, Ottawa, ON, Canada, in 1961, and an honorary doctorate from the Technical University of Budapest in 1991.

He held academic positions at the Technical University of Budapest, Stanford University, Stanford, CA, and the University of California at Los Angeles (UCLA). He worked in industry at Northern Electric R&D Laboratories (now Bell-Northern Research), Ottawa, Canada, as well as at Ampex Corporation. He is now a Professor in the School of Electrical Engineering and Computer Science at Oregon State University (OSU), Corvallis. He has served as Department Head at both UCLA and OSU. He has co-edited and co-authored many books; the most recent one is *Understanding Delta-Sigma Data Converters* (R. Schreier and G. C. Temes, IEEE Press/Wiley, 2005). He has also written approximately 300 papers in engineering journals and conference proceedings. His recent research has dealt with CMOS analog integrated circuits, as well as data converters.

Dr. Temes has been an Associate Editor of the *Journal of the Franklin Institute*, Editor of the IEEE TRANSACTIONS ON CIRCUIT THEORY, and Vice President of the IEEE Circuits and Systems (CAS) Society. In 1968 and 1981, he was co-winner of the IEEE CAS Darlington Award, and in 1984 winner of the Centennial Medal of the IEEE. He received the Andrew Chi Prize Award of the IEEE Instrumentation and Measurement Society in 1985, the Education Award of the IEEE CAS Society in 1987, and the Technical Achievement Award of the IEEE CAS Society in 1989. He received the IEEE Graduate Teaching Award in 1998, and the IEEE Millennium Medal as well as the IEEE CAS Golden Jubilee Medal in 2000.



**Un-Ku Moon** (S'92-M'94-SM'99) received the B.S. degree from the University of Washington, Seattle, in 1987, the M.Eng. degree from Cornell University, Ithaca, NY, in 1989, and the Ph.D. degree from the University of Illinois at Urbana-Champaign in 1994, all in electrical engineering.

He has been with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, since 1998, where he is currently a Professor. Before joining Oregon State University, he was with Bell Laboratories from 1988 to 1989, and from 1994 to 1998. His technical contributions have been in the area of analog and mixed-signal circuits including highly linear and tunable continuous-time filters, telecommunication circuits including timing recovery and data converters, and ultra-low-voltage analog circuits for CMOS.

Prof. Moon is a recipient of the National Science Foundation CAREER Award, and the Engelbrecht Young Faculty Award from Oregon State University College of Engineering. He has served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING. He currently serves as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He also serves on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference and the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society.