ECE1371 Advanced Analog Circuits
Lecture 10

NOISE IN SC CIRCUITS

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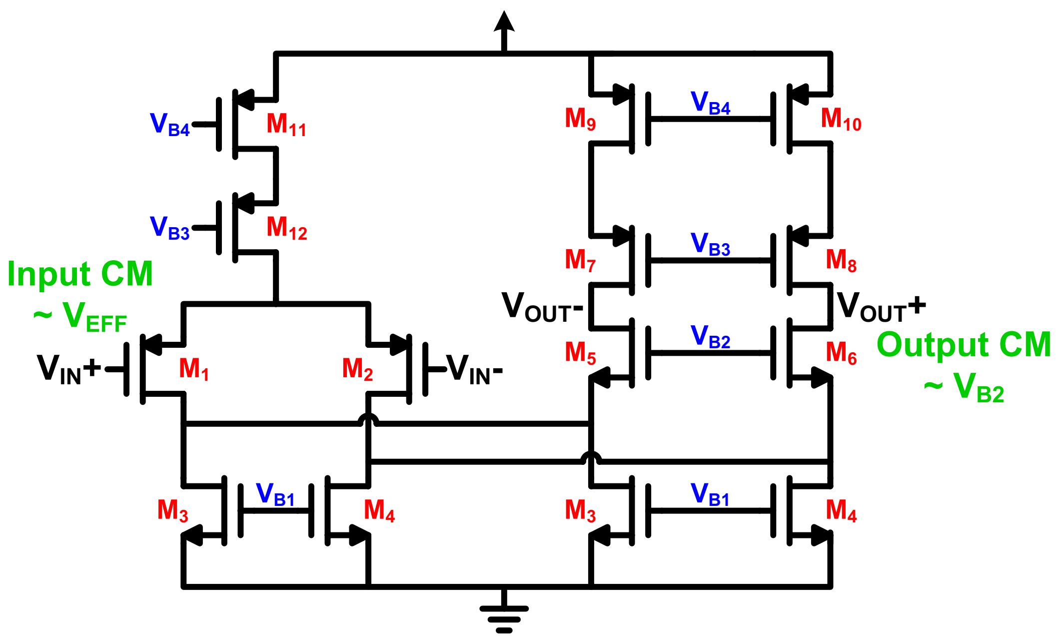
Course Goals

- **Deepen Understanding of CMOS analog circuit design through a top-down study of a modern analog system**
  - The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.
- **Develop circuit insight through brief peeks at some nifty little circuits**
  - The circuit world is filled with many little gems that every competent designer ought to recognize.

Date	Lecture			Ref	Homework
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim
2008-01-21	RS	3	Example Design: Part 2	J&M 14, S&T B	Q-level sim
2008-01-28	TC	4	Pipeline and SAR ADCs	J&M 11,13	Pipeline DNL
2008-02-04	ISSCC – No Lecture				
2008-02-11	RS	5	Advanced ΔΣ	S&T 4, 6.6, 9.4, B	CTMOD2; Proj.
2008-02-18	Reading Week – No Lecture				
2008-02-25	RS	6	Comparator and Flash ADC	J&M 7	
2008-03-03	TC	7	SC Circuits	Raz 12, J&M 10	
2008-03-10	TC	8	Amplifier Design		
2008-03-17	TC	9	Amplifier Design		
2008-03-24	TC	10	Noise in SC Circuits	S&T C	
2008-03-31	RS	11	Switching Regulator		
2008-04-07	Project Presentations				
2008-04-14	TC	12	Matching & MM-Shaping		Project Report

NLCOTD: Gain Booster CMFB

- Need CMFB for Gain Booster
  - One option is to use standard CT CMFB (Lecture 9)
  - Is there an easier way with less circuitry?



Highlights
(i.e. What you will learn today)

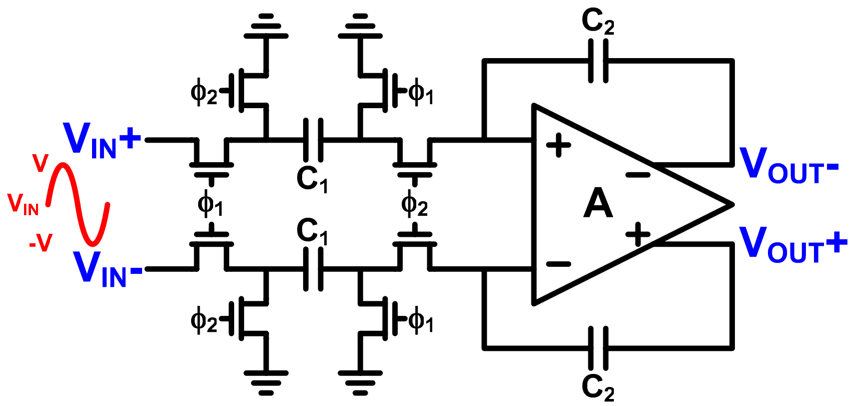
1. How to analyze noise in switched-capacitor circuits

2. Significance of switch noise vs. OTA noise
   Power efficient solution
   Impact of OTA architecture

3. Design example for ΔΣ modulator

Review

- Previous analysis of kT/C noise (ignoring OTA/opamp noise)
  Phase 1: kT/C_1 noise (on each side)
  Phase 2: kT/C_1 added to previous noise (on each side)
  Total Noise (input referred): $2kT/C_1$
  Differentially: $4kT/C_1$



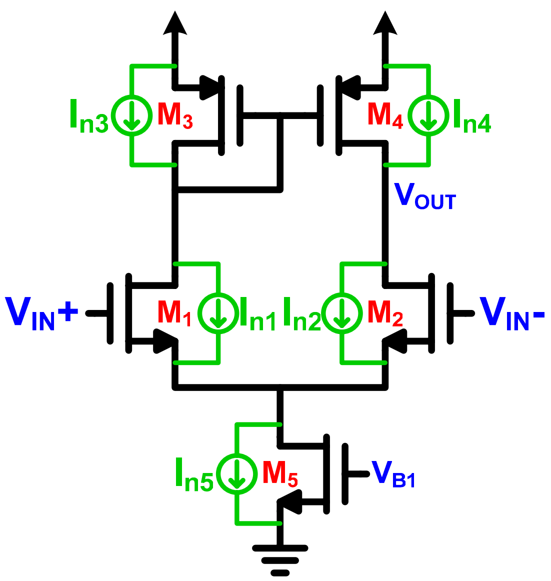
Review

- **SNR**
  - **Total noise power: $4kT/C_1$**
  - **Signal power: $V^2/2$**
  - **SNR: $V^2C_1/8kT$**

- **SNR (single-ended)**
  - **Total noise power: $2kT/C_1$ (sampling capacitor C_1)**
  - **Signal power: $V^2/2$ (signal from -V to V)**
  - **SNR: $V^2C_1/4kT$**

Thermal Noise in OTAs

- **Single-Ended Example**
  - **Noise current from each transistor is $\overline{I_n^2} = 4kT\gamma g_m$**
  - **Assume $\gamma = 2/3$**



Thermal Noise in OTAs

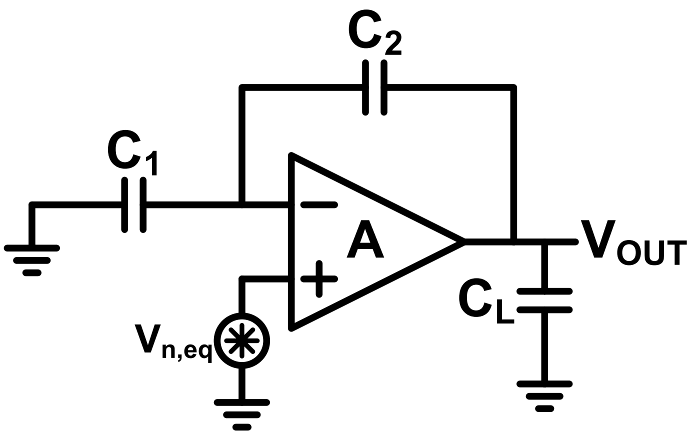
- **Single-Ended Example**
  - **Thermal noise in single-ended OTA**
  - **Assuming paths match, tail current source M_5 does not contribute noise to output**
  - **PSD of noise voltage in M_1 (and M_2):** $\frac{8kT}{3g_{m1}}$
  - **PSD of noise voltage in M_3 (and M_4):** $\frac{8kTg_{m3}}{3g_{m1}^2}$
  - **Total input referred noise from M_1 - M_4**

$$S_{n,eq} = \frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}\right) = \frac{16kT}{3g_{m1}} n_f$$

  - **Noise factor n_f depends on architecture**

OTA with capacitive feedback

- **Analyze output noise in single-stage OTA**
  - **Use capacitive feedback in the amplification / integration phase of a switched-capacitor circuit**



OTA with capacitive feedback

- **Transfer function of closed loop OTA**

$$H(s) = \frac{V_{OUT}}{V_{n,eq}} = \frac{G}{1 + s/\omega_o}$$

where the DC Gain and 1st-pole frequency are

$$G \approx \frac{1}{\beta} = 1 + C_1/C_2 \qquad \omega_o = \frac{\beta g_{m1}}{C_O}$$

Load capacitance C_O depends on the type of OTA – for a single-stage, it is $C_L+C_1C_2/(C_1+C_2)$, while for a two-stage, it is the compensation capacitor C_C

OTA with capacitive feedback

- **Integrate total noise at output**

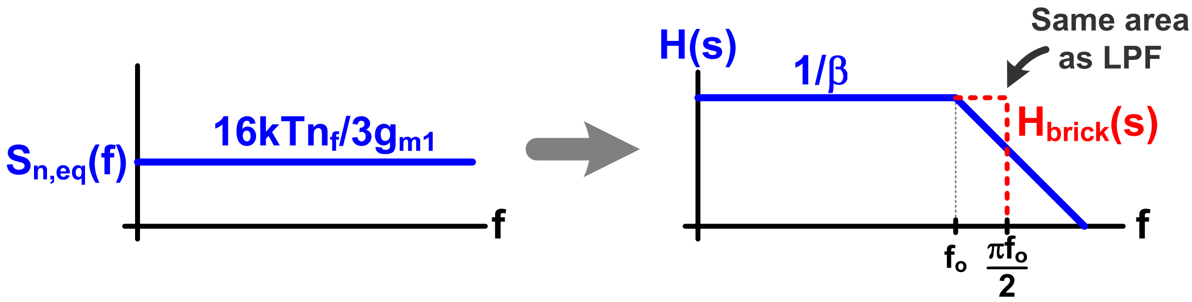
$$\overline{V_{OUT}^2} = \int_0^\infty S_{n,eq}(f)\left|H(j2\pi f)\right|^2 df$$
$$= \frac{16kT}{3g_{m1}} n_f \frac{\omega_o}{4} G^2$$
$$= \frac{4kT}{3\beta C_O} n_f$$

Minimum output noise for β=1 is $\frac{4kT}{3C_O} n_f$

Not a function of g_{m1} since bandwidth is proportional to g_{m1} while PSD is inversely proportional to g_{m1}

OTA with capacitive feedback

- Graphically…



Noise is effectively filtered by the equivalent brick wall response with a cut-off frequency of $\pi f_o/2$

Total noise at V_{OUT} is the integral of the noise within the brick wall filter (area is simply $\pi f_o/2 \times 1/\beta^2$)

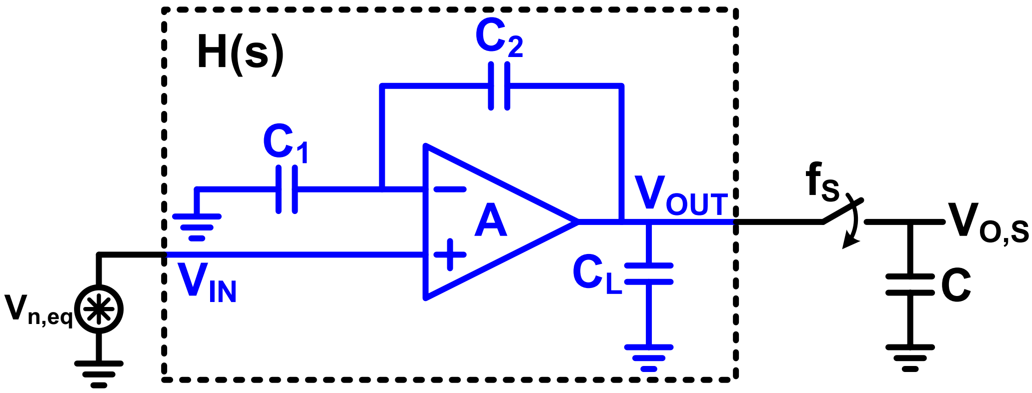
Sampled Thermal Noise

- What happens to noise once it gets sampled?

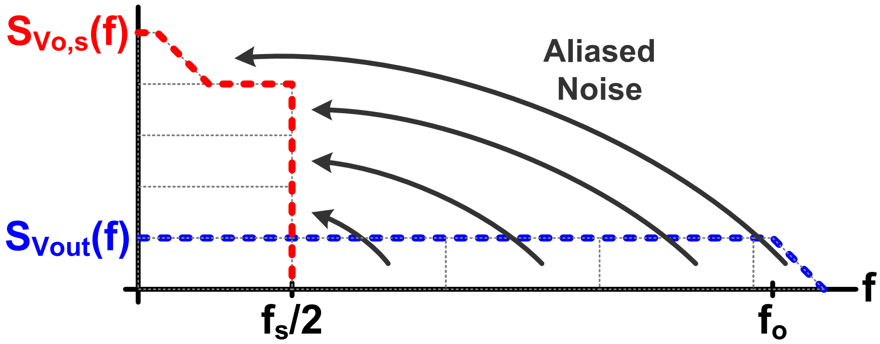
Total noise power is the same

Noise is aliased – folded back from higher frequencies to lower frequencies

PSD of the noise increases significantly



Sampled Thermal Noise



- **Same total area, but PSD is larger from 0 to $f_S/2$**

$$S_{Vout}(f) = \frac{G^2 S_{n,eq}}{4\tau f_S/2} = \frac{\overline{V_{OUT}^2}}{f_S/2} = \frac{4kT}{3\beta C_O} n_f \frac{1}{f_S/2}$$

Low frequency PSD $G^2 S_{n,eq}$ is increased by $\frac{1}{2\tau f_S} = \frac{\pi f_{3dB}}{f_S}$

Sampled Thermal Noise

- **$1/f_{3dB}$ is the settling time of the system, while $1/2f_S$ is the settling period for a two-phase clock**

$$e^{-\frac{1/2f_S}{\tau}} < 2^{-(N+1)}$$

$$\frac{\pi f_{3dB}}{f_S} > (N+1)\ln 2$$

PSD is increased by at least $(N+1)\ln 2$

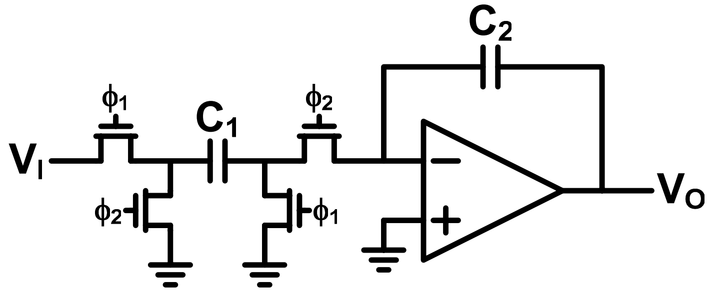
If N = 10 bits, PSD is increased by 7.6, or 8.8dB

- **This is an inherent disadvantage of sampled-data compared to continuous-time systems**

But noise is reduced by oversampling ratio after digital filtering

Noise in a SC Integrator

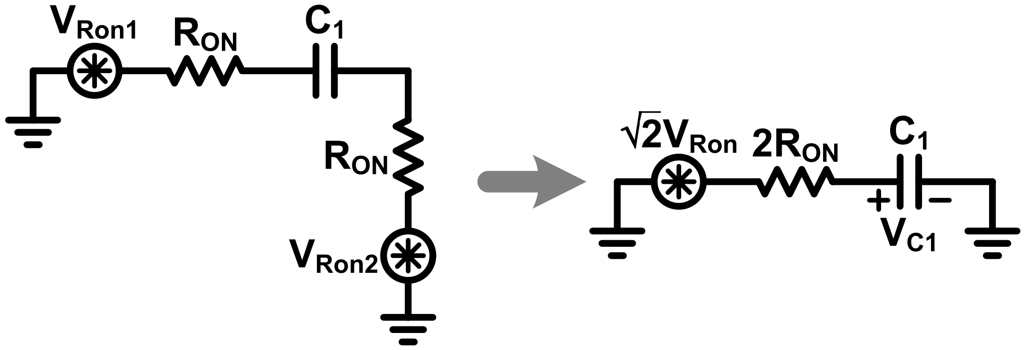
- **Using the parasitic-insensitive SC integrator**



- **Two phases to consider**
  - **1) Sampling Phase**
    - **Includes noise from both ϕ_1 switches**
  - **2) Integrating Phase**
    - **Includes noise from both ϕ_2 switches and OTA**

Noise in a SC Integrator

- **Phase 1: Sampling**



Noise PSD from two switches: $S_{Ron}(f) = 8kTR_{ON}$

Time constant of R-C filter: $\tau = 2R_{ON}C_1$

PSD of noise voltage across C_1

$$S_{C1}(f) = \frac{8kTR_{ON}}{1 + (2\pi f\tau)^2}$$

Noise in a SC Integrator

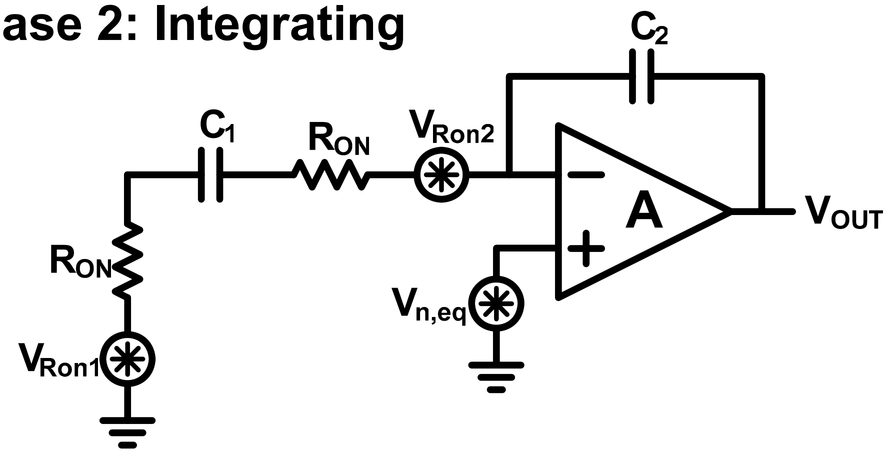
- **Phase 1: Sampling**
  - Integrated across entire spectrum, total noise power in C_1 is

$$\overline{V_{C1,sw1}^2} = \frac{8kTR_{ON}}{4\tau} = \frac{kT}{C_1}$$

  - Independent of R_{ON} (PSD is proportional to R_{ON}, bandwidth is inversely proportional to R_{ON})
  - After sampling, charge is trapped in C_1

Noise in a SC Integrator

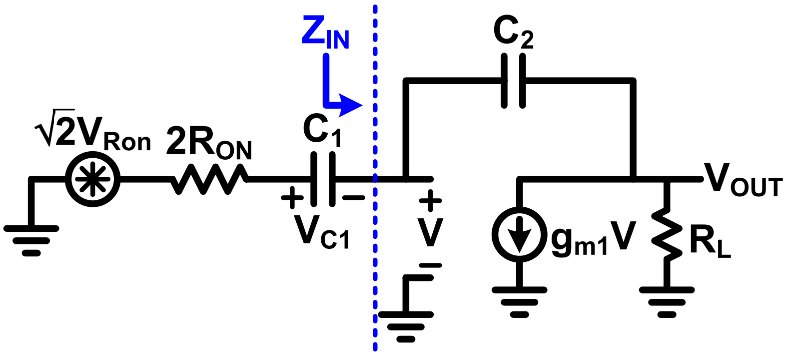
- **Phase 2: Integrating**



- **Two noise sources - switches and OTA**
  - Noise PSD from two switches: $S_{Ron}(f) = 8kTR_{ON}$
  - Noise PSD from OTA: $S_{vn,eq}(f) = \frac{16kT}{3g_{m1}} n_f$
  - Noise voltage across C_1 charges to $\sqrt{2}V_{Ron} - V_{n,eq}$

Noise in a SC Integrator

- **What is the time-constant?**



Analysis shows that $Z_{IN} = \frac{1/sC_2 + R_L}{1 + g_{m1}R_L}$

For large R_L**, assume that** $Z_{IN} = \frac{1}{g_{m1}}$

Resulting time constant $\tau = (2R_{ON} + 1/g_{m1})C_1$

Noise in a SC Integrator

- **Total noise power with both switches and OTA on integrating phase**

$$\overline{V_{C1,op}^2} = \frac{S_{vn,eq}(f)}{4\tau} = \frac{16kT}{3g_{m1}} \frac{n_f}{4(2R_{ON} + 1/g_{m1})C_1} = \frac{4kT}{3C_1} \frac{n_f}{(1+x)}$$

$$\overline{V_{C1,sw2}^2} = \frac{S_{Ron}(f)}{4\tau} = \frac{8kTR_{ON}}{4(2R_{ON} + 1/g_{m1})C_1} = \frac{kT}{C_1} \frac{x}{(1+x)}$$

Introduced extra parameter $x = 2R_{ON}g_{m1}$

Noise in a SC Integrator

- **Total noise power on C_1 from both phases**

$$\overline{V_{C1}^2} = \overline{V_{C1,op}^2} + \overline{V_{C1,sw1}^2} + \overline{V_{C1,sw2}^2}$$
$$= \frac{4kT}{3C_1}\frac{n_f}{(1+x)} + \frac{kT}{C_1}\frac{x}{(1+x)} + \frac{kT}{C_1}$$
$$= \frac{kT}{C_1}\left(\frac{4n_f/3+1+2x}{1+x}\right)$$

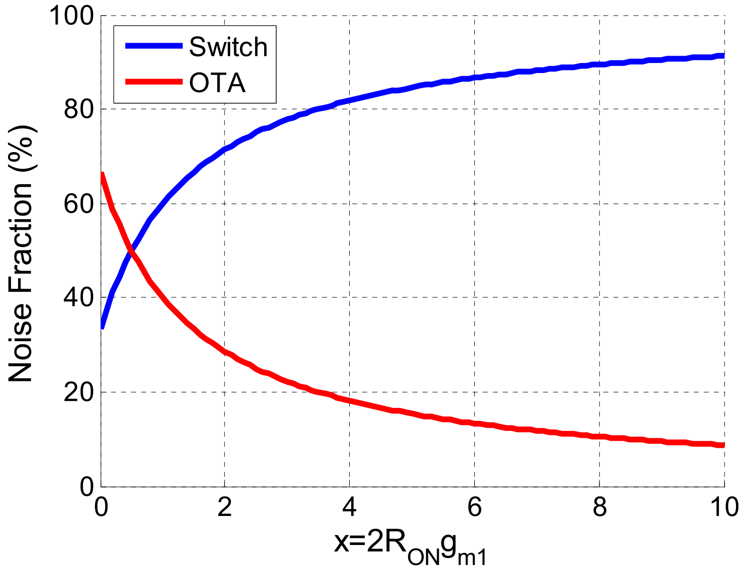
Lowest possible noise achieved if $x \to \infty$

In this case, $\overline{V_{C1}^2} = \frac{2kT}{C_1}$

What was assumed to be the total noise was actually the least possible noise!

Noise Contributions

- **Percentage noise contribution from switches and OTA (assume n_f=1.5)**



Noise Contributions

- When $g_{m1} >> 1/R_{ON}$ ($x >> 1$)…
  - Switch dominates both bandwidth and noise
  - Total noise power is minimized

- When $g_{m1} << 1/R_{ON}$ ($x << 1$)…
  - OTA dominates both bandwidth and noise
  - Power-efficient solution
    - Minimize g_{m1} (and power) for a given settling time and noise

$$g_{m1} = \frac{kT}{\tau \overline{V_{C1}^2}} \left(\frac{4}{3} n_f + 1 + 2x \right)$$

    - Minimized for x=0

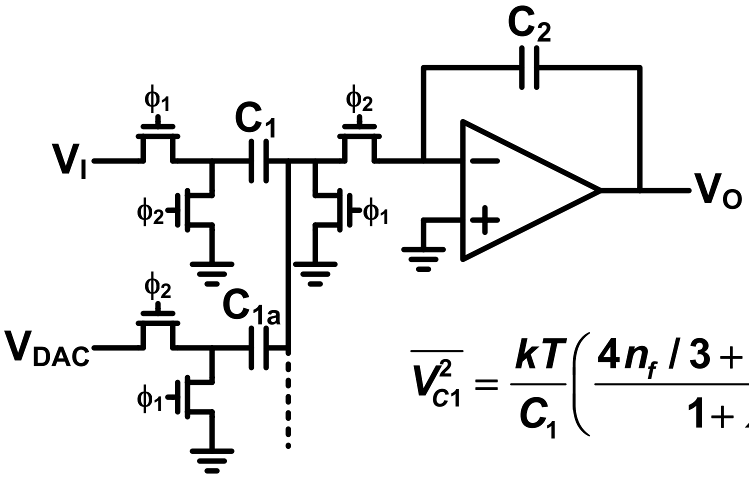
Maximum Noise

- How much larger can the noise get?
  - Depends on n_f… (table excludes cascode noise)

Architecture	Relative V_{EFF}'s	n_f	Maximum Noise (x=0)	+dB
Telescopic/ Diff.Pair	$V_{EFF,1}=V_{EFF,n}/2$	1.5	$3 \cdot kT/C_1$	1.76
Telescopic/ Diff.Pair	$V_{EFF,1}=V_{EFF,n}$	2	$3.67 \cdot kT/C_1$	2.63
Folded Cascode	$V_{EFF,1}=V_{EFF,n}/2$	2.5	$4.33 \cdot kT/C_1$	3.36
Folded Cascode	$V_{EFF,1}=V_{EFF,n}$	4	$6.33 \cdot kT/C_1$	5.01

Separate Input Capacitors

- **Using separate input caps increases noise**
  - **Each additional input capacitor adds to the total noise**
  - **Separate caps help reduce signal dependent disturbances in the DAC reference voltages**



$$\overline{V_{C1}^2} = \frac{kT}{C_1}\left(\frac{4n_f/3+1+2x}{1+x}\right)\left(1+\frac{C_{1a}}{C_1}+\ldots\right)$$

Differential vs. Single-Ended

- **All previous calculations assumed single-ended operation**
  - **For same settling time, $g_{m1,2}$ is the same, resulting in the same total power [0dB]**
  - **Differential input signal is twice as large [gain 6dB]**
  - **Differential operation has twice as many caps and therefore twice as much capacitor noise (assume same size per side – C_1 and C_2) [lose ~1.2dB for n_f=1.5, x=0… less for larger n_f]**

- **Net Improvement: ~4.8dB**

Differential vs. Single-Ended

- **Single-Ended Noise**

$$\overline{V^2_{C1,se}} = \frac{kT}{C_1}\left(\frac{4n_f/3 + 1 + 2x}{1+x}\right)$$

- **Differential Noise**

$$\overline{V^2_{C1,diff}} = \overline{V^2_{C1,op}} + \overline{V^2_{C1,sw1}} + \overline{V^2_{C1,sw2}}$$

$$= \frac{4kT}{3C_1}\frac{n_f}{(1+x)} + \frac{2kT}{C_1}\frac{x}{(1+x)} + \frac{2kT}{C_1}$$

$$= \frac{kT}{C_1}\left(\frac{4n_f/3 + 2 + 4x}{1+x}\right)$$

- **Relative Noise (for n_f=1.5, x=0)**

$$\frac{\overline{V^2_{C1,diff}}}{\overline{V^2_{C1,se}}} = \frac{4n_f/3 + 2 + 4x}{4n_f/3 + 1 + 2x} = \frac{4}{3}$$

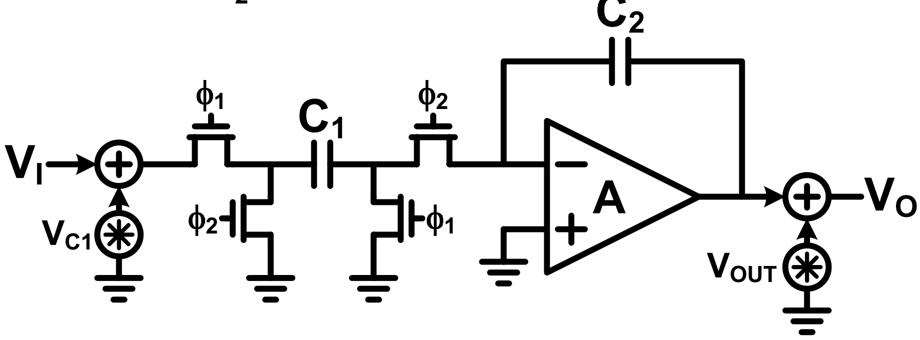
Noise in an Integrator

- **What is the total output-referred noise in an integrator?**

Assume an integrator transfer function

$$H(z) = \frac{kz^{-1}}{1 + \mu(1+k) - (1+\mu)z^{-1}}$$

where $k = \frac{C_1}{C_2}$ **and** $\mu = \frac{1}{A}$



Noise in an Integrator

- **Total output-referred noise PSD**

$$S_{INT}(f) = S_{C1}(f)\left|H(z)\right|^2 + S_{OUT}(f)$$

where $\overline{V_{OUT}^2} = \dfrac{4kT}{3\beta C_O} n_f$

and $\overline{V_{C1}^2} = \dfrac{kT}{C_1}\left(\dfrac{4n_f/3 + 1 + 2x}{1 + x}\right)$

Since all noise sources are sampled, white PSDs

$$S_x = \frac{\overline{V_x^2}}{f_S/2}$$

To find output-referred noise for a given OSR

$$\overline{V_{INT}^2} = \int_0^{f_S/(2\cdot OSR)} S_{INT}(f)\,df$$

Noise in a ΔΣ Modulator

- **How do we find the total input-referred noise in a ΔΣ modulator?**
  1) **Find all thermal noise sources**
  2) **Find PSDs of the thermal noise sources**
  3) **Find transfer functions from each noise source to the output**
  4) **Using the transfer functions, integrate all PSDs from DC to the signal band edge $f_S/2\cdot OSR$**
  5) **Sum the noise powers to determine the total output thermal noise**
  6) **Input noise = output noise (assuming STF is ~1 in the signal band)**

Noise in a ΔΣ Modulator

- **Example:**

  f_S = 100MHz, T = 10ns, OSR = 32

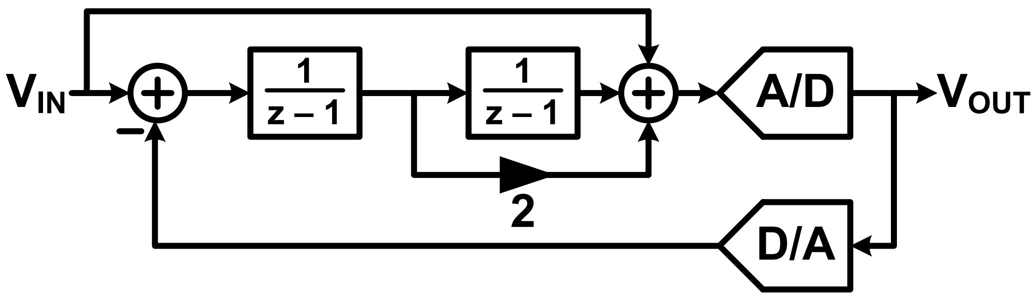
  SNR = 80dB (13-bit resolution)

  Input Signal Power = 0.25V² (-6dB from 1V²)

  Noise Budget: 75% thermal noise

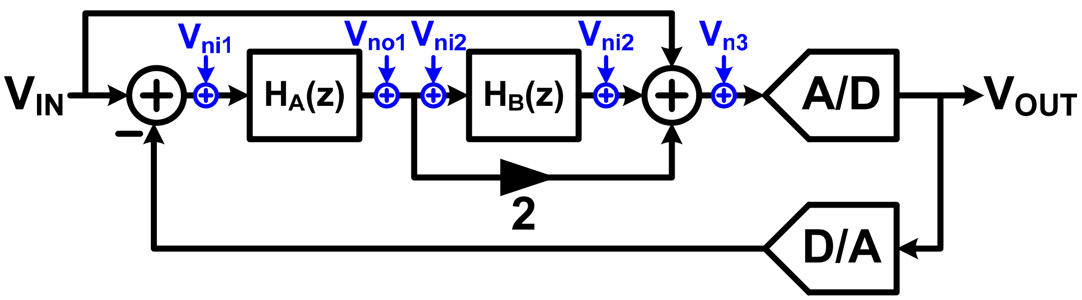
  Total input referred thermal noise:

$$\overline{V_{TH}^2} = 0.75 * 10^{(-6-SNR)/10} = (43.4\mu V)^2$$



Noise in a ΔΣ Modulator

1) Find all thermal noise sources



$$\overline{V_{ni1}^2} = \frac{kT}{C_{1A}}\left(\frac{4n_{fA}/3 + 1 + 2x_A}{1 + x_A}\right) \qquad \overline{V_{ni2}^2} = \frac{kT}{C_{1B}}\left(\frac{4n_{fB}/3 + 1 + 2x_B}{1 + x_B}\right)$$

$$\overline{V_{no1}^2} = \frac{4kT}{3\beta_A C_{OA}} n_{fA} \qquad \overline{V_{no2}^2} = \frac{4kT}{3\beta_B C_{OB}} n_{fB}$$

$$\overline{V_{n3}^2} = \frac{2kT}{C_{f1}}\left(1 + \frac{C_{f2}}{C_{f1}} + \frac{C_{f3}}{C_{f1}}\right) = \frac{2kT}{C_{f1}}(1 + 2 + 1)$$

Noise in a ΔΣ Modulator

2) Find PSDs of the thermal noise sources

For each of the mean square voltage sources,

$$S_x = \frac{\overline{V_x^2}}{f_S / 2}$$

3) Find transfer functions from each noise source to the output

Assume ideal integrators

$$H_A(z) = H_B(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$STF(z) = 1$$

$$NTF(z) = (1 - z^{-1})^2 = \frac{1}{1 + 2H(z) + H(z)^2}$$

Noise in a ΔΣ Modulator

3) Find transfer functions from each noise source to the output

From input of $H_A(z)$ to output…

$$NTF_{i1}(z) = \left(2H(z) + H(z)^2\right) NTF(z)$$

$$= \frac{2H(z) + H(z)^2}{1 + 2H(z) + H(z)^2} = 2z^{-1} - z^{-2}$$

From output of $H_A(z)$ to output…

$$NTF_{o1}(z) = \left(2 + H(z)\right) NTF(z)$$

$$= \frac{2 + H(z)}{1 + 2H(z) + H(z)^2} = (1 - z^{-1})(2 - z^{-1})$$

Noise in a ΔΣ Modulator

3) Find transfer functions from each noise source to the output

From input of $H_B(z)$ to output…

$$NTF_{i2}(z) = H(z)NTF(z)$$

$$= \frac{H(z)}{1 + 2H(z) + H(z)^2} = z^{-1}(1 - z^{-1})$$

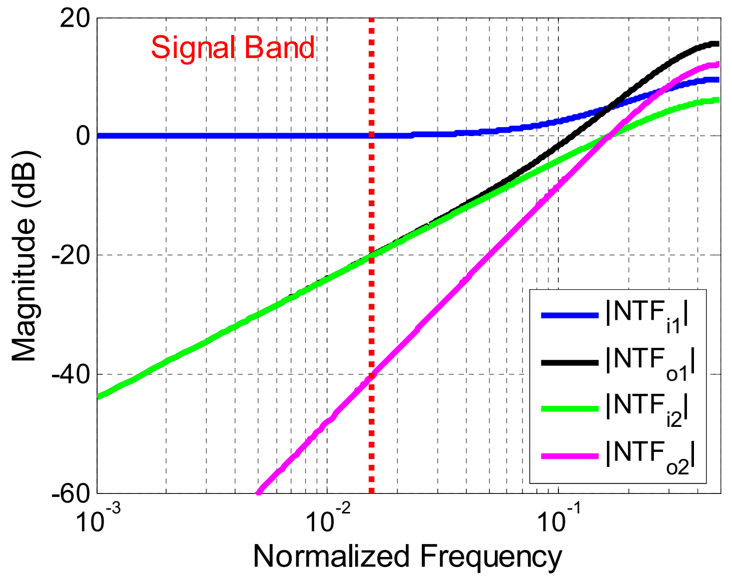
From output of $H_B(z)$ to output (equal to transfer function at input of summer to output)…

$$NTF_{o2}(z) = NTF(z) = (1 - z^{-1})^2$$

Noise in a ΔΣ Modulator

3) Find transfer functions from each noise source to the output

Most significant is NTF_{i1}



Noise in a ΔΣ Modulator

4) **Using the transfer functions, integrate all PSDs from DC to the signal band edge $f_S/2 \cdot OSR$**

Use MATLAB/Maple to solve the integrals…

$$\overline{N_{i1}^2} = \frac{\overline{V_{ni1}^2}}{f_S/2} \int_0^{f_S/(2\cdot OSR)} \left|NTF_{i1}(f)\right|^2 df$$

$$= \frac{\overline{V_{ni1}^2}}{f_S/2}\left[\frac{5f_S}{2\cdot OSR} - \frac{2f_S}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right]$$

$$\overline{N_{o1}^2} = \frac{\overline{V_{no1}^2}}{f_S/2} \int_0^{f_S/(2\cdot OSR)} \left|NTF_{o1}(f)\right|^2 df$$

$$= \frac{\overline{V_{no1}^2}}{f_S/2}\left[\frac{7f_S}{OSR} + \frac{2f_S}{\pi}\sin\left(\frac{\pi}{OSR}\right)\cos\left(\frac{\pi}{OSR}\right) - \frac{9f_S}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right]$$

Noise in a ΔΣ Modulator

4) **Using the transfer functions, integrate all PSDs from DC to the signal band edge $f_S/2 \cdot OSR$**

$$\overline{N_{i2}^2} = \frac{\overline{V_{ni2}^2}}{f_S/2}\left[\frac{f_S}{OSR} - \frac{f_S}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right]$$

$$\overline{N_{o2}^2} = \frac{\overline{V_{no2}^2} + \overline{V_{n3}^2}}{f_S/2}\left[\frac{3f_S}{OSR} + \frac{f_S}{\pi}\sin\left(\frac{\pi}{OSR}\right)\cos\left(\frac{\pi}{OSR}\right) - \frac{4f_S}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right]$$

(Some simplifications can be made for large OSR)

Noise in a ΔΣ Modulator

5) Sum the noise powers to determine the total output thermal noise

Assume $x_A = x_B = 0.1$ and $n_{fA} = n_{fB} = 1.5$

$$\overline{V_{TH}^2} \approx \frac{2.9kT}{C_{1A}}\frac{1}{OSR} + \frac{2kT}{\beta_A C_{OA}}\frac{\pi^2}{3OSR^3} + \frac{2.9kT}{C_{1B}}\frac{\pi^2}{3OSR^3} + \frac{2kT}{\beta_B C_{OB}}\frac{\pi^4}{5OSR^5} + \frac{8kT}{C_{f1}}\frac{\pi^4}{5OSR^5}$$

With an OSR of 32, first term is most significant (assume $\beta_A = \beta_B = 1/3$)

$$\overline{V_{TH}^2} \approx 9.1\times10^{-2}\frac{kT}{C_{1A}} + 6.0\times10^{-4}\frac{kT}{C_{OA}} + 2.9\times10^{-4}\frac{kT}{C_{1B}} + \ldots$$

Noise in a ΔΣ Modulator

6) Input noise = output noise (assuming STF is ~1 in the signal band)

$$\overline{V_{TH}^2} \approx 9.1\times10^{-2}\frac{kT}{C_{1A}} = (43.4\mu V)^2$$

=> C_{1A} = 200fF

Assuming other capacitors are smaller than C_{1A}, then subsequent terms are insignificant and the approximation is valid

If lower oversampling ratios are used, other terms may become more significant in the calculation

Noise in a Pipeline ADC

- **Similar procedure to ΔΣ modulator, except transfer functions are much easier to compute**

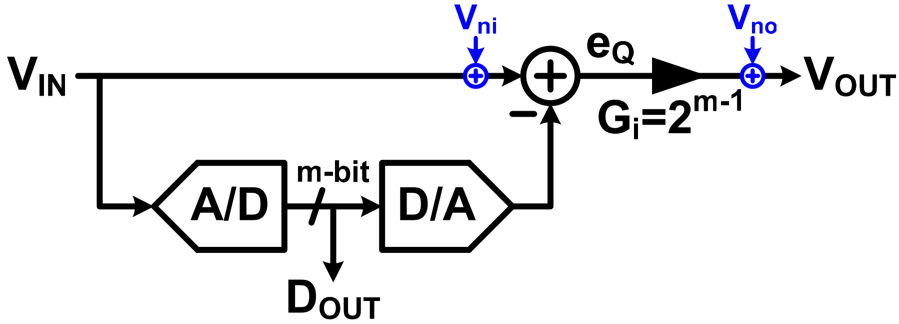
- **Differences…**
  - **Input refer all noise sources**
  - **Gain from each stage to the input is a scalar**
  - **Noise from later stages will be more significant since typical stage gains are as low as 2**
  - **Sample-and-Hold adds extra noise which is input referred with a gain of 1**
  - **Entire noise power is added since the signal band is from 0 to $f_S/2$ (OSR=1)**

Noise in a Pipeline ADC

- **Example**
  - **If each stage has a gain G_1, G_2, … G_N**

$$\overline{N_i^2} = \overline{V_{ni1}^2} + \frac{\overline{V_{no1}^2} + \overline{V_{ni2}^2}}{G_1^2} + \frac{\overline{V_{no2}^2} + \overline{V_{ni3}^2}}{G_1^2 G_2^2} + \cdots + \frac{\overline{V_{noN}^2}}{G_1^2 G_2^2 \cdots G_N^2}$$

  - **S/H stage noise will add directly to V_{ni1}**



NLCOTD: Gain Booster CMFB

What You Learned Today

1. Noise analysis for switched-capacitor circuits
2. Contributions of both switch noise and OTA noise
   - Finding a power efficient solution
   - Significance of OTA architecture
3. $\Delta\Sigma$ modulator design example

Some Project Guidelines

- **General:**
  1) **Corners: Do not need to simulate**
  2) **Noise analysis: use calculations to size the capacitors, but use Cadence to find OTA noise**
  3) **Clock Generator: don't need to design non-overlapping clock generator, but buffer the ideal clocks and take into account the buffer size for power calculations (if you have other clock phases – not just ϕ_1 and ϕ_2 – you should indicate how you would generate these)**
  4) **Biasing: Ideal voltage source for VDD/VSS and reference ladder edges; Ideally one current source from which all currents are derived (at least use only one current source per circuit block)**

Some Project Guidelines

- **Presentation: 15-20 minutes**

  12 Slides (1 title, 11 content)

  Focus on major design issues and circuit blocks (what you consider the most important design decisions)

- **Report**

  We should be able to replicate your circuit with the information provided in the report

  Give transistor sizes, preferably annotated on figures

  Try to avoid Cadence schematics (if you use them, make them more readable without all the unnecessary annotations)