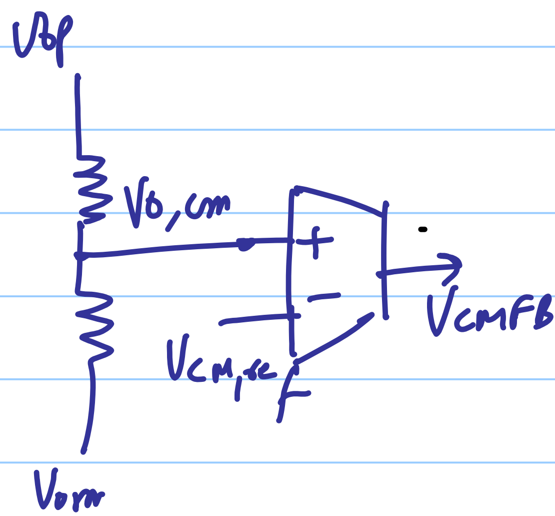
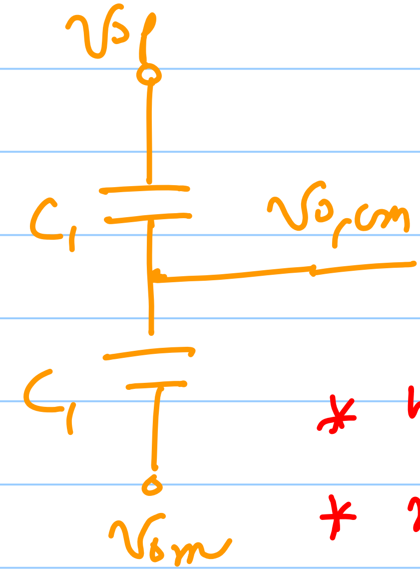
ECE 614 – Lecture 7

Note Title 9/16/2014

CM-detectors ⟶ dual diff pair

↳ Resistive averaging → load the output but wide swing



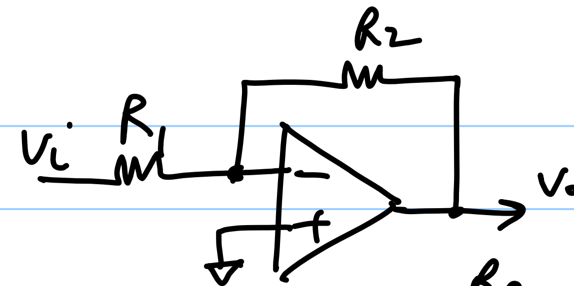


* wide swing

* no resistive loading

* Can we use Capacitive CM-detector?

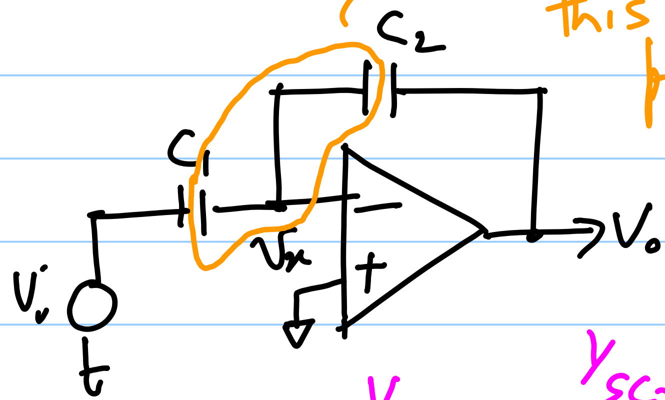
Switched Capacitor Circuits



$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

Car

total charge in this surface is preserved.



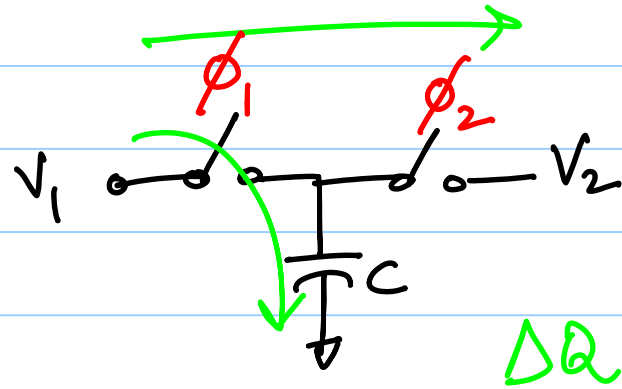
$$\frac{V_o}{V_i} = -\frac{Y_{sC_2}}{Y_{sC_1}} = -\frac{C_1}{C_2}$$

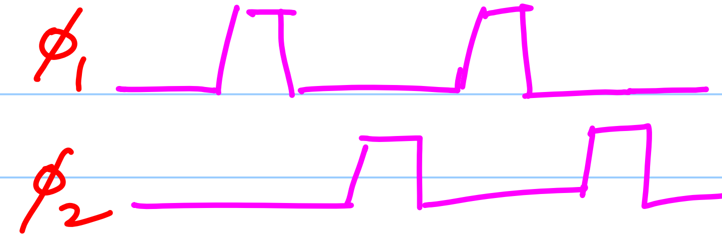
, No resistive loading!

But, there is no DC feedback path.

↳ doesn't bias properly

Switched Cap Resistor



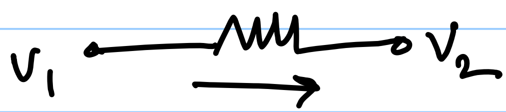


Complementary clocks @ f_s

$$\Delta Q = C(V_1 - V_2)$$

$$I_{av} = \frac{\Delta Q}{T_s} = f_s \Delta Q = f_s C (V_1 - V_2)$$

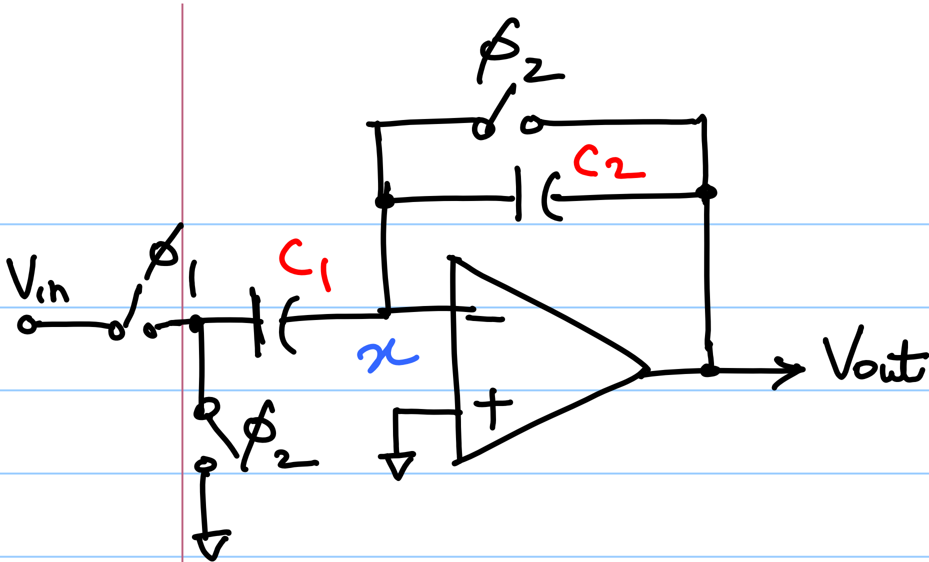
$$= \frac{V_1 - V_2}{1/f_s C}$$

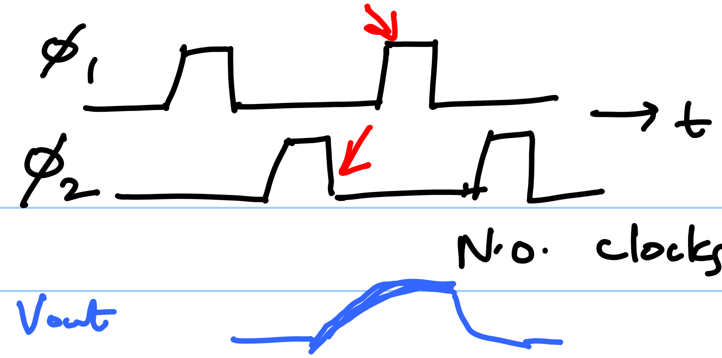


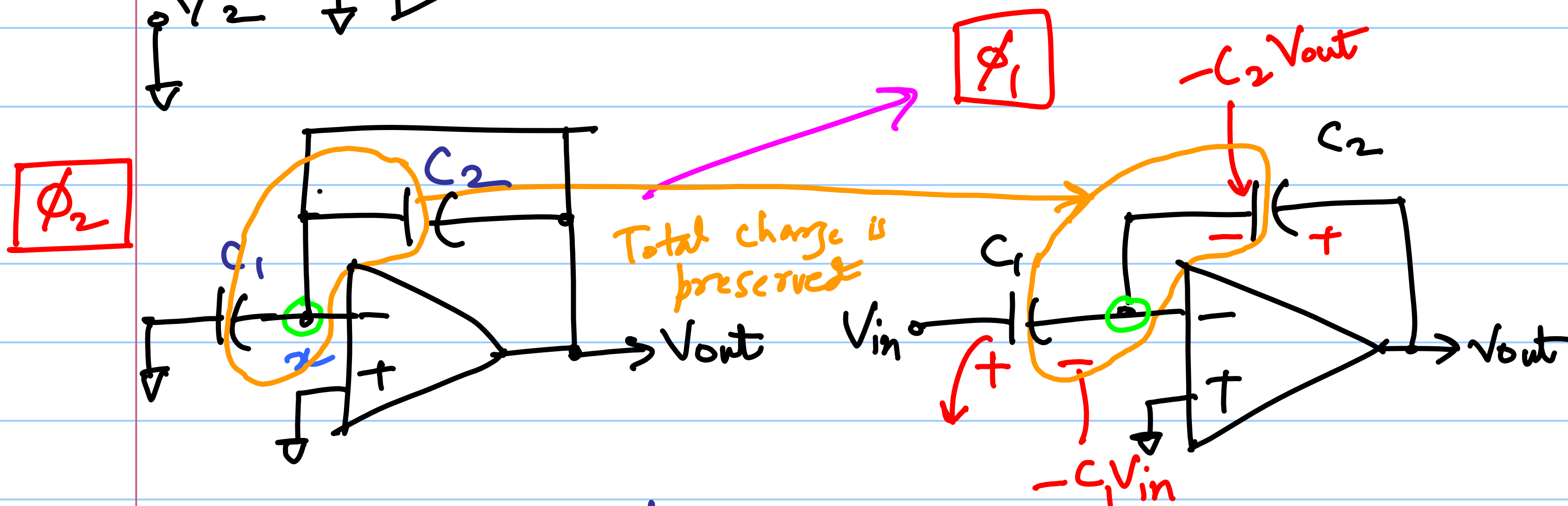
$$I = \frac{V_1 - V_2}{R}$$

$$R = \frac{1}{f_s C}$$

× Discrete-time circuit







$V_x = 0$ due to the DC feedback

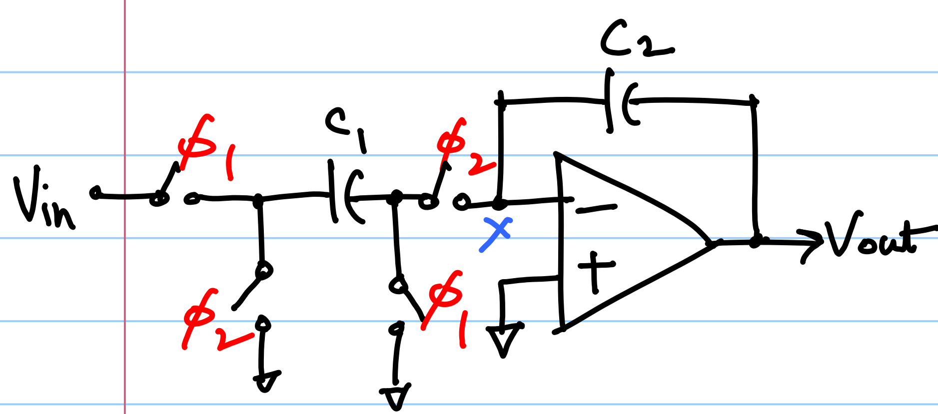
Input is sampled on C_1 & C_2

* Since the charge on the virtual ground is preserved

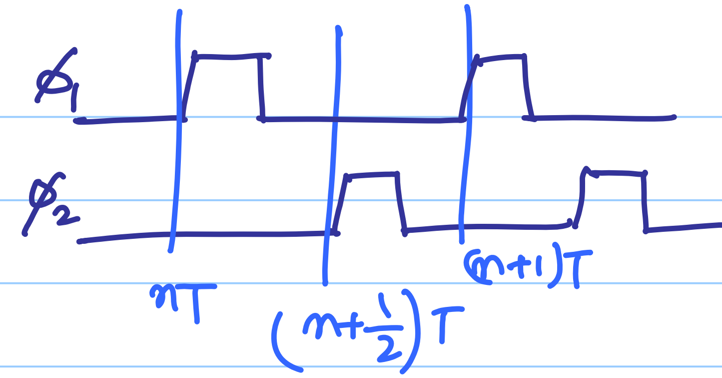
$$Q = \underbrace{C_1(0) + C_2(0)}_{0} = -C_1 V_{in} - C_2 V_{out} = 0$$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$$ after settling occurs

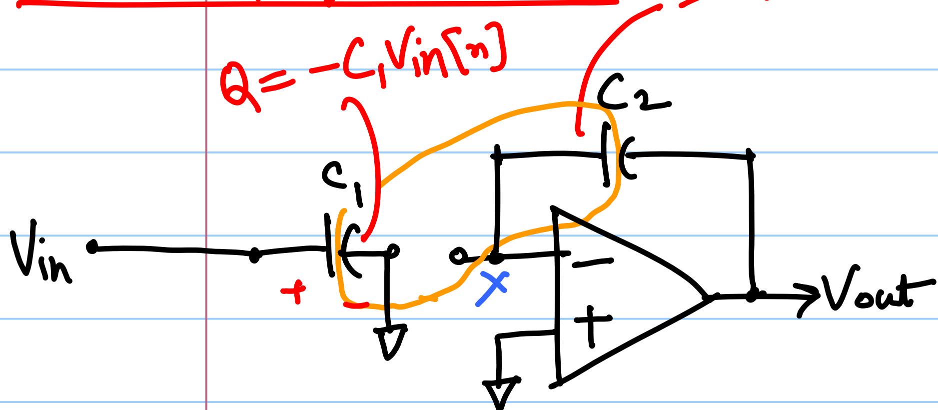
SC Integrator:



assume ideal switches



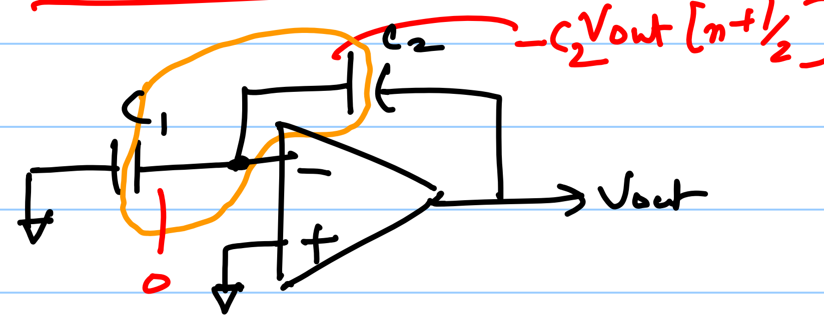
ϕ_1: sampling phase



Voltage across C_1 tracks V_{in}

C_2 holds previous value

ϕ_2: integration phase



* charge stored in C_1 is transferred to C_2

$$Q[n] = -V_{in}[n]C_1 + (0 - V_{out}[n])C_2$$
$$= -V_{in}(n)C_1 - V_{out}[n]C_2$$

$$Q[n+\tfrac{1}{2}] = 0\cdot C_1 - V_{out}[n+\tfrac{1}{2}]\cdot C_2$$

* Since the charge at the plates connected to V_x is conserved

$$\Rightarrow \quad Q[n+\tfrac{1}{2}] = Q(n)$$

$$\Rightarrow \quad V_{out}[n+\tfrac{1}{2}]C_2 = V_{in}(n)C_1 + V_{out}[n]C_2$$

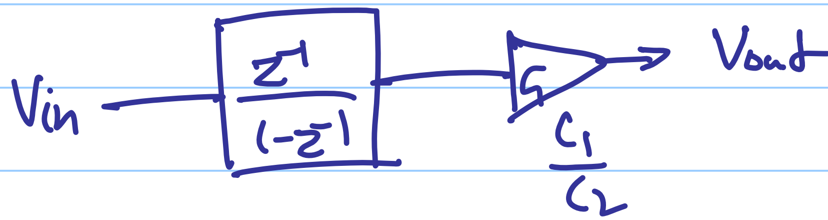
$V_{out}[n+1] \triangleq V_{out}[n+\tfrac{1}{2}]$ ← C_2 is disconnected during ϕ_1

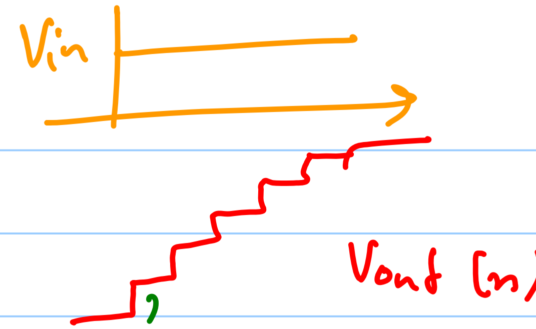
$$V_{out}[n] = V_{out}[n-1] + \frac{C_1}{C_2}V_{in}[n-1]$$

$$V_{out}(z) = z^{-1}V_{out}(z) + z^{-1}\frac{C_1}{C_2}V_{in}(z)$$

$$\frac{V_{out}}{V_{in}}(z) = \underbrace{\frac{C_1}{C_2}}_{\text{gain}} \cdot \frac{z^{-1}}{1-z^{-1}}$$

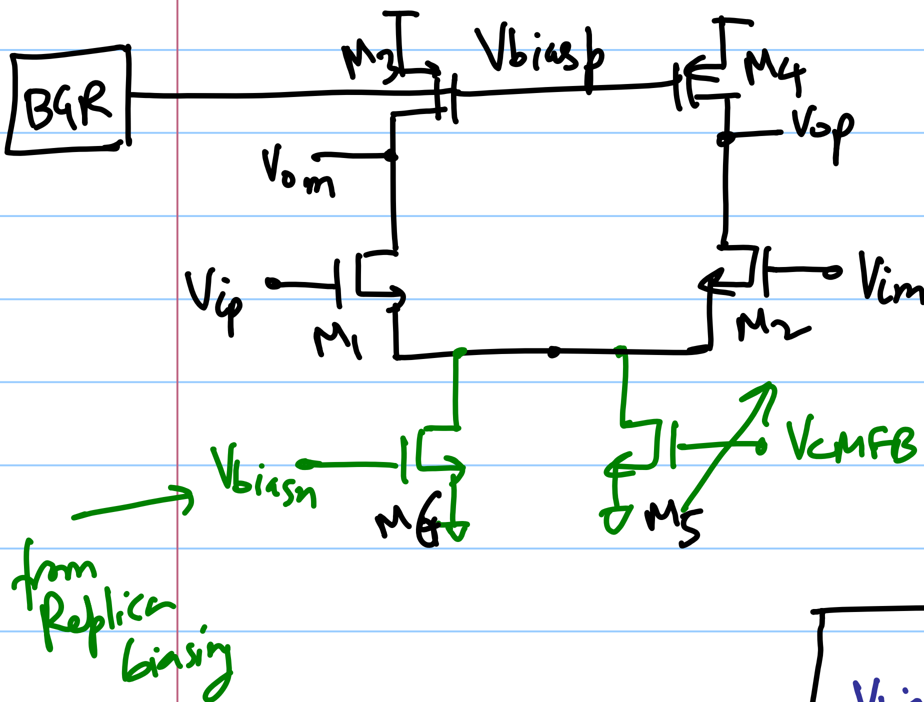
Delaying Discrete-time integrator

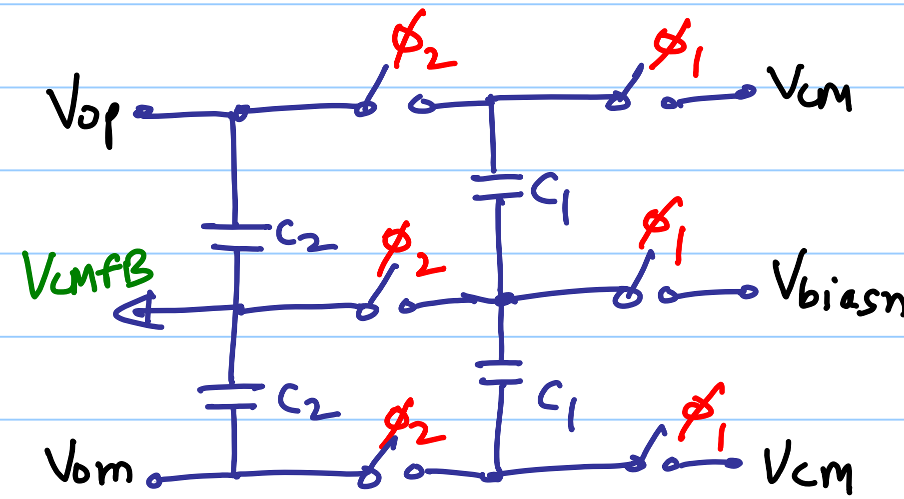




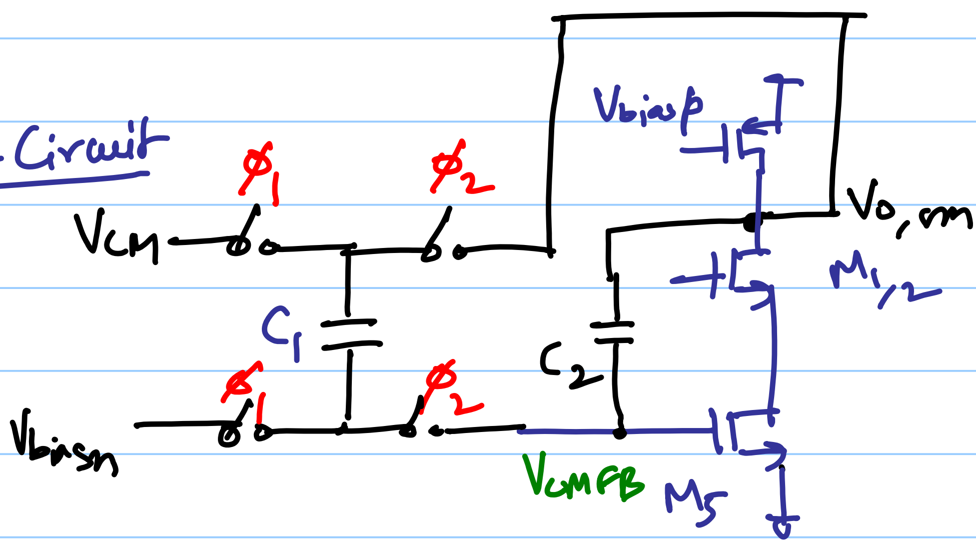
$$\Delta = \frac{C_1}{C_2} V_{in}[n]$$

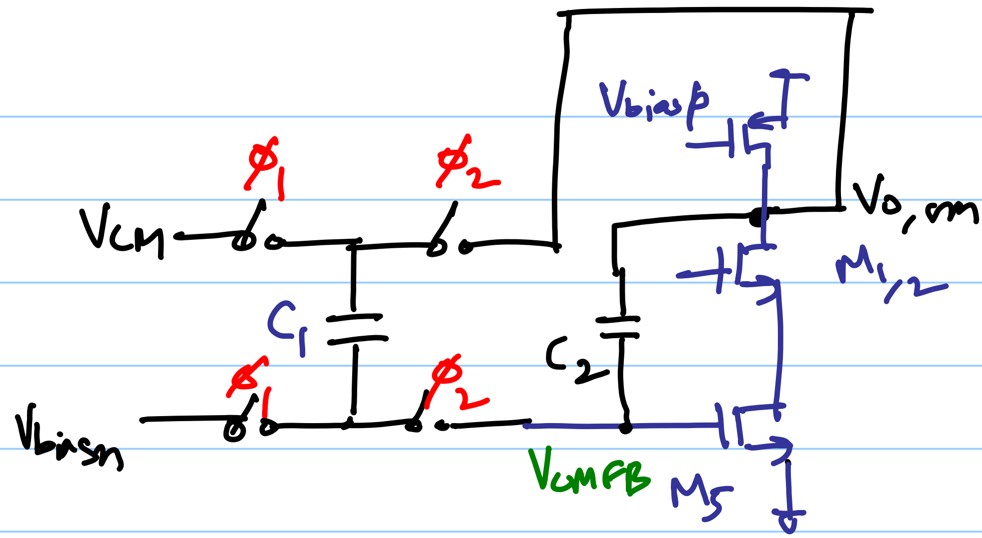
SC CMFB



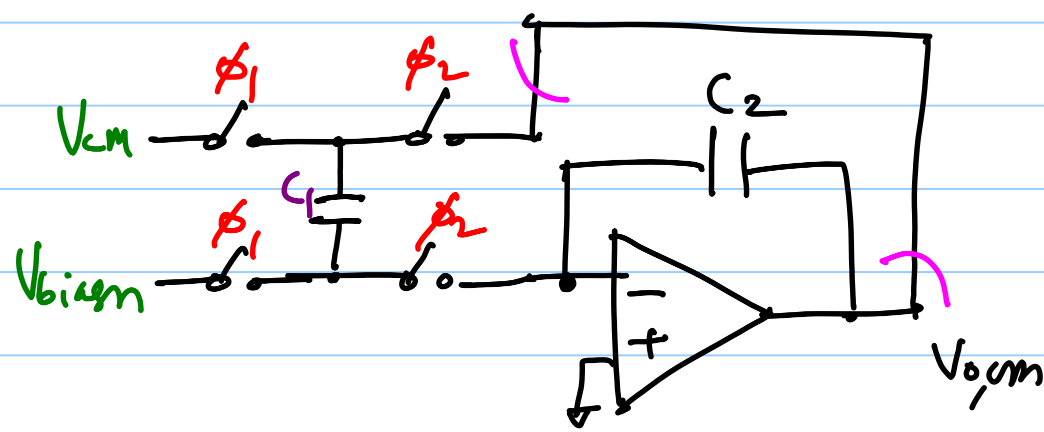


CM Half-Circuit

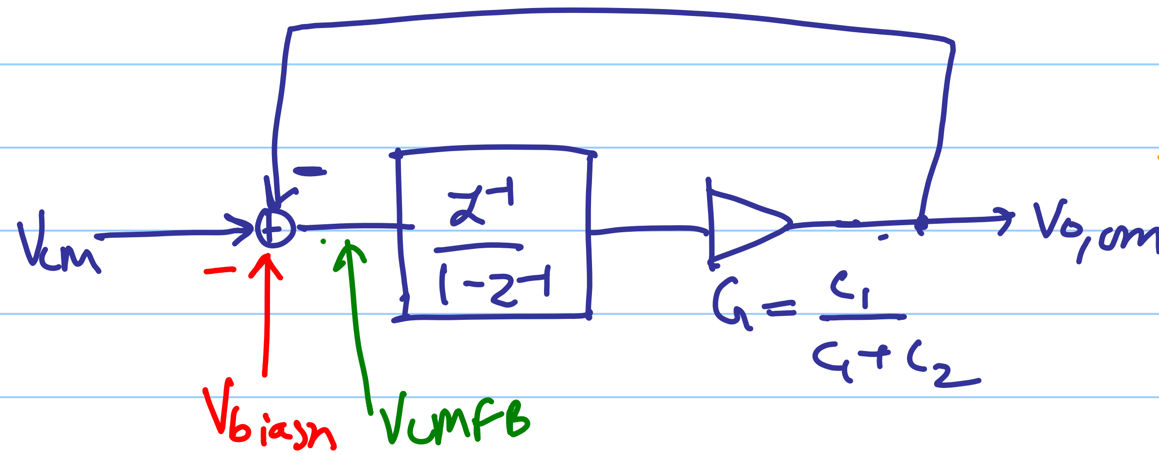


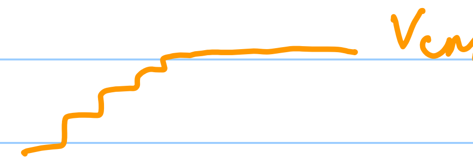


DT Integrator in a negative feedback

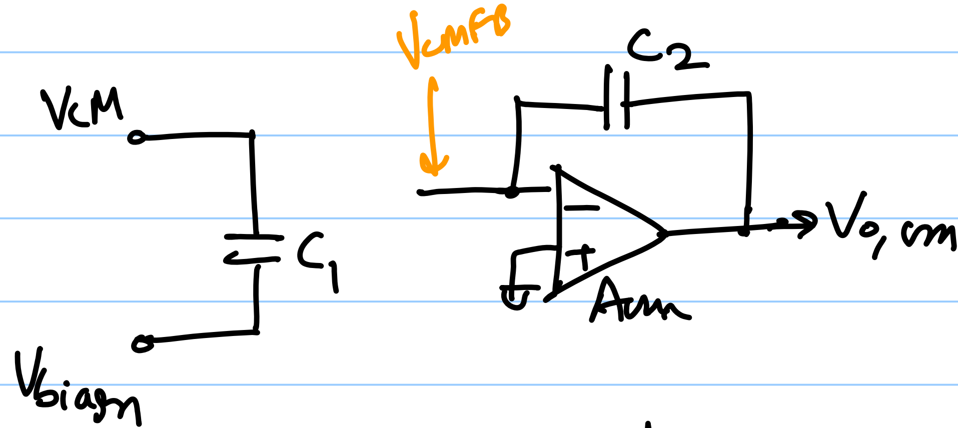


Assuming $|A_{cm}| >> 1$



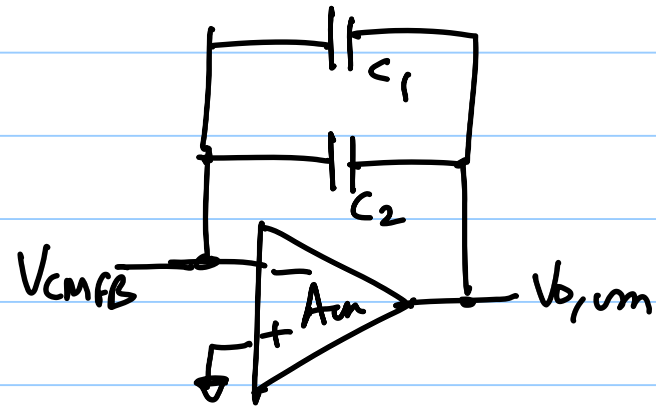


During ϕ_1



* C_1 is charged to $V_{cm} - V_{biasn}$
* $V_{o,cm}$ is undisturbed

During ϕ_2



* Charge sharing occurs b/w C_1 & C_2

In steady-state $V_{o,cm}$ becomes constant

$\Rightarrow$ C_1 doesn't transfer any charge into C_2

$$\Rightarrow \quad Q(\phi_1) \triangleq Q(\phi_2)$$

$$\frac{V_{op}+V_{om}}{2}$$

$$\cancel{C_1}\left(V_{cm} - V_{biasn}\right) = \cancel{C_1}\left(V_{o,cm} - V_{CMFB}\right)$$

$$\Rightarrow \quad V_{cm} - V_{o,cm} = \underbrace{V_{biasn} - V_{CMFB}}_{\text{systematic offset}}$$

If $V_{CMFB} \triangleq V_{biasn} \Rightarrow V_{o,cm} = V_{cm}$

If $V_{biasn} - V_{CMFB} = \Delta$

$$V_{o,cm} = V_{cm} - \Delta$$