CM - detectors $\rightarrow$ dual diff pair $\rightarrow$ resistive averaging $\rightarrow$ load the output but wide swing

- wide swing
- no resistive loading
- can we use capacitive CM - detector?
Switched Capacitor Circuits

Can total charge on this surface is preserved.

\[ V_0 = -\frac{V_{SC_2}}{V_{SC_1}} = -\frac{C_1}{C_2} \]

\[ \frac{V_o}{V_i} = \frac{-R_2}{R_1} \]

But there is no DC feedback path, \( V_o \) doesn't bias properly.
Switched Cap Resistor

\[
\phi_1 \quad \phi_2
\]

Complementary clock

\[\Delta Q = C(v_1 - v_2)\]

\[
I = \frac{\Delta Q}{T_s} = f_s \Delta Q = f_s C (v_1 - v_2)
\]

\[
I = \frac{v_1 - v_2}{R}
\]

\[
R = \frac{1}{f_s C}
\]

\[\times\] Discrete-time circuit
\( V_{in} = 0 \) due to the DC feedback

Input is sampled on \( C_1 \) & \( C_2 \)

*Since the charge on the virtual ground is preserved*
\[ Q = \underbrace{c_1(t) + c_2(t)}_{0} = -c_1 V_{in} - c_2 V_{out} = 0 \]

\[ \Rightarrow \quad \frac{V_{out}}{V_{in}} = -\frac{c_1}{c_2} \quad \text{after settling occurs} \]
**SC Integrator:**

Assume ideal switches

\[ \phi_1 \]

\[ \phi_2 \]

\[ nT \quad (n+\frac{1}{2})T \]

\[ \phi_1: \text{ sampling phase} \]

\[ C_2 V_{\text{out}[n]} \]

\[ Q = -C_1 V_{\text{in}[n]} \]

\[ \phi_2: \text{ integrator phase} \]

Voltage across \( C_1 \) tracks \( V_{\text{in}} \)

\( C_2 \) holds previous value
\[ Q[n] = -V_{in}[n] C_1 + (0 - V_{out}[n]) C_2 \]
\[ Q[n+\frac{1}{2}] = 0 \cdot C_1 - V_{out}[n+\frac{1}{2}] C_2 \]

Since the charge at the plate connected to \( V_A \) is conserved,

\[ Q[n+\frac{1}{2}] = Q[n] \]
\[ \Rightarrow V_{out}[n+\frac{1}{2}] C_2 = V_{in}[n] C_1 + V_{out}[n] C_2 \]

\[ V_{out}[n+1] = V_{out}[n+\frac{1}{2}] \Leftrightarrow C_2 \text{ is disconnected during } \phi_1 \]

\[ V_{out}[n] = V_{out}[n-1] + \frac{C_1}{C_2} V_{in}[n-1] \]

\[ V_{out}(z) = \frac{z^{-1} V_{out}(z) + \frac{C_1}{C_2} z^{-1} V_{in}(z)}{C_1 - C_2 z^{-1}} \]

\[ \frac{V_{out}}{V_{in}}(z) = \frac{\text{gain}}{C_1 - C_2 z^{-1}} \]

Delaying Discrete-time integrator
\[
\frac{1}{Z} \rightarrow \frac{c_1}{c_2} \rightarrow V_{out} \rightarrow V_{in} \rightarrow V_{out} \left[ n \right] \\
\Delta = \frac{c_1}{c_2} \cdot V_{in}(n)
\]
SC CMFB

CM Hay Circuit
DT Integrator in a negative feedback
Assuming $|A_{om}| >> 1$

- $V_{cm}$
- $V_{bias}$
- $V_{umfb}$

$A_{cm} = \frac{c_1}{c_1 + c_2}$
During $\phi_1$:

- $C_1$ is charged to $V_{CM} - V_{bias}$
- $V_{bias}$ is undisturbed

During $\phi_2$:

- Charge sharing occurs between $C_1$ and $C_2$

In steady state, $V_{bias}$ becomes constant

$\Rightarrow C_1$ doesn't transfer any charge into $C_2$
\[ Q(\phi_1) = Q(\phi_2) \]

\[ \sum_1 (V_{cm} - V_{biasn}) = \sum_1 (V_{b, om} - V_{cmFB}) \]

\[ \Rightarrow V_{cm} - V_{b, om} = V_{biasn} - V_{cmFB} \]

Systematic Offset

If \( V_{cmFB} = V_{biasn} \) then \( V_{b, om} = V_{cm} \)

If \( V_{biasn} - V_{cmFB} = \Delta \)

\[ V_{g, om} = V_{cm} - \Delta \]