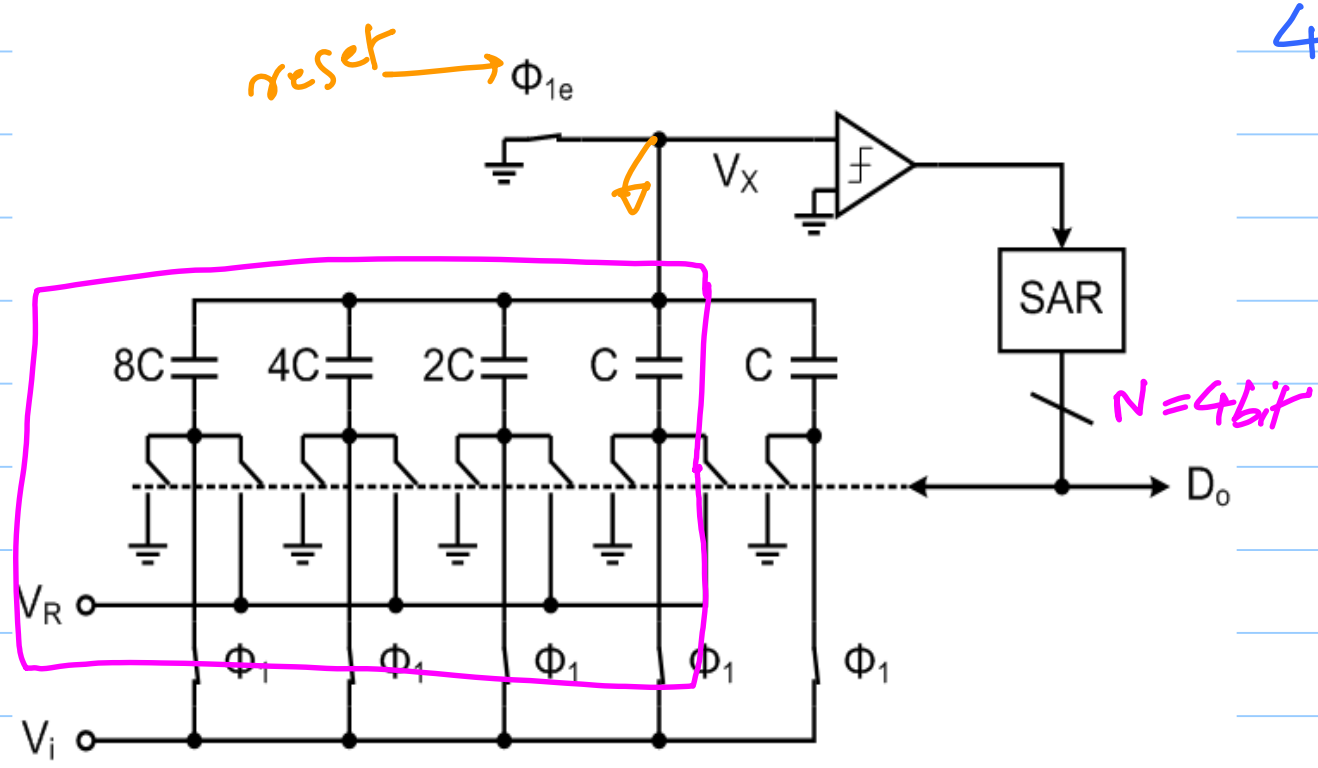
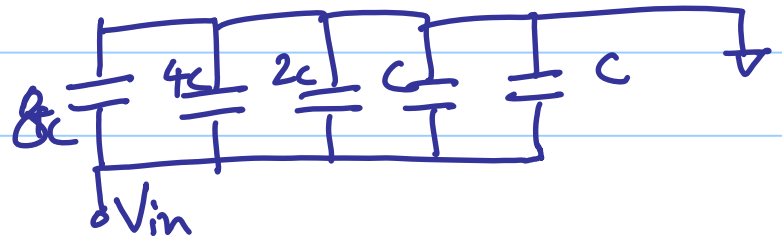
ECE 614 - Lecture 26

Note Title 12/4/2014

4-bit SAR



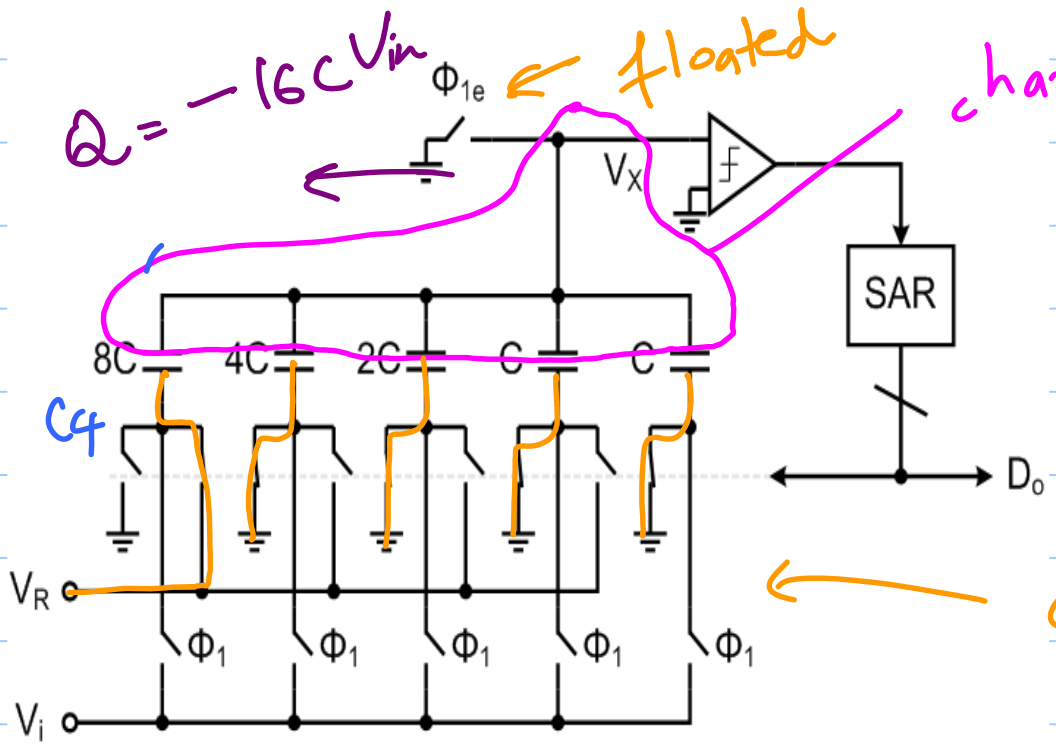
Capacitors sample the input, V_{in}, when $\phi_1 \Rightarrow 1$



$Q_{in} = 16C\,V_{in}$

total cap = 8 + 4 + 2 + 1 + 1 = 16C

$2^N C$



$Q = -16C V_{in}$ ← floated

charge is conserved at this surface

SAR = 1000

↑ MSB

← charge redistribution

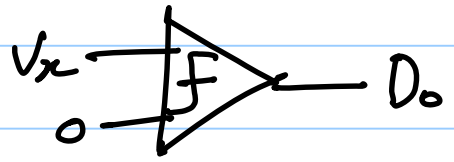
$Q = V_{in} \cdot 16C = (V_R - V_x) C_4 + (0 - V_x)(C_3 + C_2 + C_1 + C)$

$= V_R \cdot 8C - V_x \cdot 16C$

$$V_x = \frac{V_R \cdot 8C - V_{in} \cdot 16C}{16C} = \frac{V_R}{2} - V_{in}$$

$$\boxed{V_x = \frac{V_R}{2} - V_{in}}$$

MSB Test: V_x

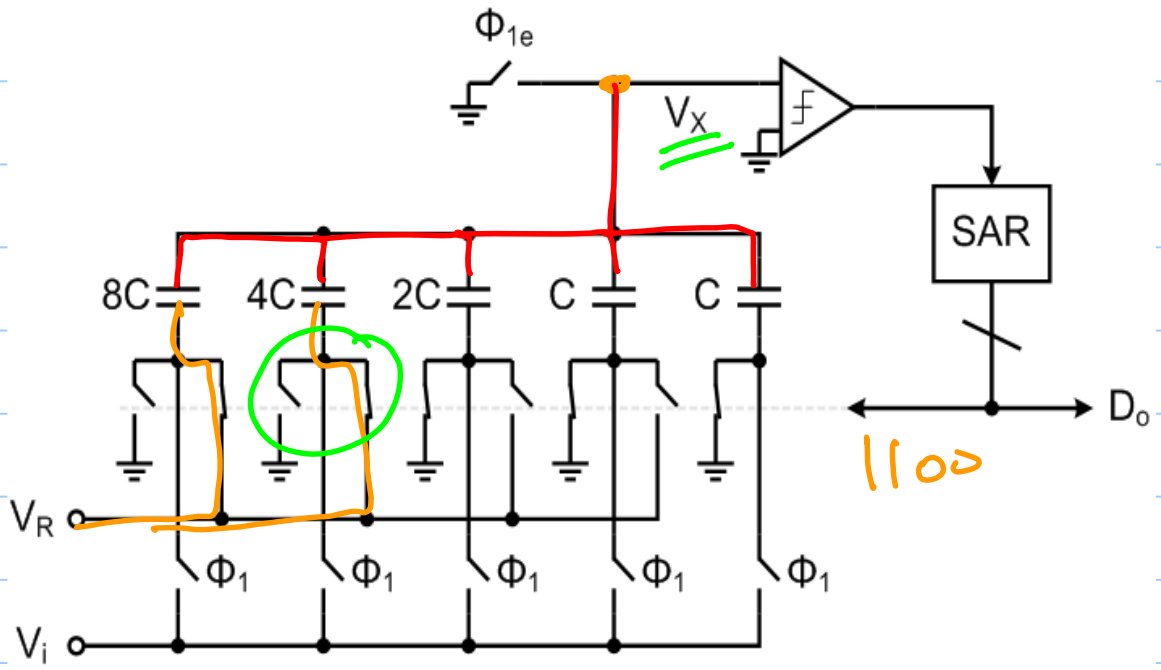


If $V_x < 0$, $V_{in} > \frac{V_R}{2} \Rightarrow$ MSB = 1 & C_4 remains Connected to V_R

SAR ↵ 1100

If $V_x > 0$, $V_{in} < \frac{V_R}{2} \Rightarrow$ MSB = 0 $\Rightarrow$ switch C_4 to ground

SAR ↵ 0100

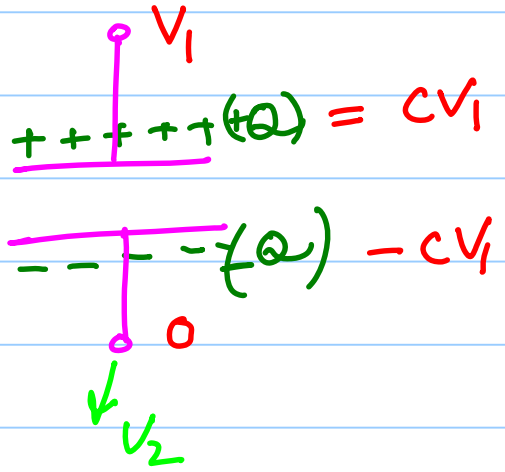


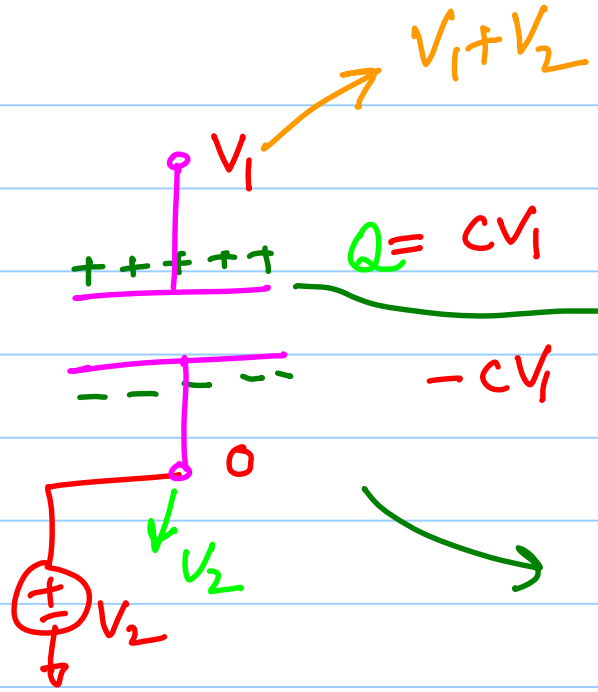
Still the "charge" at V_x is conserved

$$V_{in} \cdot 16C = (V_R - V_x)(C_{pt} + C_3) + (0 - V_x)(2C + C + C)$$

$$= 12C\,V_R - 16C\,V_x$$

$$\Rightarrow \quad V_x = \frac{3}{4} V_R - V_i$$





Skip

$Q = V_+ - V_-$

$= CV_1$

If $V_x < 0 \Rightarrow V_i > \frac{3}{4} V_R \Rightarrow C_3$ remains connected to V_R

SAR ↵ 1110

If $V_x > 0 \Rightarrow$ then $V_i < \frac{3}{4} V_R \Rightarrow C_3$ is switched to ground

SAR ↵ 1010

V_R ↵ set by V_{FS}

↵ limited by the switch linearity

Usually half clock cycle is for charge redistribution

other half clock cycle is for comparison + digital logic

Note that V_x always converges to 0.

↳ V_{os} of the comparator plays no role