\[ R \quad \Rightarrow \quad \frac{R}{V_{in}} = 4kT \]

\[ V_{out} = L \frac{Q}{C} \]

\[ Q_{in} = \frac{1}{2\pi RC} \]

\[ V_{out, n, rms} = \sqrt{\frac{4kT}{C}} \]
$V_{\text{in}}(t) = A \sin(\omega t)$

\[
\begin{align*}
\phi &= \frac{V_{\text{in}}[mT_s]}{\sigma} + V_{\text{noise}, \text{rms}} = \sqrt{\frac{kT}{c}} \\
\text{SNR} &= \frac{A^{\frac{3}{2}}}{kT/c} > 60 \text{dB} \\
\text{Quantizer} \Rightarrow \text{SQNR} &= (6.02 \cdot N_{\text{eff}} - 1.76) \text{dB} \\
\Rightarrow 60 \text{dB}
\end{align*}
\]
**MOSFET Noise**

\[ \overline{I_n^2} = 4kT \gamma g_m \leq \text{Thermal Noise} \]

\[ \gamma = \frac{2}{3} \quad \text{for Long-channel} \]

\[ \leq 2.5 \quad \text{for short-channel (180nm)} \]

\[ \leq f(V_{DS}) \leq \frac{V_{DS}}{V_{DS}} \]

For handcalc: \[ \overline{I_n^2} = \frac{8}{3} kT g_m \quad \text{for} \quad \gamma = \frac{2}{3} \]

\[ \frac{A^2}{H_2} \]
Example: Max noise voltage from a MOSFET

\[ V_{N_{\text{out}}}^2 = \frac{8}{3} kT g_m \sigma_0^2 \]

for constant \( \sigma_0 \)

\( g_m \) minimize
\[ R_g = \frac{1}{3} R_{D,Poly} \cdot \left(\frac{W}{L}\right) \]

\(\Rightarrow\) Distributed gate resistance

To minimize noise from \(R_C\)

\(\Leftrightarrow\) Multi-finger layout

\(\&\) we will neglect these thermal noise sources for simplicity.
Flicker Noise:

- Bulks component
- Thermal component
- Dangling bond at the interface
- Traps, or extra energy state
- Charge carriers get trapped at lower energy states and released by higher energy states.
$\log_{10}(\overline{v_n^2})$ vs $\log(f)$

"Flicker Noise"

\[ \overline{v_n^2} = \frac{K}{\cos WL} \cdot \frac{1}{f} \]

Flicker Noise

\[ \frac{1}{f} \rightarrow \text{noise} \]

Large Area \( WL \rho = \overline{v_n^2} + \frac{1}{\Delta} \)
key process dependent parameter \( \Rightarrow 10^{-25} \) V in [Razavi]

\( \Rightarrow \) more frequent at lower frequencies \( (\frac{1}{f}) \)

\( \Rightarrow \) doesn't depend on bias condition 

\( \Rightarrow \) only on WL area

\( \Rightarrow \) To decrease \( \frac{1}{f} \)-noise \( \Rightarrow \) increase device area

\( \Rightarrow \) In 180nm CMOS \( \Rightarrow \) PMOS exhibit less 

flicker noise than NMOS.

\( \Rightarrow \) holes were carried in a 

* In present technologies buried channel

\( \Rightarrow \) verify with process datasheet
\[ \overline{I_n^2} = \frac{8}{3} kT g_m \]

Reflected thermal noise to a noise voltage source at the gate.

\[ \overline{V_n^2} = \frac{I_n^2}{g_m^2} = \frac{8}{3} \frac{kT}{g_m} \]

10 \log(\overline{V_n^2})

Total noise

Corner frequency

\[ f_c \]

\[ f_c \] tells us which part of the signal band is most corrupted by the flicker noise.
\[\sqrt{I_n^2} = \frac{8}{3} \frac{K T}{g_m} = \frac{K}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f_c}\]

\[f_c = \frac{K}{C_{ox} \cdot W \cdot L} \cdot \frac{3}{8kT}\]

\[f_c \text{ depends on device bias current } (g_m) \text{ and process technology}\]

\[f_c = 800kHz \text{ for } f_m \leq 0.25\mu m\]

\[g_m \text{ nano-CMOS } \geq 1 - 100 \text{ MHz}\]
\[ V_{\text{noise, out}}^2 = \left[ \frac{8}{3} \beta \frac{kT}{C_{ox}} + \frac{k}{C_{ox}} \frac{1}{2} g_m^2 + \frac{4kT}{R_0} \right] R_0^2 \frac{V^2}{H^2} \]

\[ \text{total noise current} \]

\[ \text{noise circuit} \rightleftharpoons \text{small-signal circuit with the noise source} \]

\[ R_D \ll \beta \]
Representing Noise in Circuits

\[ \text{noise at the output } V_{\text{out}} \uparrow = \sqrt{V_{n,\text{out}}^2 \cdot A^2} \]

- \( A \uparrow \) leads to a circuit becoming noisier.
- But, \( A \) also amplifies the signal.
- \( \Rightarrow \) the output SNR is independent of \( A \).
- \( \Rightarrow \) We want to get the circuit gain out of the noise comparison.
Specify the "input referred noise" of the circuit. NOT the output noise.

Noisy circuit

Noisy 2-port

Noisier circuit