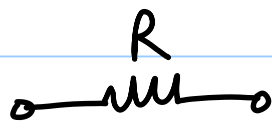
ECE 614 - Lecture 10

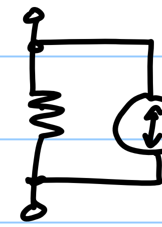
Note Title 9/25/2014



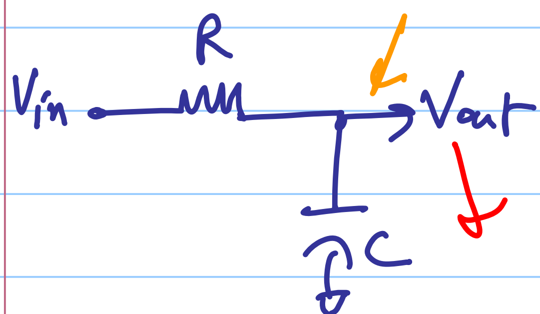
$\Rightarrow$

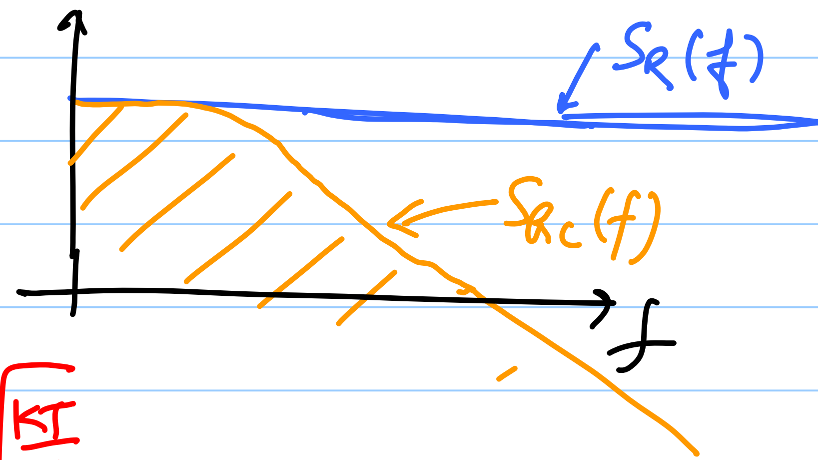
$\overline{v_n^2} = 4kTR$

OR



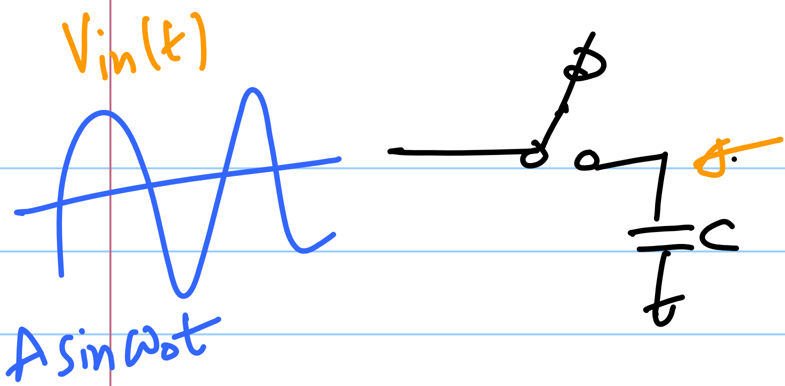
$\overline{i_n^2} = \frac{4kT}{R}$





$f_{3dB} = \frac{1}{2\pi RC}$

$V_{out,n,rms} = \sqrt{\frac{kT}{C}}$



$V_{in}[nT_s]$

$+$

$V_{o,noise,rms} = \sqrt{\frac{kT}{C}}$

$$SNR = \frac{A^2/2}{kT/C} > 60dB$$

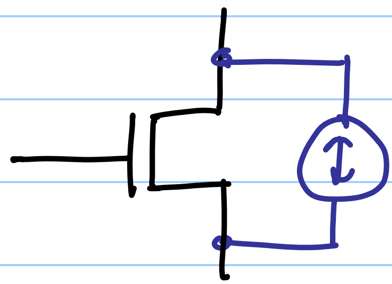
Quantizer $\Rightarrow$ $SQNR = (6.02\, N_{eff} - 1.76)\, dB$

$\uparrow$ 10

$\geq 60dB$

MOSFET Noise

 $\frac{4kT}{R}$



$\overline{I_n^2} = 4kT\gamma g_m$ ⟸ Thermal Noise

$\gamma = \frac{2}{3}$ for Long-channel

$\simeq 2.5$ for short-channel (180nm)

$\simeq f(V_{DS})$ ⟸ also varies with some extent
V_{DS}

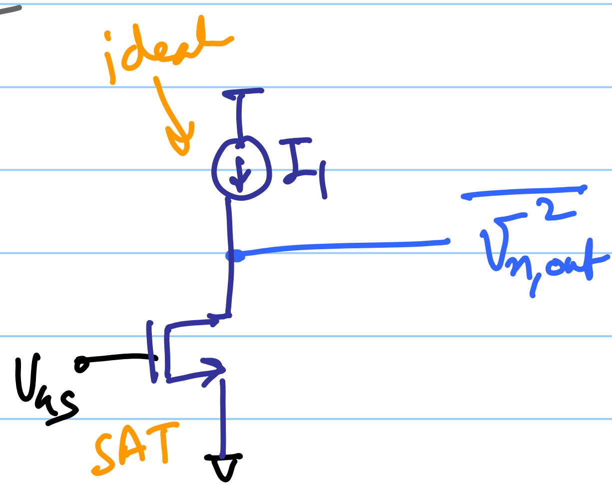
for handcalcs ⇒ $\overline{I_n^2} = \frac{8}{3}kTg_m$ for $\gamma = 2/3$

$\frac{A^2}{Hz}$

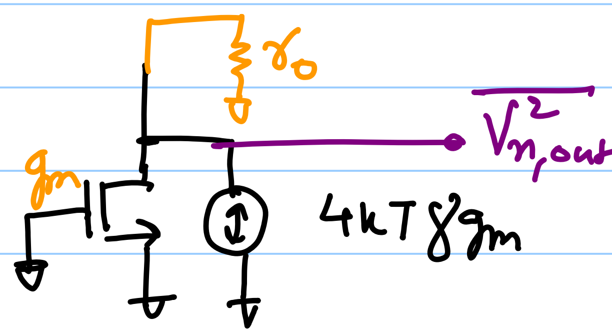
/home/pdks/IBM_PDK/8RF ⇐ docs

Spice model

Ex. Max noise voltage from a MOSFET

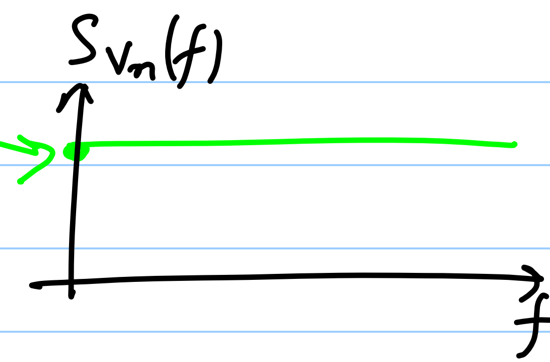


noise circuit

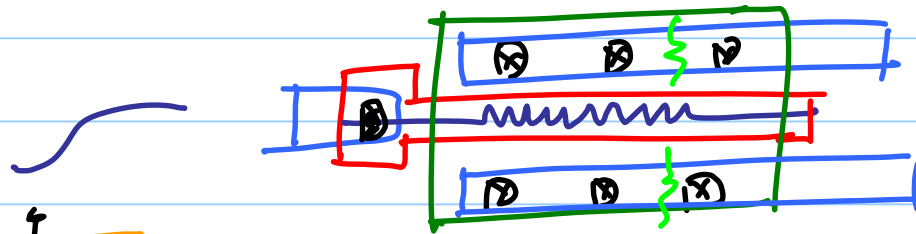


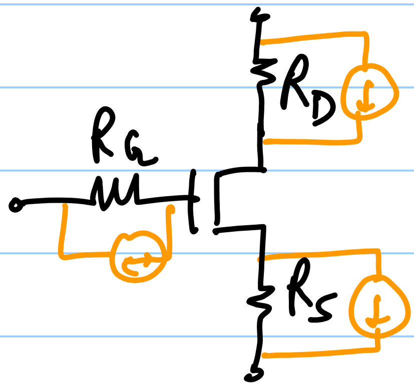
Noise Power density:

$$\overline{V_{n,out}^2} = \overline{I_n^2} \cdot r_o^2 = \frac{8}{3} kT g_m r_o^2$$



for constant r_o minimize g_m



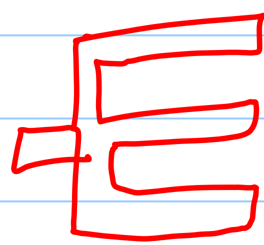


$$R_G = \frac{1}{3} R_{\square,poly} \cdot \left(\frac{W}{L}\right)$$

$\Uparrow$

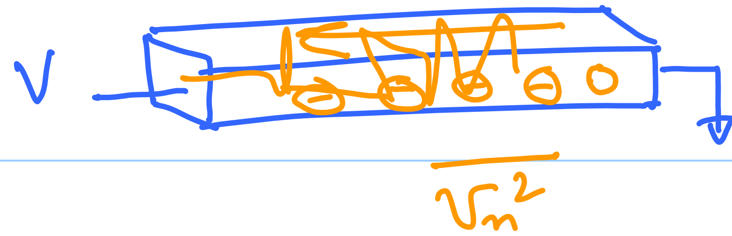
Distributed gate resistance

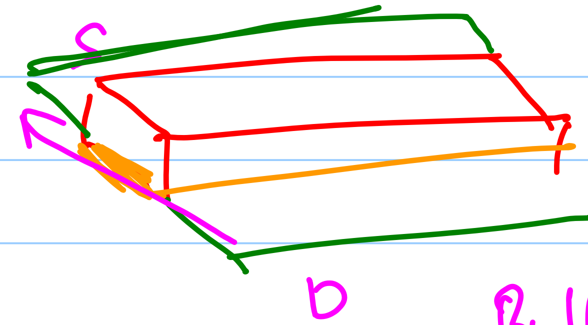
To minimize Noise from R_G $\Rightarrow$ Multi finger layout



* We will neglect these thermal noise sources for simplicity.

Flicker Noise:



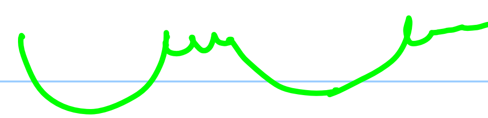


Bulk component
↳ Thermal

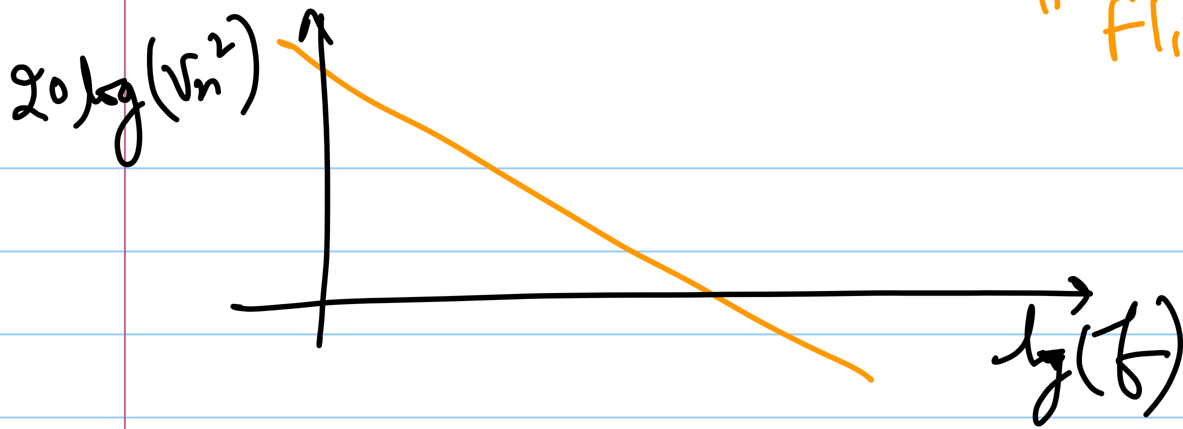
Dangling bond at the interface

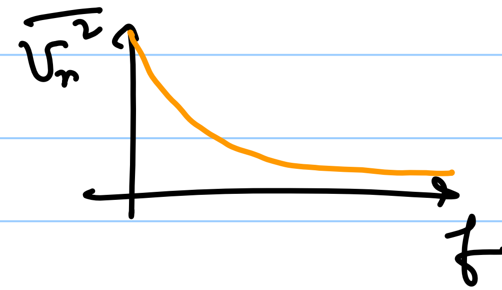
* Traps, or extra energy state

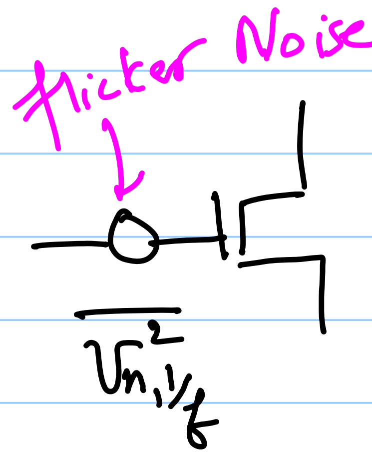
* charge carriers get trapped an then released by these energy states



"Flicker Noise"







$$\overline{V_n^2} = \frac{K}{C_{ox} WL} \cdot \frac{1}{f}$$

$1/f \rightarrow$ noise

Large Area $\Rightarrow$ $WL \uparrow$ $\Rightarrow$ $\overline{V_n^2} \downarrow$

$K \Rightarrow$ process dependent parameter

$\Rightarrow 10^{-25}\ V^2F$

in Razavi

↳ more frequent at lower frequencies ($1/f$)

↳ doesn't depend on bias condition

↳ only on WL area

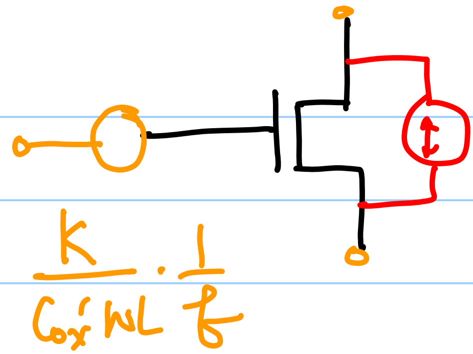
$\Rightarrow$ To decrease $1/f$-noise $\Rightarrow$ increase device area

$\Rightarrow$ In 180nm CMOS $\Rightarrow$ PMOS exhibit less flicker noise than NMOS.

$\Rightarrow$ holes were carried in a buried channel

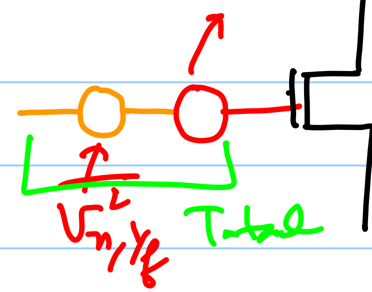
* In present technologies

↳ verify with process datasheet



$\overline{I_n^2} = \frac{8}{3}kT g_m \Rightarrow$

$\overline{V_n^2} = \frac{\overline{I_n^2}}{g_m^2} = \frac{8}{3}\frac{kT}{g_m}$



Reflected thermal noise to a noise voltage source at the gate

↑ Corner frequency

* f_c tells us which part of the signal band is most corrupted by the flicker noise

$\overline{V_n^2} \Rightarrow \quad \frac{8}{3}\frac{kT}{g_m} = \frac{K}{C_{ox}'WL}\cdot\frac{1}{f_c}.$

$$\Rightarrow \quad \boxed{f_c = \frac{K}{C_{ox}'WL}\, g_m \cdot \frac{3}{8kT}}$$

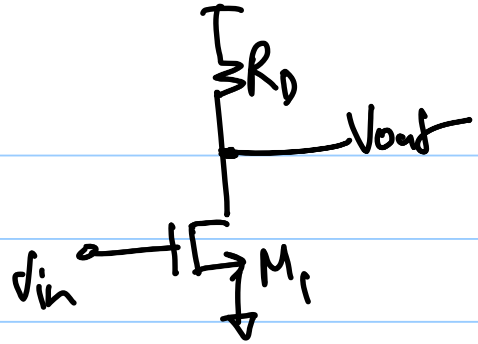
↑ depends on device bias current (g_m)

& process technology

$f_c \simeq 500\text{kHz} - 1\text{MHz}$ for $\leq 0.25\,\mu m$

In nano-CMOS $\Rightarrow$ $1 - 100\text{ MHz}$

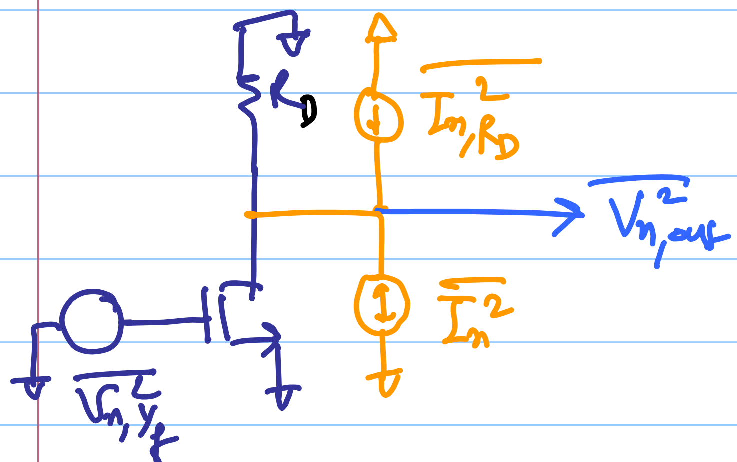
Ex.

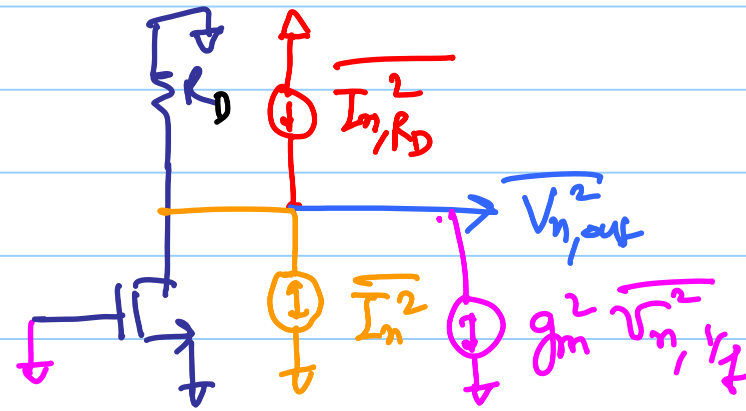


noise circuit
$\Rightarrow$ small-signal circuit with the noise sources

$\overline{V_{n,out}^2} = ?$

$R_D \ll r_o$

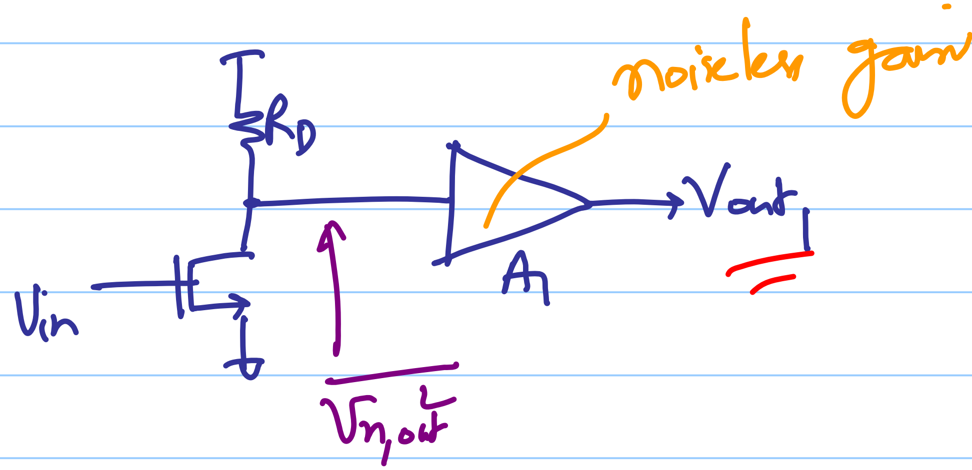




bring 1/f noise to the output as a noise current source

$$\overline{V_{n,out}^2} = \Big[\underbrace{\frac{8}{3}kTg_m + \frac{K}{C_{ox}WL}\frac{1}{f}g_m^2 + \frac{4kT}{R_D}}_{\text{total noise current}}\Big]R_D^2 \qquad \frac{V^2}{Hz}$$

Representation of Noise in Circuits



noise PSD at the output $V_{out,1}$ $\Rightarrow$ $\overline{V^2_{n,out}} \cdot A_1^2$

$A_1 \uparrow$ $\Rightarrow$ Circuit becomes noisier ?!

But A_1 also amplifies the signal

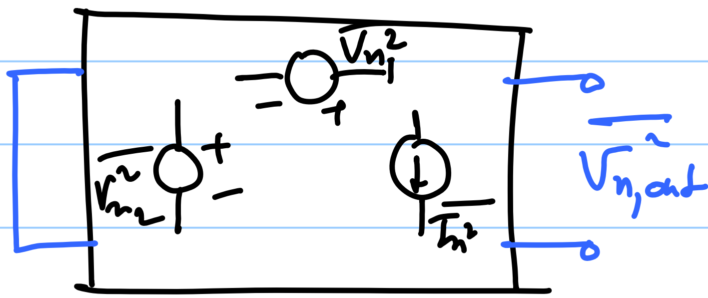
$\Rightarrow$ the output SNR is independent of A_1

$\Rightarrow$ We want to get the circuit gain out of the noise comparison

⇒ Specify the "input referred noise" of the circuit.

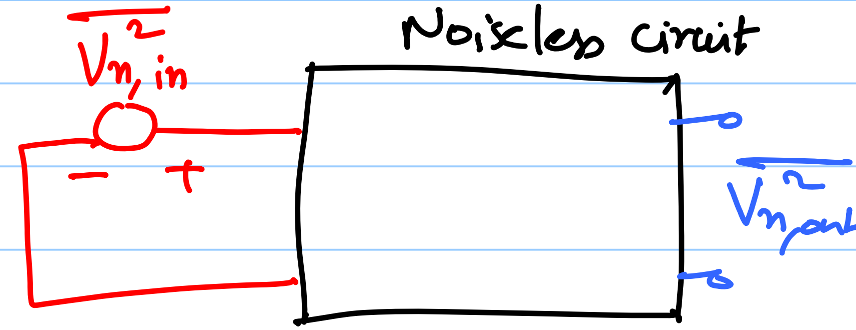
⇒ NOT the output noise

noisy circuit



⇒

Noiseless circuit



Noisy 2-port