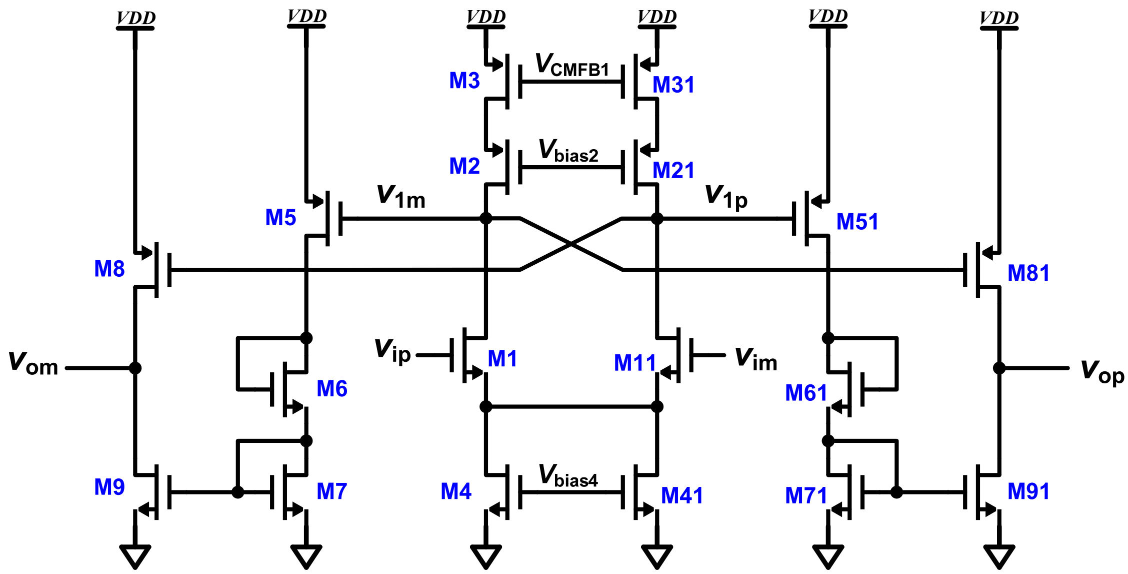
ECE 614 Advanced Analog Integrated Circuit Design
Sample Midterm Exam
Nov 6, 2012 Name: ____________________

Open Book, Open Notes, Closed Computer.
Clearly show your steps to get partial credit.
State clearly any assumptions made.
This exam has 4 questions, for a total of 100 points.

Useful data:
$k = 1.38 \times 10^{-23}\, J/K$
$T = 300\, K$

Expressions for pole-splitting in a second-order system
$A_v = g_{m1} R_1 g_{m2} R_2$
$\omega_{p_1} \approx \frac{1}{g_{m2} R_2 R_1 C_c}$
$\omega_{p_2} \approx \frac{g_{m2} C_c}{C_2 (C_1 + C_C) + C_C C_1} \propto \frac{g_{m2}}{C_2}$
$\omega_{un} \approx \frac{g_{m1}}{C_C}$

1. Consider the two-stage fully-differential opamp designed for continuous-time (CT) operation shown below. Standard notations for bias voltages apply. *Be clear and legible in your answers.*



(a) (2 points) Draw differential-mode (DM) compensation networks in the above figure (LHP zero should be pushed out to ∞).

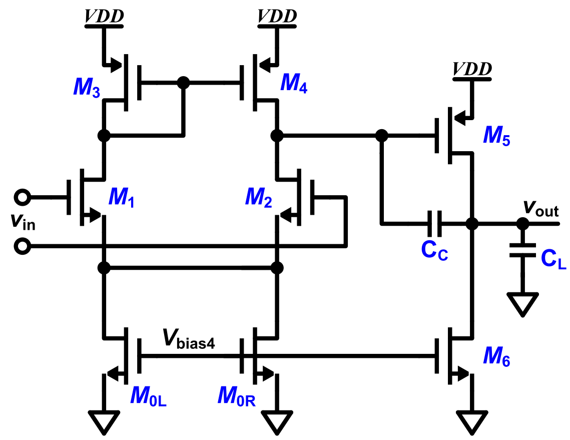
(b) (10 points) Sketch **appropriate** CT common-mode feedback (CMFB) circuits for the first- and second- gain stages which will not adversely impact the opamp performance. Show transistor-level sketches and **compensation** used in the CMFB circuits.

Important: *Do not use source-followers and keep the CMFB circuits simple.*

(c) (10 points) Sketch the individual common-mode equivalent circuits for both the stages and label the nodes contributing low-frequency poles.

(d) (8 points) Write expressions for the DM and the first-stage CM open-loop gains (A_{DM} and A_{CM_1}) and unity-gain frequencies ($\omega_{u,DM}$ and ω_{u,CM_1}) for the two loops. **Hint:** All the loops exhibit 2^{nd}-order response.

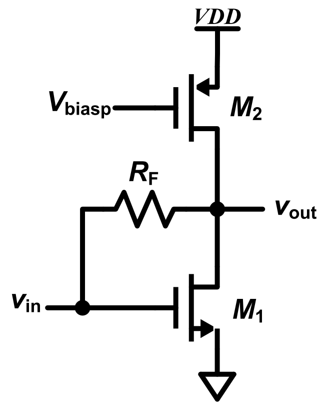
2. For the two-stage opamp shown below:



(a) (10 points) Find the input-referred thermal noise voltage, $\overline{V_{n,in}^2}$, at low frequencies. Use symbolic variables $g_{m_k}$and r_{o_k} for the transistors as shown in class. Clearly show the steps, and *present the final answer in a concise form.*

(b) (10 points) Find the input-referred flicker noise voltage, $\overline{V^2_{n,in,\frac{1}{f}}}$.

3. For the feedback amplifier shown below assume the transistors are biased in saturation. Use data: $g_{m1} = g_{m2} = 100\frac{mA}{V}$, $r_{o1} = 100k\Omega$, $r_{o2} = 300k\Omega$ and $R_F = 1k\Omega$. Show *the final expressions as well as the numerical results for your answers.*



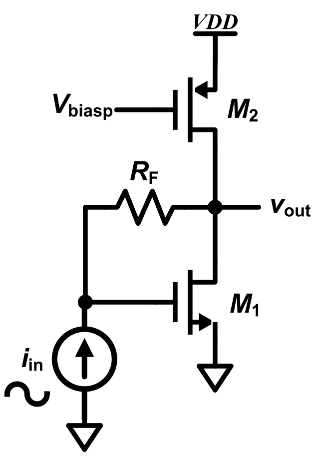
(a) (3 points) Calculate the voltage gain $A_v = \frac{v_{out}}{v_{in}}$ of the amplifier.

(b) (3 points) Calculate the trans-impedance gain $R_T = \frac{v_{out}}{i_{in}}$ of the amplifier

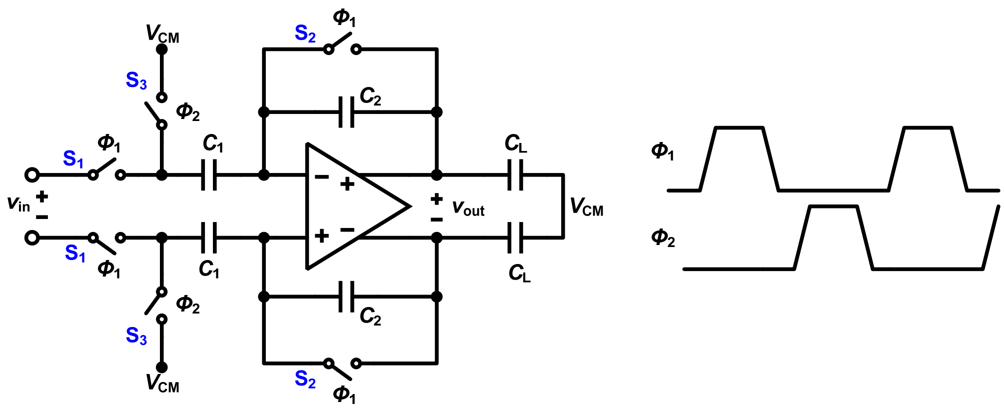
(c) (7 points) Calculate the input-referred thermal noise voltage ($\overline{V_{n,in}^2}$)

(d) (7 points) Calculate the input-referred thermal noise current ($\overline{I_{n,in}^2}$)

(e) (5 points) A sinusoidal current input (i_{in}) is applied to use the above amplifier as a trans-impedance amplifier (TIA). Assuming a circuit bandwidth of of $f_B = 1\,GHz$, find the minimum peak-to-peak input current ($i_{in,p-p}$) needed to achieve a signal-to-noise ratio, $SNR \geq 40\,dB$.



4. Consider the fully-differential implementation of a switched-capacitor amplifier shown below. The output CM-level of the opamp is set using a fast CMFB circuit at V_{CM}, and the inputs (v_{in}) are balanced around V_{CM}. Use data: $C_1 = 2\,pF$, $C_2 = 0.5\,pF$, the input capacitance $C_{in} = 0.1\,pF$ and $C_L = 1\,pF$. The non-overlapping clocks have a 40% *duty cycle*.



(a) (5 points) Find the nominal differential gain $A_{sc} = \frac{v_{out}}{v_{in}}$ of the SC amplifier. Is the amplifier inverting or non-inverting?

(b) (5 points) Modify the above circuit to minimize the effects of charge injection from the switches.

(c) (5 points) What is the minimum opamp gain (A_v), in dB, required for a gain error $\epsilon < 0.1\%$?

(d) (5 points) Recall that the time-constant for the transient settling in the amplification phase is given by

$$\tau_{amp} = \frac{C_L C_{eq} + C_L C_2 + C_{eq} C_2}{G_m C_2}$$

where $C_{eq} = C_1 + C_{in}$. The single-stage opamp is be modeled using $G_m = 10 \frac{mA}{V}$ and $R_{out} = 1M\Omega$ as discussed in class. Assuming first-order linear settling, what is the maximum clock frequency (f_s) at which the amplifier can be operated with 1% settling accuracy?

(e) (5 points) Estimate the input referred **rms** thermal noise voltage for the amplifier. Assume the opamp noise is negligible. **Hint:** Estimate the mean-square noise for single-ended equivalent and multiply by 2.