Homework 5

ECE 614 – Advanced Analog IC Design (Fall 2014)

Due on Tuesday, Oct 22, 2014

Problem 1: Noise Simulations:

1. Simulate input referred noise of a resistive voltage divider formed using two 1k resistors and compare the results with your hand-calculations.

2. Make one of the resistors noiseless in your simulation and repeat part (1).

3. Load the output of the divider in part (1) with a 1pF capacitor and find the output rms noise voltage ($V_{n,out,rms} = \sqrt{\int \overline{V_{n,out}^2}(f) \cdot df}$). Compare with hand-calculations.

4. Size a CMOS switch to charge and discharge a 1pF capacitor using a 10 MHz clock. Estimate and simulate (try PSS with PNOISE) the output rms noise voltage ($V_{n,out,rms}$) stored in the capacitor at the end of tracking phase (i.e. when the clock goes low). Will flicker ($\frac{1}{f}$) noise have any effect on the sampled noise?

Problem 2: For the opamp designed in HW3:

(a) For the bias current and sizing of the input diff-pair (NMOS) transistors used, plot the input referred noise PSD ($\overline{V_n^2}$). What is the corner frequency for the flicker noise? For a PMOS sized for the same g_m as the NMOS, plot and compare the noise PSD.

(b) Simulate and plot the output noise PSD ($\overline{V_{n,out}^2}$) and the input referred noise PSD ($\overline{V_{n,in}^2}$) with $\frac{V^2}{Hz}$ and $\frac{V}{\sqrt{Hz}}$ units. Calculate the RMS output noise voltage ($V_{n,out,rms} = \sqrt{\int \overline{V_{n,out}^2}(f) \cdot df}$) in nV for the closed-loop amplifier.

(c) Which transistor pairs are the major noise contributors? What changes would you make in your design to reduce input referred noise voltage by 25%?

(d) Run a noise report, excluding the bias resistors. Plot a pie chart of noise contribution from each of the *transistor pairs* and compare with part (c). Use a frequency setting of >10 MHz in the tool to avoid flicker noise.