Homework 4

ECE 614 - Advanced Analog IC Design (Fall 2014)

Due on Tuesday, Oct 14, 2014

Problem 1: In the opamp designed in HW3, replace the common-mode feedback circuits by switched-capacitor common-mode CMFB. You can relax the load specification to 1 pF. Use a clock frequency (f_s) of 5 MHz. Appropriately size the switches and capacitors in the SC-CMFB circuit. Use PSS and PSTB for sampled circuit stability analysis.

- (a) Discuss the impact of sizing of C_1 and C_2 capacitors in SC-CMFB on loop-stability and transient settling.
- (b) Plot the following results:
 - 1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
 - 2. Common-mode loop (s) gainmagnitude and phase. Indicate the phase margin.
 - 3. Transient response of the inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times).
 - 4. Transient response of the inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times).

Problem 2: Use the opamp configuration in problem 1 in the sample-and-hold circuit shown in Figure 1. Use (f_s) of 5 MHz and $C_H = C_L = 0.5$ pF. You may use ideal switches with on resistance of $1k\Omega$.



Figure 1: Fully-differential opamp in feedback configuration.

- (a) Verify loop DM and CM loop-stability and show relevant plots (Be creative with simulation test-benches here).
- (b) Simulate the transient reponse of the circuit for a sinusoidal input with $1.2 V_{pp}$ differential amplitude and input frequencies of $f_{in} = \frac{1}{4}$ MHz and $\frac{11}{4}$ MHz. Plot the output waveforms.