Homework 3

ECE 614 – Advanced Analog IC Design (Fall 2014)

Due on Tuesday, Oct 7, 2014

Problem 1: A two-stage fully-differential Opamp needs to be designed to realize an amplifier of gain 2 and a closed-loop bandwidth of $f_{3dB,CL} = 20$ MHz driving a $C_L = 2\,pF$ load with rail-to-rail output swings. The open-loop DC gain of the opamp should be greater than $A_{OL} > 60\,dB$. The Use $R_1 = 10\,k\Omega$. Assume that the common mode reference voltage $V_{CM} = \frac{V_{DD}}{2} = 0.6V$ is available from a bandgap reference (BGR). Use zero canceling resistors in series with the Miller compensation capacitors.

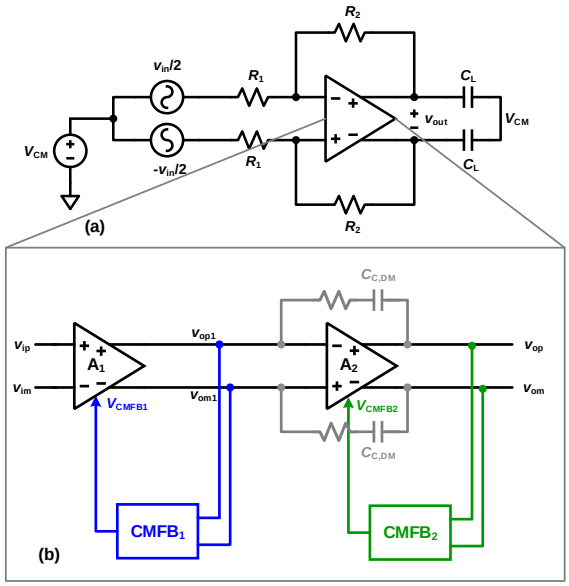

Figure 1: A two-stage fully-differential opamp in feedback configuration.

Select the appropriate topologies for the first and second stage amplifiers and individual common mode feedback (CMFB) loops. Ensure that there is no systematic offset in your CMFB loops. Compensate all the three feedback loops for a phase margin of $\geq 60°$.

Clearly show/tabulate all the transistor sizes and the component values. Use STB analysis for all loops by appropriately placing the CMDM probe. Show all relevant testbench shematics. Show results for at least **tt** and **ssf** corners.

(a) Briefly discuss you design choices with relevant calculations and plots. Draw the differential half circuit for the opamp and the common mode equivalent circuits for both the CMFB loops.

(b) Plot the following results with comments:

1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
2. Differential closed loop gain-magnitude and phase. Indicate the -3 dB bandwidth.
3. First stage common-mode loop gain-magnitude and phase. Indicate the phase margin.
4. Second stage common-mode loop gain-magnitude and phase. Indicate the phase margin.
5. Transient response of the inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times)
6. Transient response of the inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times)