Homework 1

ECE 614 – Advanced Analog IC Design (Fall 2014)

Due on Tuesday, Sep 23, 2014

Note: Use the provided 130nm CMOS process with $V_{DD} = 1.2\,V$ for all the problems. Clearly show your neatly drawn schematics with transistor types and sizes. Present your calculations and result plots with proper labels and annotation.

Problem 1: Design a single-stage fully-differential Opamp for a closed-loop gain of $A_{CL} = 2$ and a closed-loop bandwidth of $f_{3db,CL} = 10$ MHz when driving $C_L = 1\,pF$ load, as shown in Fig. 1. The open-loop DC gain of the opamp should be greater than $A_{OL} > 25\,dB$. Use $R_1 = 10\,k\Omega$. Use a common mode reference voltage $V_{CM,ref} = \frac{V_{DD}}{2} = 0.6V$. Note that you will need to modify the opamp schematic for the desired specifications (with cascoding).

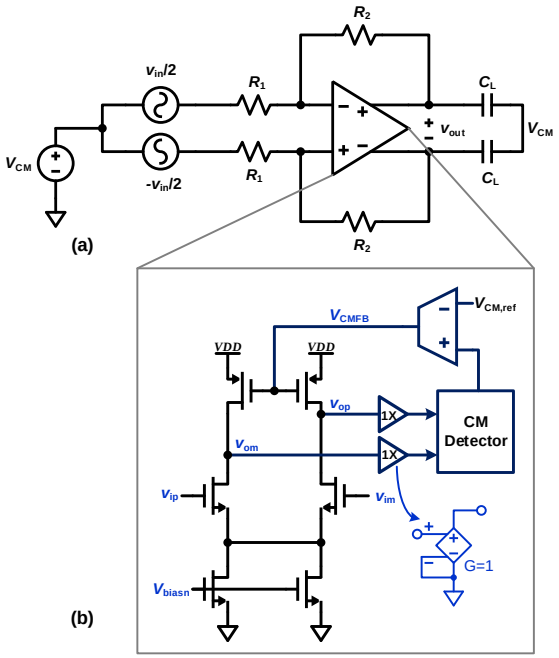

Figure 1: (a) A fully-differential opamp in feedback configuration, (b) illustrative schematic of the FD opamp (your topology may be different).

(a) In this part, use a resistive averaging CM-detector. To isolate the effect of resistive loading from R_{cm}, use ideal single-ended voltage buffers to study CMFB operation as shown in Fig. 1 (b). Compensate all the feedback loops with a phase margin of $\geq 60°$ and size the error amplifier to avoid any systematic offset. Clearly show/tabulate all the transistor sizes and the component values. Use STB analysis for all loops by appropriately placing the CMDM probe. Show all relevant test-bench schematics. Show results for at least **tt** and **ssf** corners.

Plot the following results with pertinent comments :

1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
2. Differential closed loop gain-magnitude and phase. Indicate the -3 dB bandwidth.
3. Common-mode loop gain-magnitude and phase. Indicate the phase margin.
4. Transient response of the inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times)
5. Transient response of the inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times.

(b) In part (a), what happens when the ideal voltage buffers are removed? Show with relevant plots.

(c) Repeat part (a) with a dual diff-pair CM-detector (remove the ideal buffers). Study and demonstrate the limitations due to the lower input range of this detector.