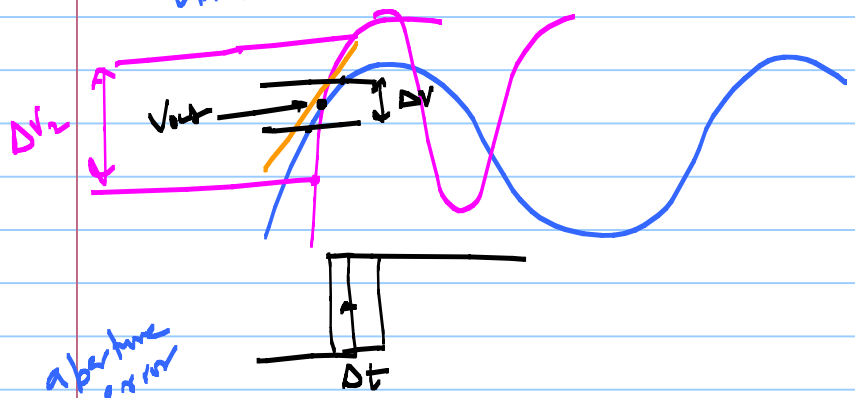
ECE 614 - Lecture 24

Note Title 12/4/2012

Sampling jitter

$V_{in} = A \sin(2\pi f_{in} t)$

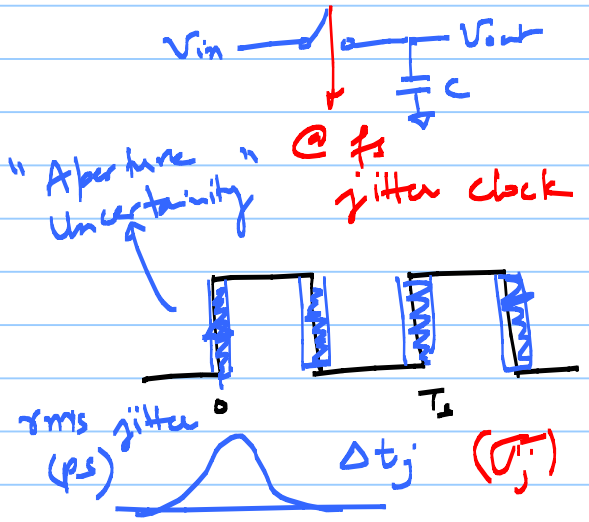


$$\Delta V = \frac{d}{dt}(V_{in}) \cdot \Delta t_j$$

$$= 2\pi A f_{in} \cos(\omega_{in} t) \cdot \Delta t_j$$

ADC Noise sources

* Quantization
* Thermal / 1/f
* distortion
* clock jitter



$$E(\Delta V^2) = (2\pi A f_{in})^2 E(\omega^2 \omega_{n,t}) \cdot E(\Delta t_j^2)$$

$$\overline{v_e^2} = (2\pi A f_{in})^2 \cdot \frac{1}{2} \cdot \sigma_j^2$$

$\overline{v_e^2}$ → noise power due to jitter

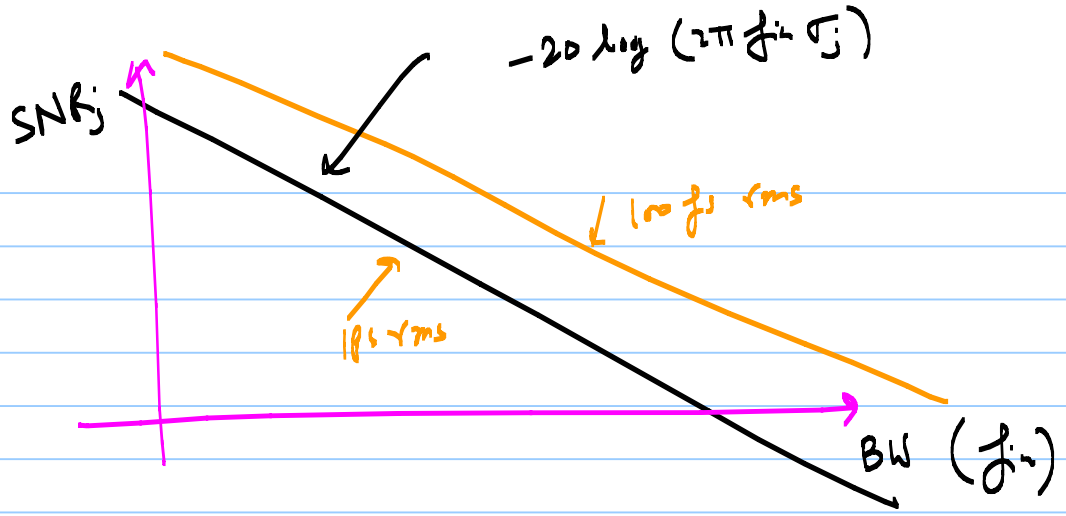
$$SNR_j = 10 \log_{10}\left(\frac{P_{sig}}{P_{jitter,noise}}\right)$$

$$= 10 \log_{10}\left(\frac{A^2/2 \; 1}{(2\pi f_{in})^2 A^2 \sigma_j^2}\right)$$

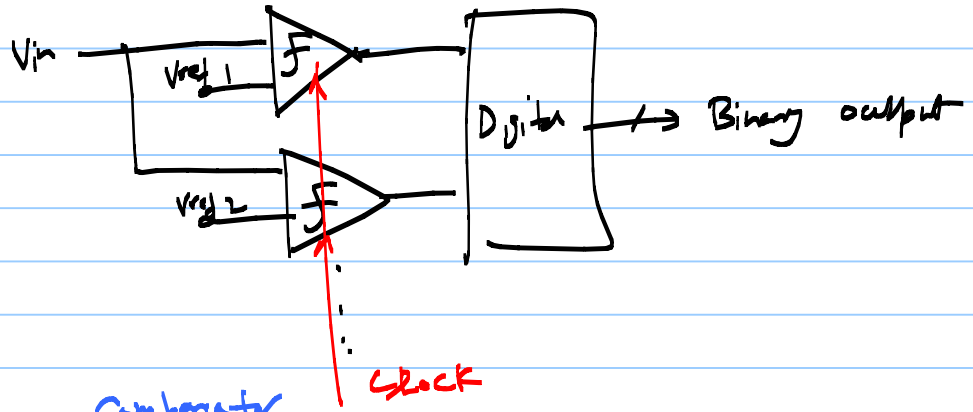
$$\boxed{SNR_j = -20 \log_{10}(2\pi f_{in} \sigma_j)}$$

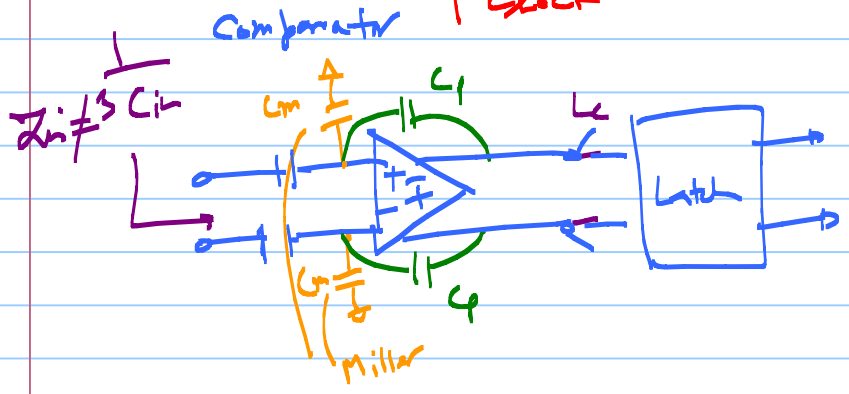
$\sigma_j \leftarrow$ low-jitter clock

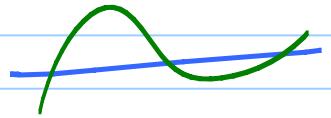
$f_{in} \uparrow \Rightarrow SNR_j \downarrow$


SNRj
-20 log (2π fc σj)
10log fc rms
10log rms
BW (fc)

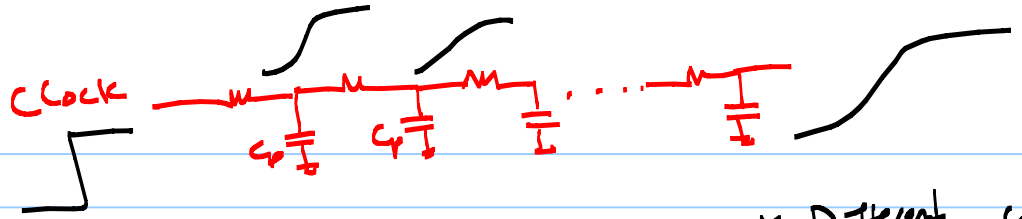
* Do we need a S/H ?

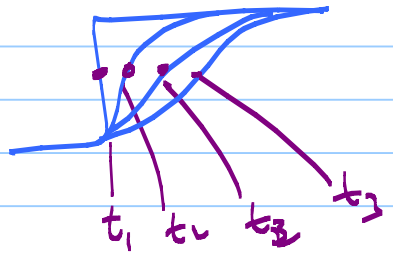




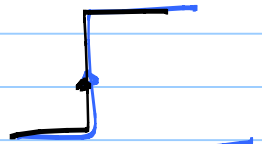


⇒ clock skew

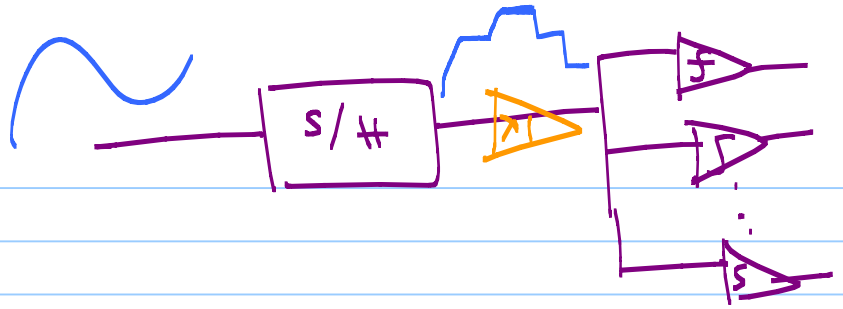




* Different comparators sample at different instances of time



* fast edges :



* Dedicated S/H for better Dynamic performance