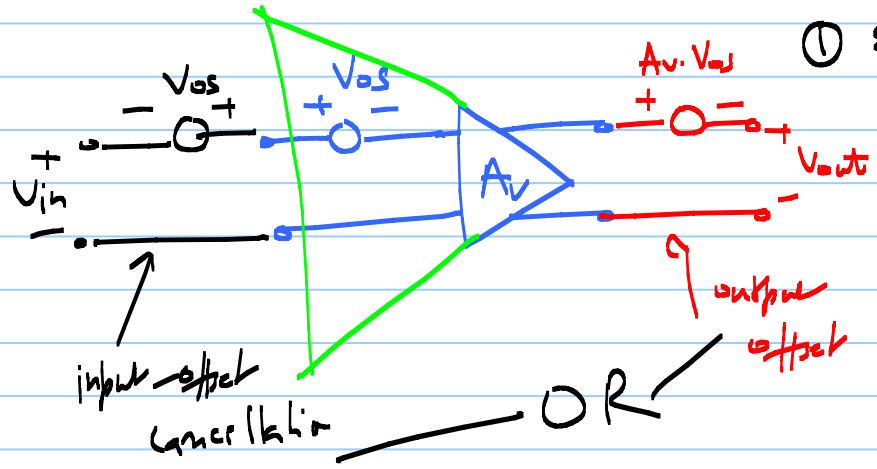
ECE 614 – Lecture 20

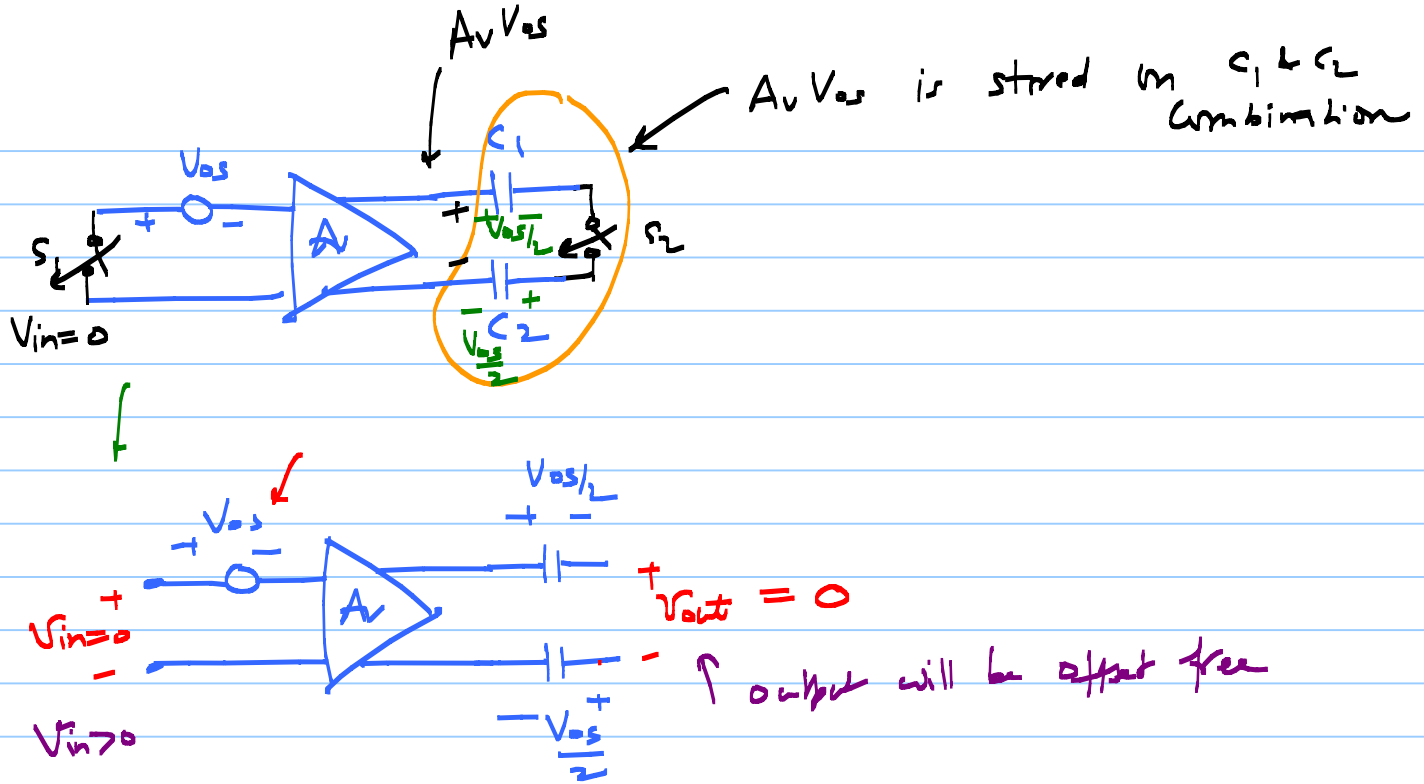
Note Title 11/13/2012

offset cancellation

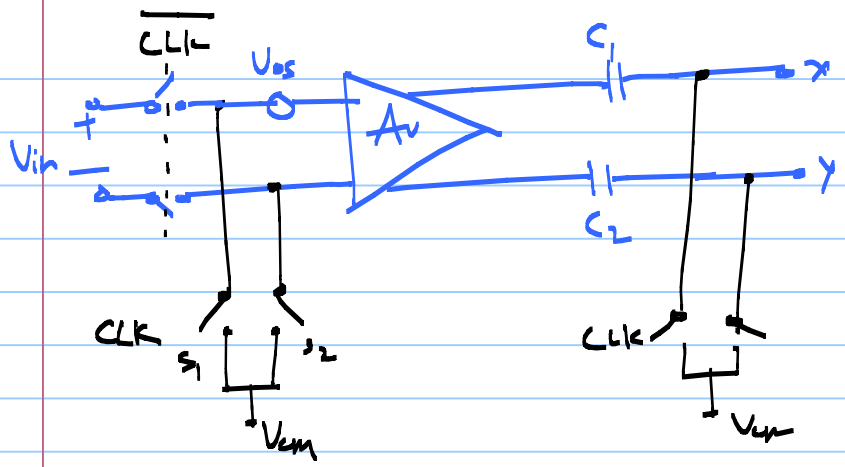


① Estimate the offset

② offset cancellation


$A_V V_{os}$
$A_V V_{os}$ is stored in C_1 & C_2 combination
V_{os}
S_1
$V_{in}=0$
A_V
C_1
$V_{os}/2$
S_2
C_2
$V_{os}/2$
V_{os}
$V_{os}/2$
$V_{in}=0$
A_V
$V_{out}=0$
$V_{in}>0$
$-V_{os}/2$
output will be offset free

output offset cancellation



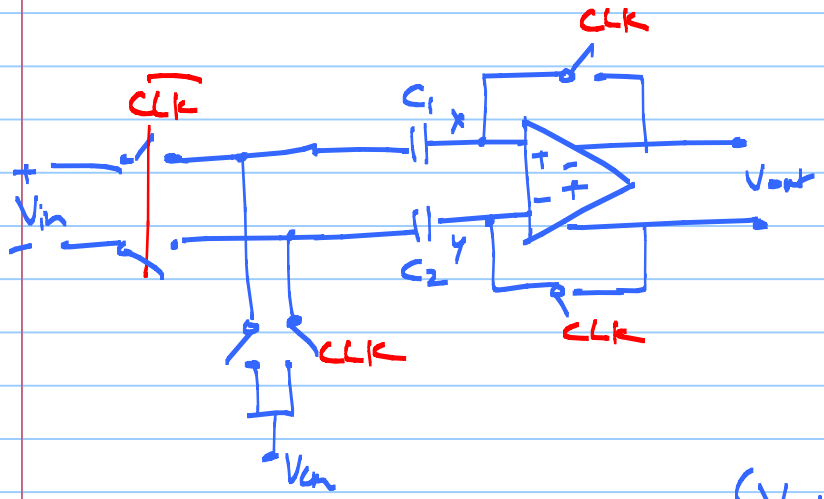
* During CLK phase

Large A_v

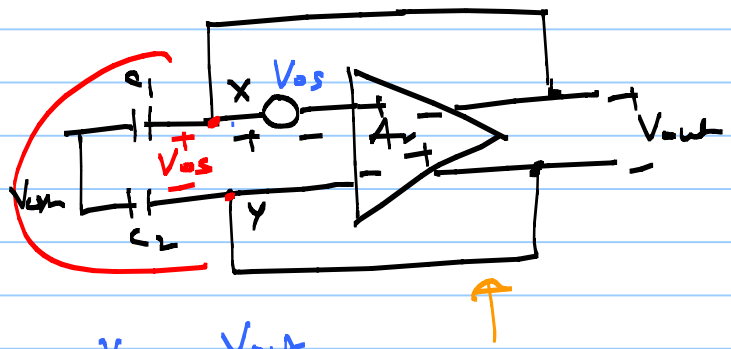
* $A_v V_{os}$ can saturate the amplifier

$A_v \lesssim 10$

Input offset Story



During CLK phase

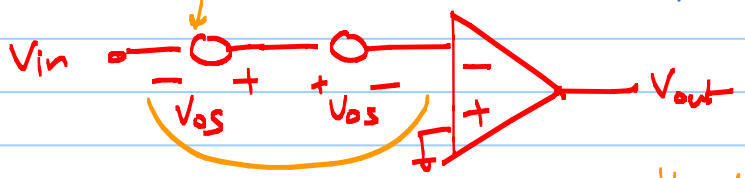


$V_{xy} = V_{out}$

$(V_{out} - V_{os})(-A_v) = V_{out}$

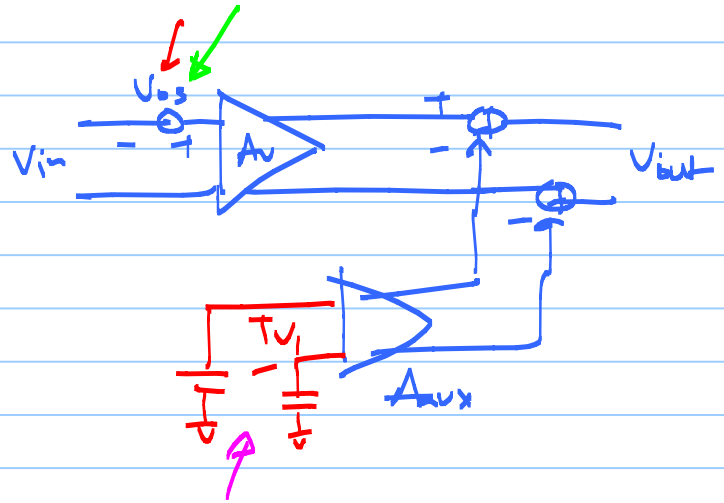
$\Rightarrow V_{out} = \frac{A_v}{1+A_v} \cdot V_{os} \simeq V_{os}$

Voltage on C_1 & C_2

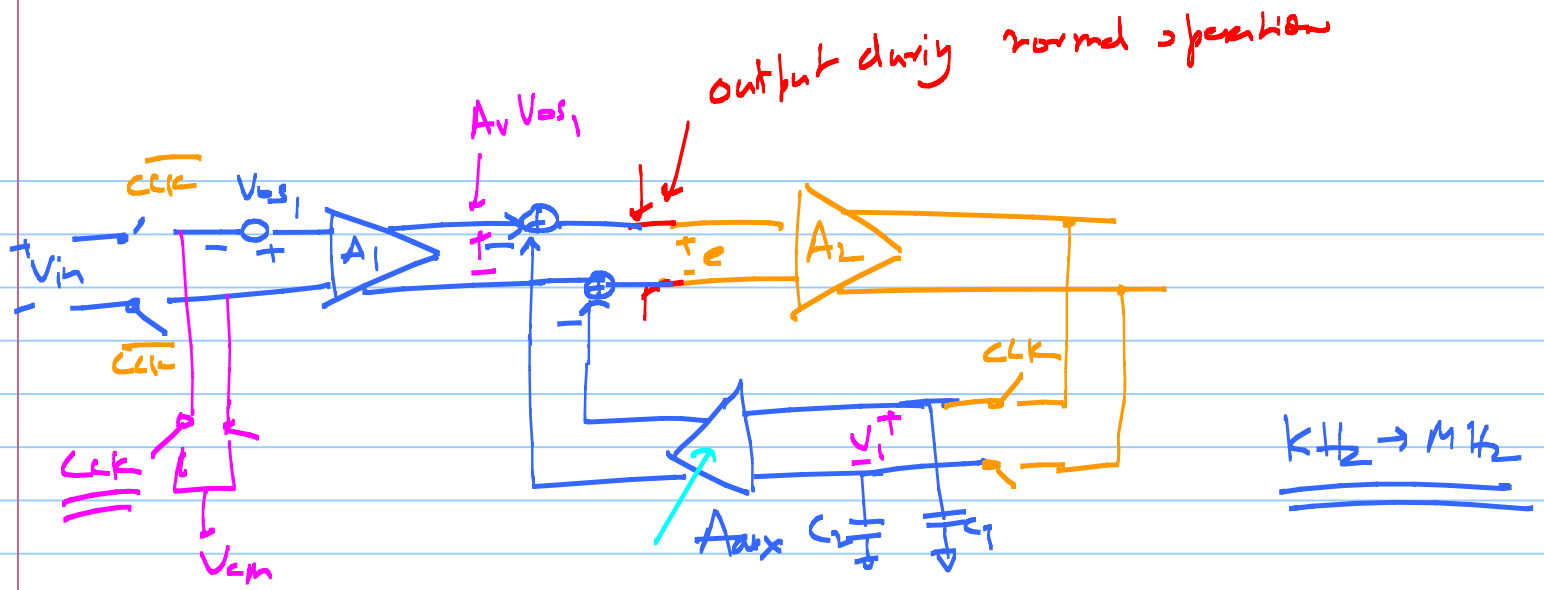


offset cancelled at the input

* Caps in the signal path
  ↳ limits the setting speed.



How to estimate V_1 ?

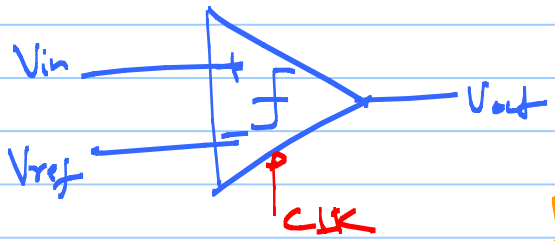


kHz → MHz

$$A_v V_{os_1} = A_{aux} V_1$$

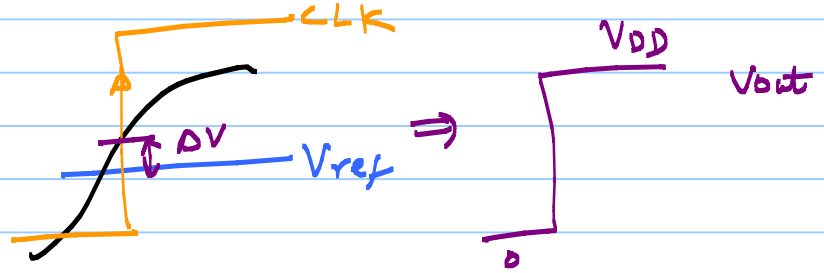
Comparators

- clocked (regenerative) ← ADC's
- asynchronous comparators ?

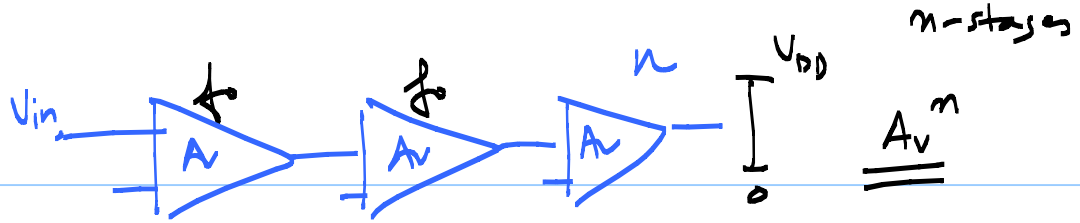


@ CLK ↑↓ $V_{in} > V_{ref} \Rightarrow V_{out} = 1$

else $\Rightarrow V_{out} = 0$

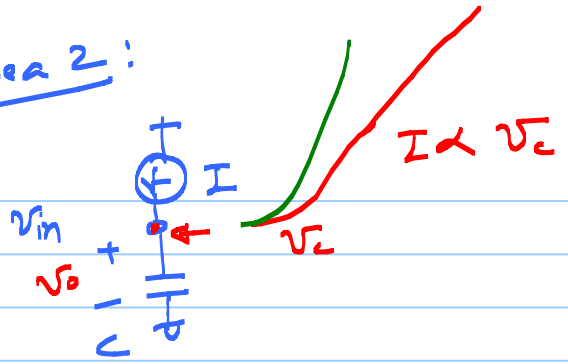


Idea 1 :



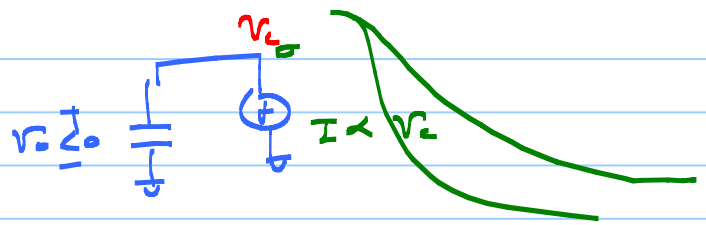
resolvable input $= \frac{V_{DD}}{A_v^n}$, $f_{3dB} = f_0\sqrt{2^{\frac{1}{N}}-1}$

Idea 2:

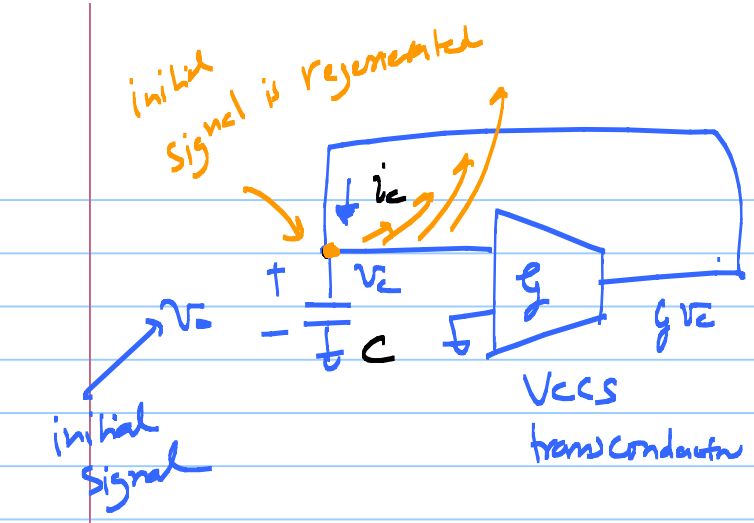


for $V_o > 0$, inject current

$V_{ref} = 0$



for $V_o < 0$, steal current



$$i_c = C\frac{dv_c}{dt} = g v_c$$

$$v_c(t) = v_o e^{+t\frac{G}{C}}$$

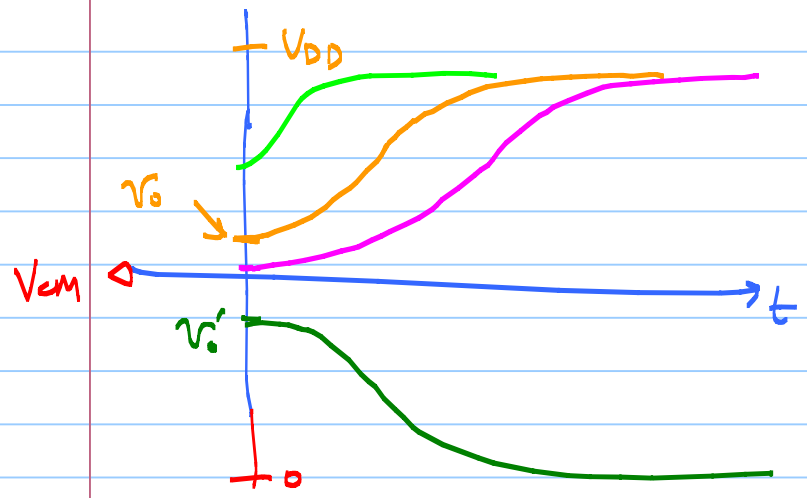
$$\tau = \frac{C}{G}$$

⇒ +ve feedback

* Regenerative Comparator

⇒ Settling speed $\propto v_o$

* metastability

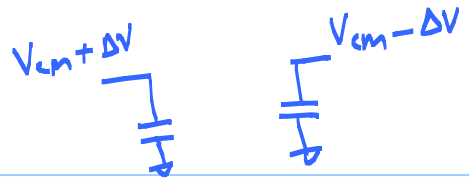


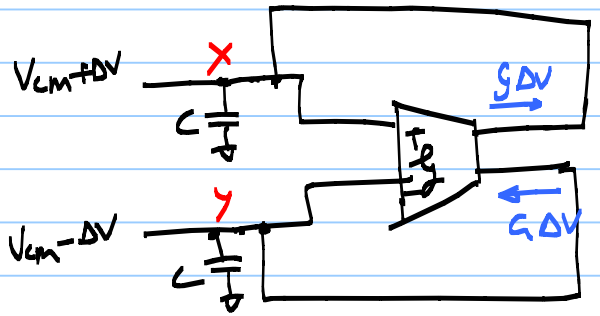
minimum resolvable input $= \dfrac{V_{DD}}{e^{T G/C}}$

To regeneration $< T_s/2$

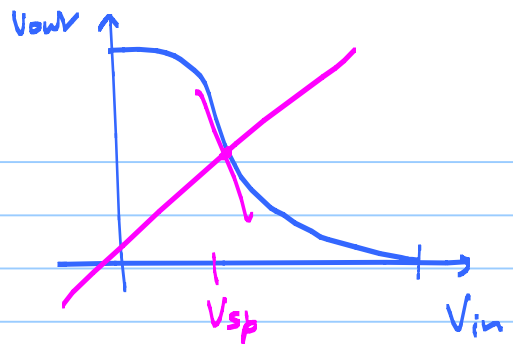
"T"

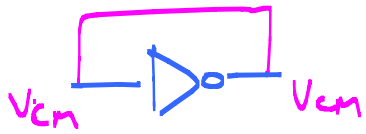
$\tau_c = \dfrac{C}{G}$ ⇐ time-constant

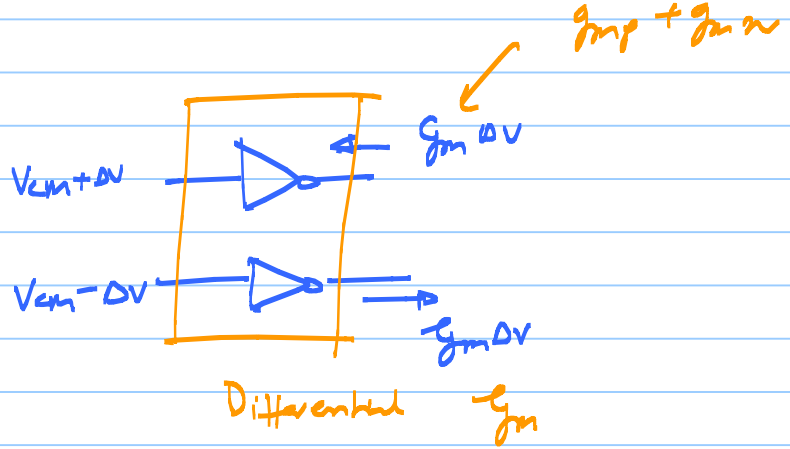


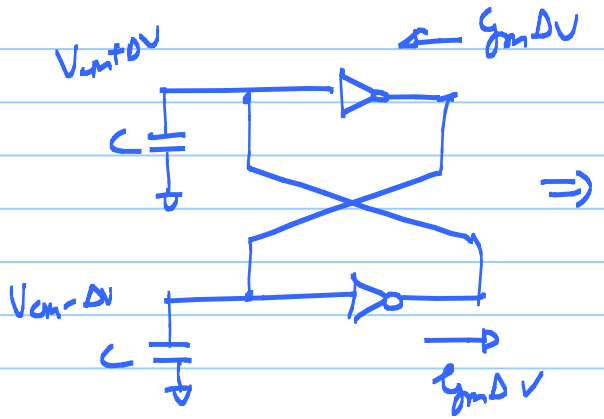


* Differential transconductor
  ↳ several possible circuit topologies

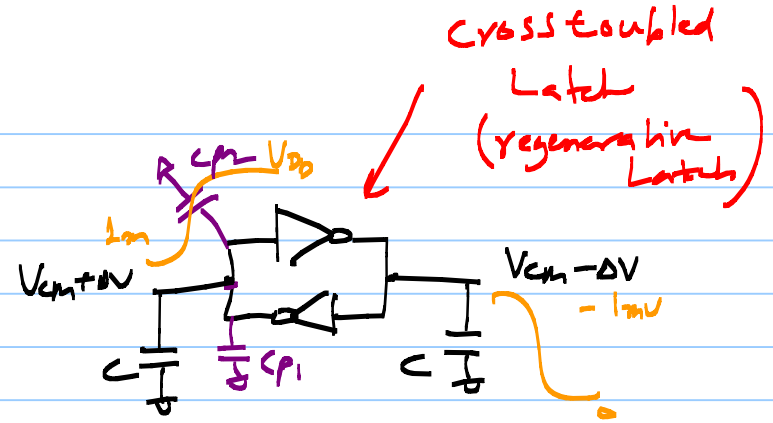

Vout
Vsp
Vin


Vcm
Vcm


gmp + gmn
Vcm+ΔV
Vcm-ΔV
gmΔV
gmΔV
Differential
gm

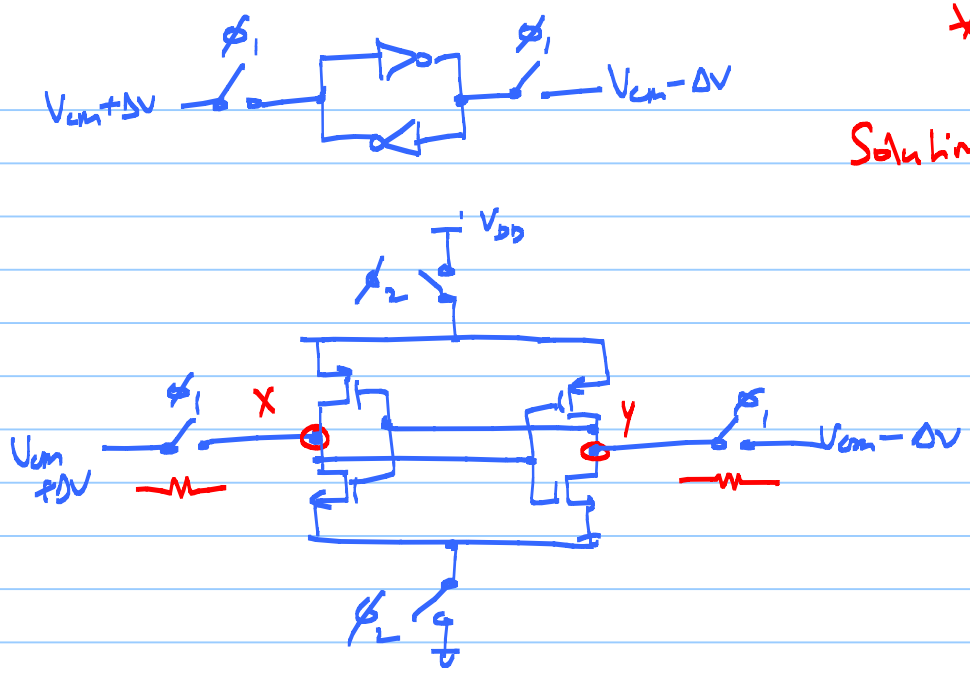


$\Rightarrow$



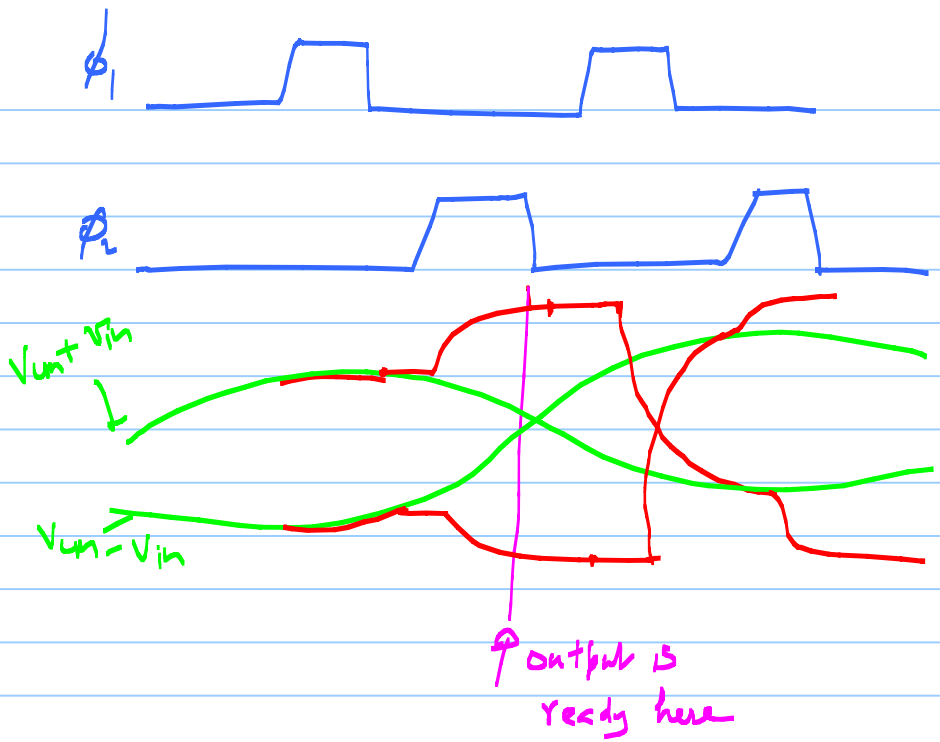
$$\tau_c = \frac{C}{G} = \frac{\cancel{C} + C_{p1} + C_{p2}}{G} \simeq \frac{2C_p}{G}$$

$G \uparrow$

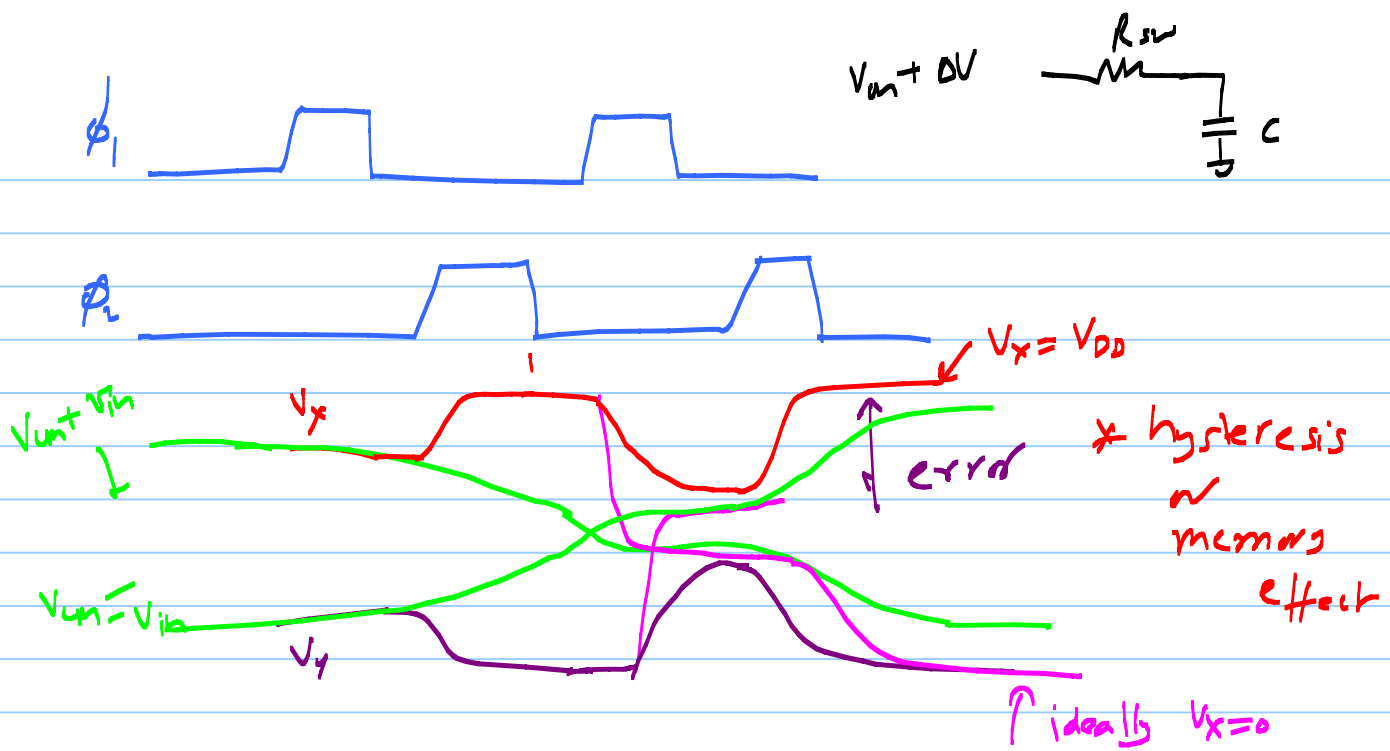


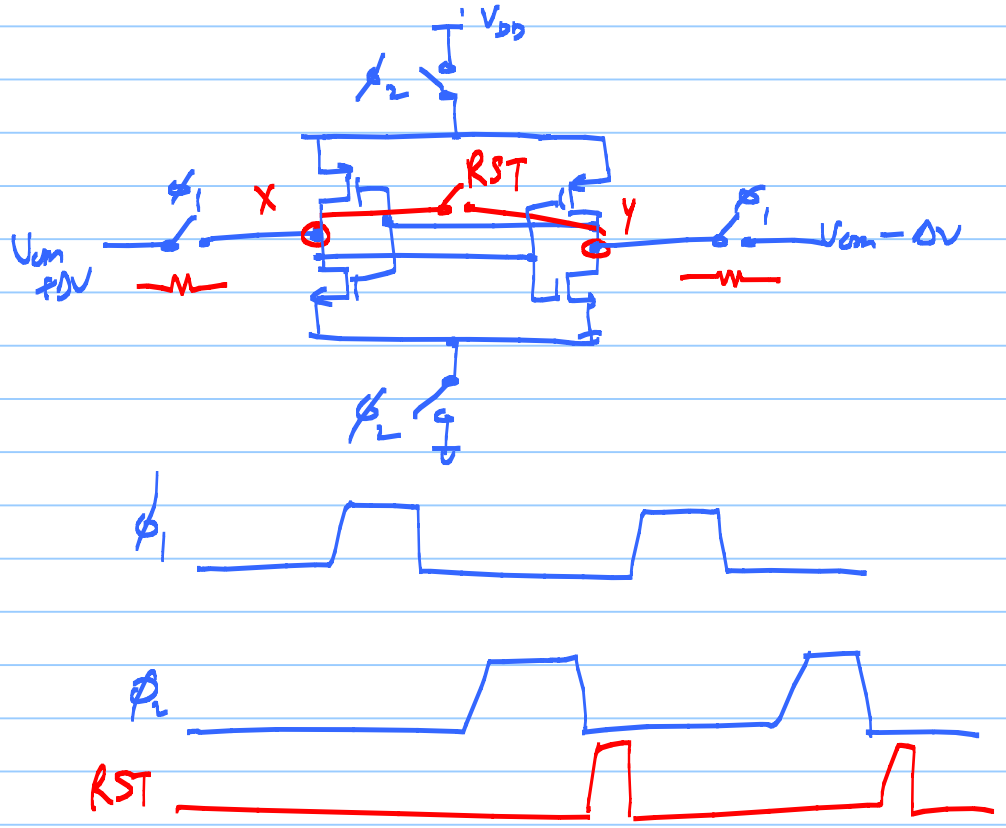
* static power issue

Solution: Disable the latch during ϕ_2



V_x , V_y


ϕ_1
ϕ_2
$V_{in}+\Delta V$
R_{sw}
C
$V_x = V_{DD}$
$V_{in}+V_{th}$
V_x
error
$V_{in}-V_{th}$
V_y
* hysteresis
or
memory
effect
ideally $V_x=0$


V_{DD}
ϕ_2
ϕ_1
X
RST
Y
ϕ_1
V_{cm} +ΔV
V_{cm} − ΔV
ϕ_2
ϕ_1
ϕ_2
RST