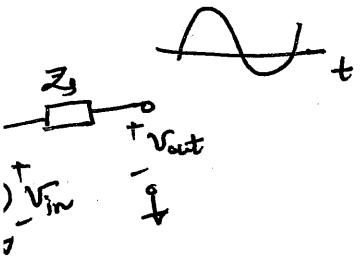
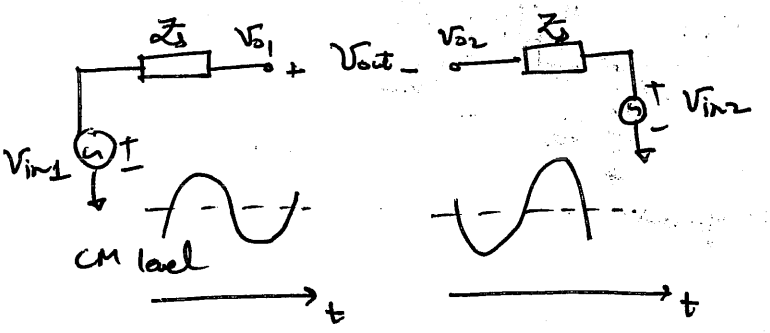
* Advantages of fully differential circuits over their single-ended counterparts

Single-ended signal



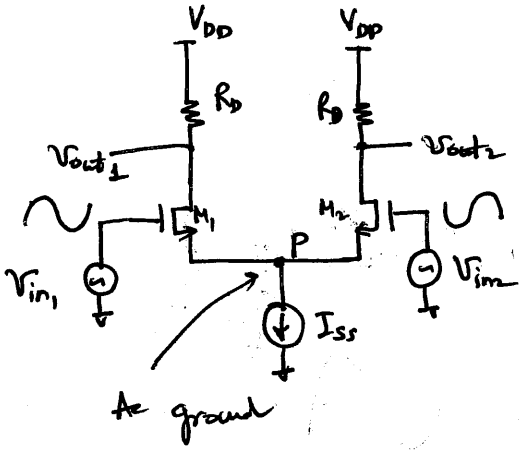




Comm-mode level : $V_{cm} = \frac{V_{o1} + V_{o2}}{2}$ ← center potential in differential signalling

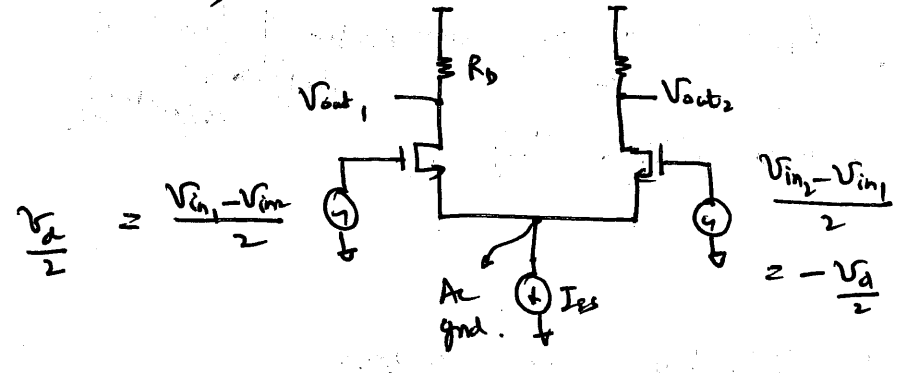
differential Signal : $V_d = (V_{o1} - V_{o2})$

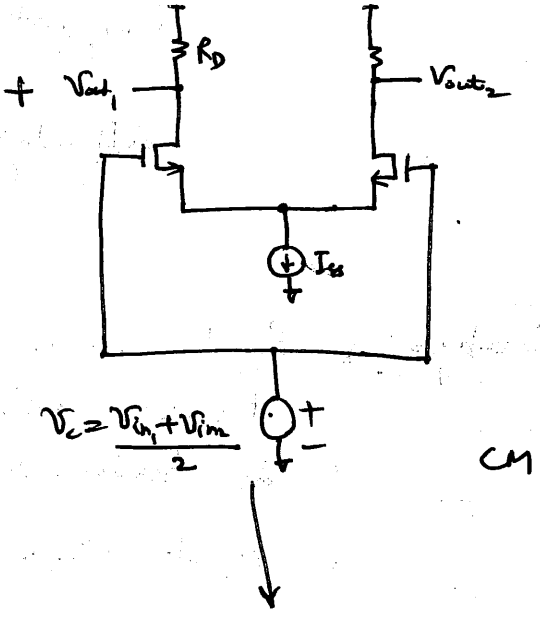
Advantages: * Rejects common mode disturbances or CM-noise
↳ supply noise or clock coupling.
* 2× signal swing
* rejects even-order distortion (harmonics)

## Half Circuit Analysis Review:

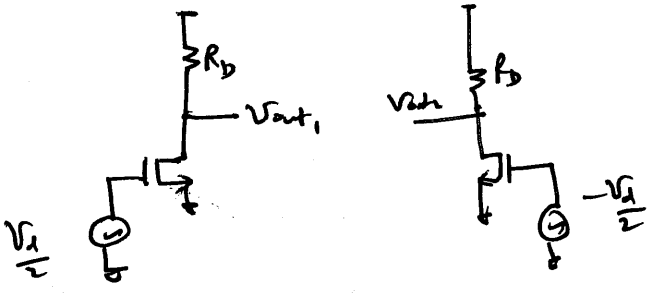



$\Rightarrow$




DM




$$v_{out_1} = -g_m(R_D \| r_{o1}) \cdot \frac{v_d}{2}$$

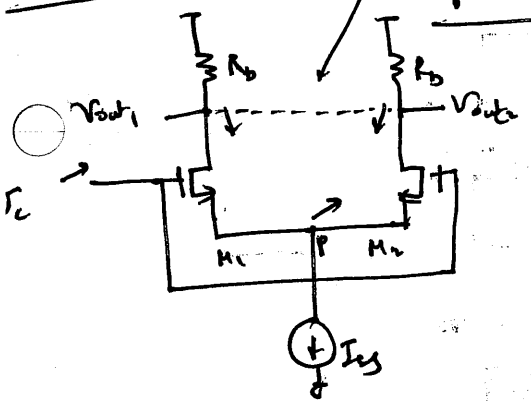
$$v_{out_2} = -g_m(R_D \| r_{o2})\left(-\frac{v_d}{2}\right)$$

$$\Rightarrow v_{out_1} - v_{out_2} = -g_m(R_D \| r_o)\, v_d$$

$$\Rightarrow A_{v,DM} = -g_m(R_D \| r_o).$$

CM equivalent circuit.

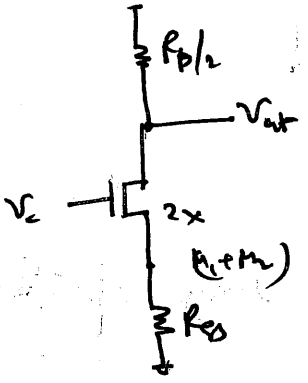
Symmetry.



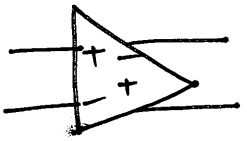

$V_{out_1} = V_{out_2}$

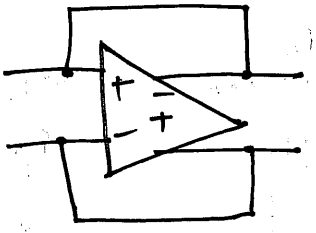
by symmetry.

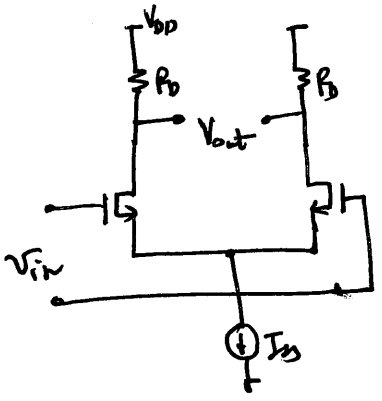
⇒ Short the nodes together

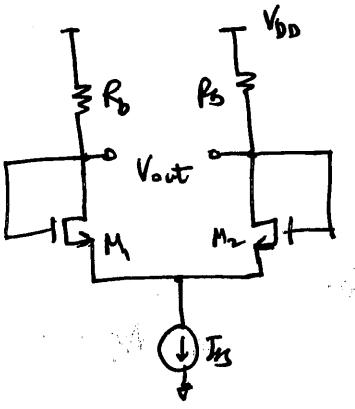



$$\Rightarrow A_{v,cm} = -\frac{R_D/2}{\frac{1}{(2g_m)} + R_{SS}}$$








In some circuits we short the input and output during operation.

↳ differential negative feedback

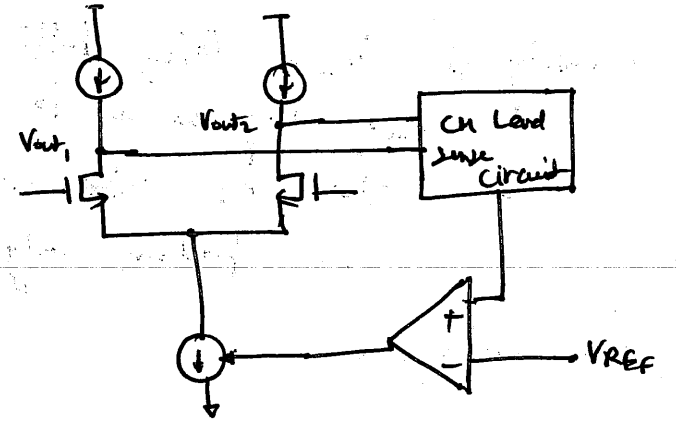
Here, input and output CM levels are well defined

$$\Rightarrow V_{DD} - \frac{I_{SS}}{2} \cdot R_D$$

Now, let's replace the load resistors by a PMOS current source. to increase the differential voltage gain

⇒ In high-gain amplifiers, the output cm-level is quite sensitive to device mismatch and cannot be stabilized by differential feedback.

⇒ A cm-feedback network is required to set the output cm level at a defined level → $V_{REF}$

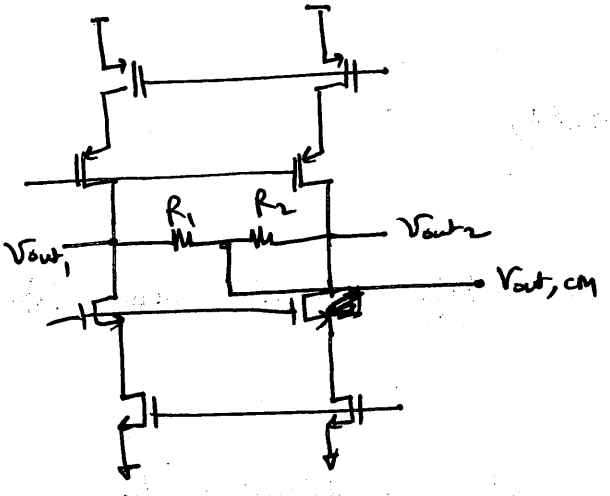



in steady state for large loop gain

$V_{out,cm} \triangleq V_{ref}$.

* How sense the output cm-level ??

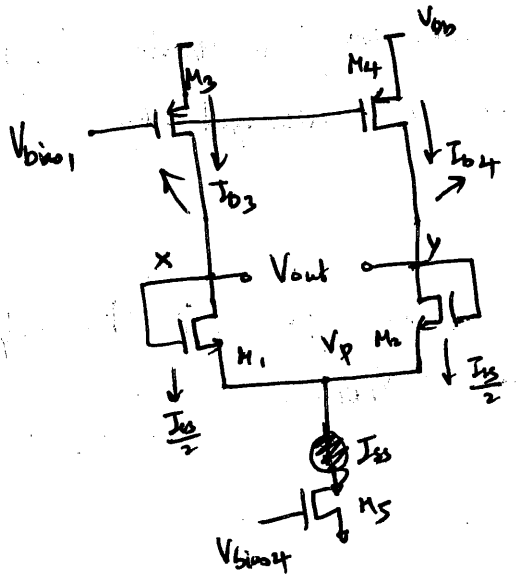
$$V_{out,cm} = \frac{(V_{out_1} + V_{out_2})}{2}$$




resistive sensing.

$$V_{out,cm} = \frac{R_1 V_{out_2} + R_2 V_{out_1}}{R_1 + R_2}$$

$$= \frac{V_{out_1} + V_{out_2}}{2} \quad \text{for } R_1 = R_2$$



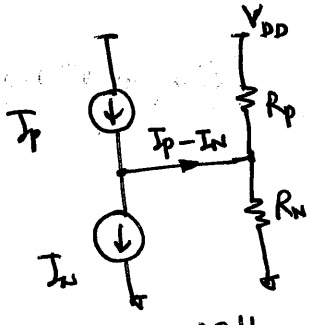

what is the CM-level at X & Y ?

* let's assume that drain currents of $M_3$ & $M_4$ are slightly higher than $\frac{I_{ss}}{2}$.

⇒ $M_3$ and $M_4$ must start to enter triode so that $I_{D3}$ & $I_{D4}$ start falling close to $I_{ss}/2$.

Conversely for $I_{D3,4} < I_{ss}/2$, both $V_x$ & $V_y$ must drop so as to drop so that $M_5$ enters triode and thus producing only $2I_{D3,4}$.

fundamental difficulty in high-gain amplifiers.




Two current sources fighting.

Voltage change ⇒ $(I_p - I_N)(R_p \| R_N)$

drives the p-type or n-type current source into triode region.

⇒ the output CM-level can't be determined by "visual inspection" ⇒ poorly defined.

⇒ differential feedback cannot define CM-level.

Issues:

⇒ $R_1, R_2 \gg$ Rout of the opamp to avoid lowering the open-loop gain

but large $R_1$ & $R_2$ ⇒ large area
large parasitic cap.
RC poles