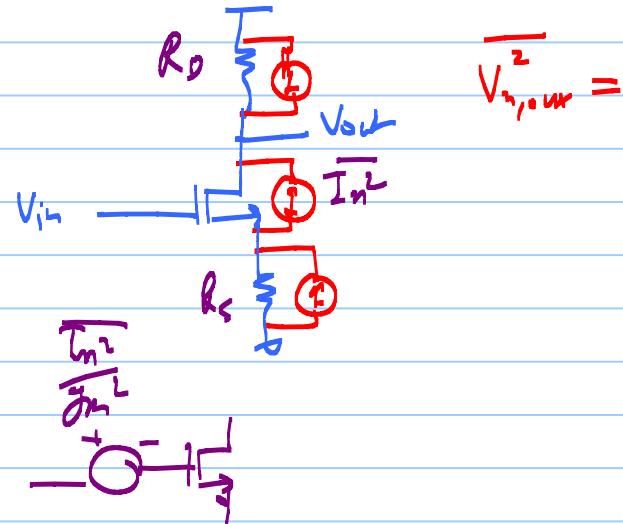


ECE 614 - Lecture 15

Note Title

10/23/2012



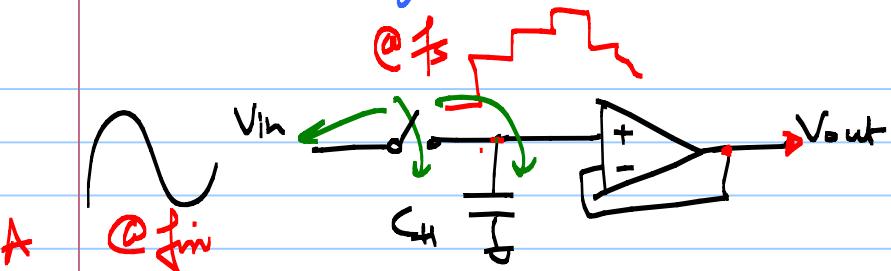
$$\bar{v}_{n1, out} =$$

$$V_n = V_{n1} + V_{n2}$$

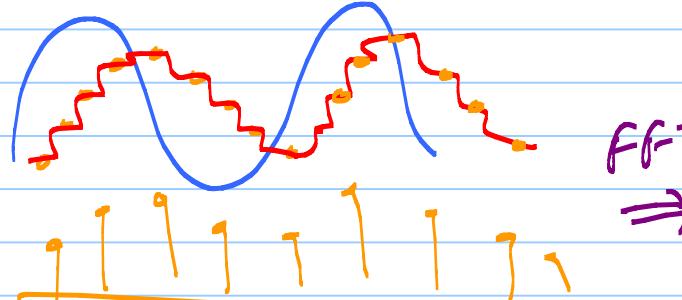
$$\begin{aligned}\bar{v}_n^2 &= (V_{n1} + V_{n2})^2 \\ &= \bar{v}_{n1}^2 + \bar{v}_{n2}^2 + 2 E(V_n, V_n)\end{aligned}$$

uncorrel-ha

Unity-gain Sampler (S/H)

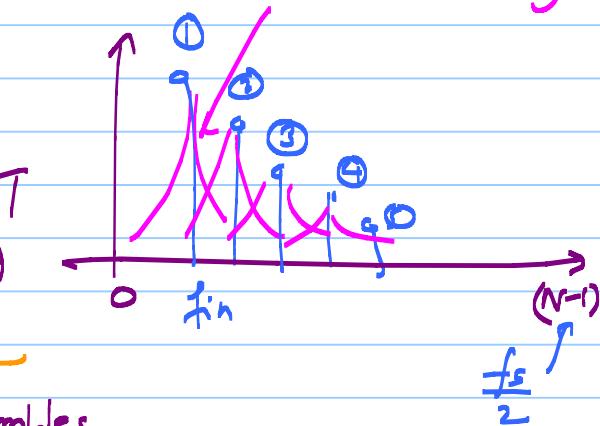


input dependent CI



FFT

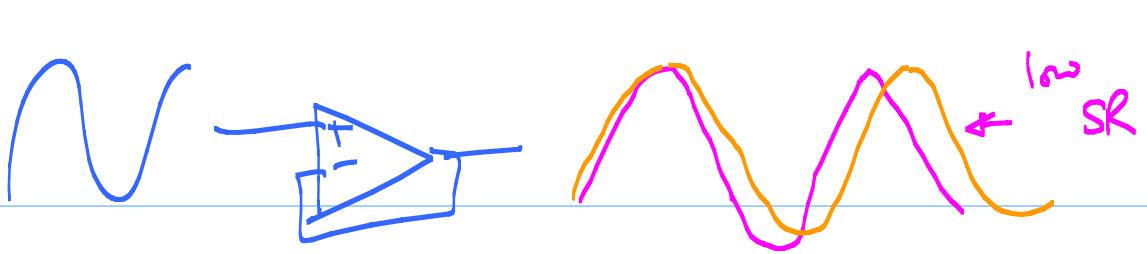
FFT leakage



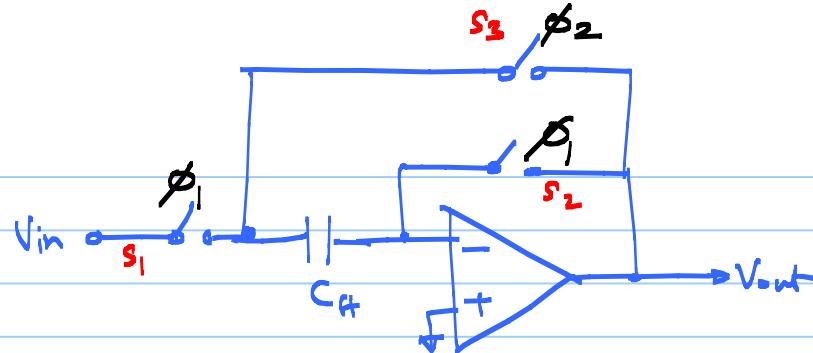
$$\frac{f_{\text{in}}}{f_s} = \frac{k}{2} = \frac{1}{128} \quad \cancel{\frac{1001}{128}} \quad "N" \text{ samples}$$

\neq Coherent Sampling \nearrow mutually prime $= \frac{32}{128} = \frac{1}{4}$

"Dynamic Characterization"

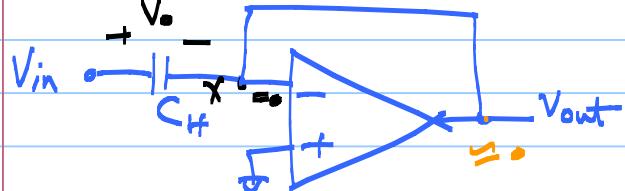


distr him due to slew rate



ϕ_1 Sampling mode

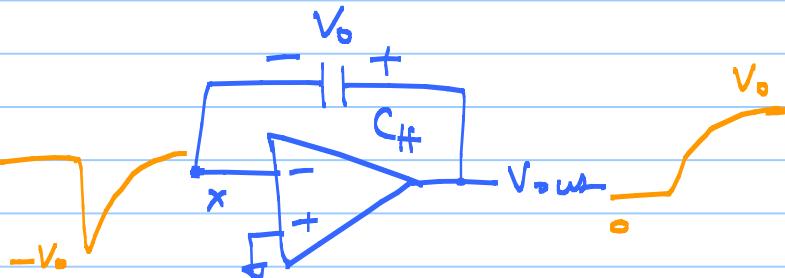
ϕ_2 Amplification/Hold mode



$$V_{out} = V_n = 0$$

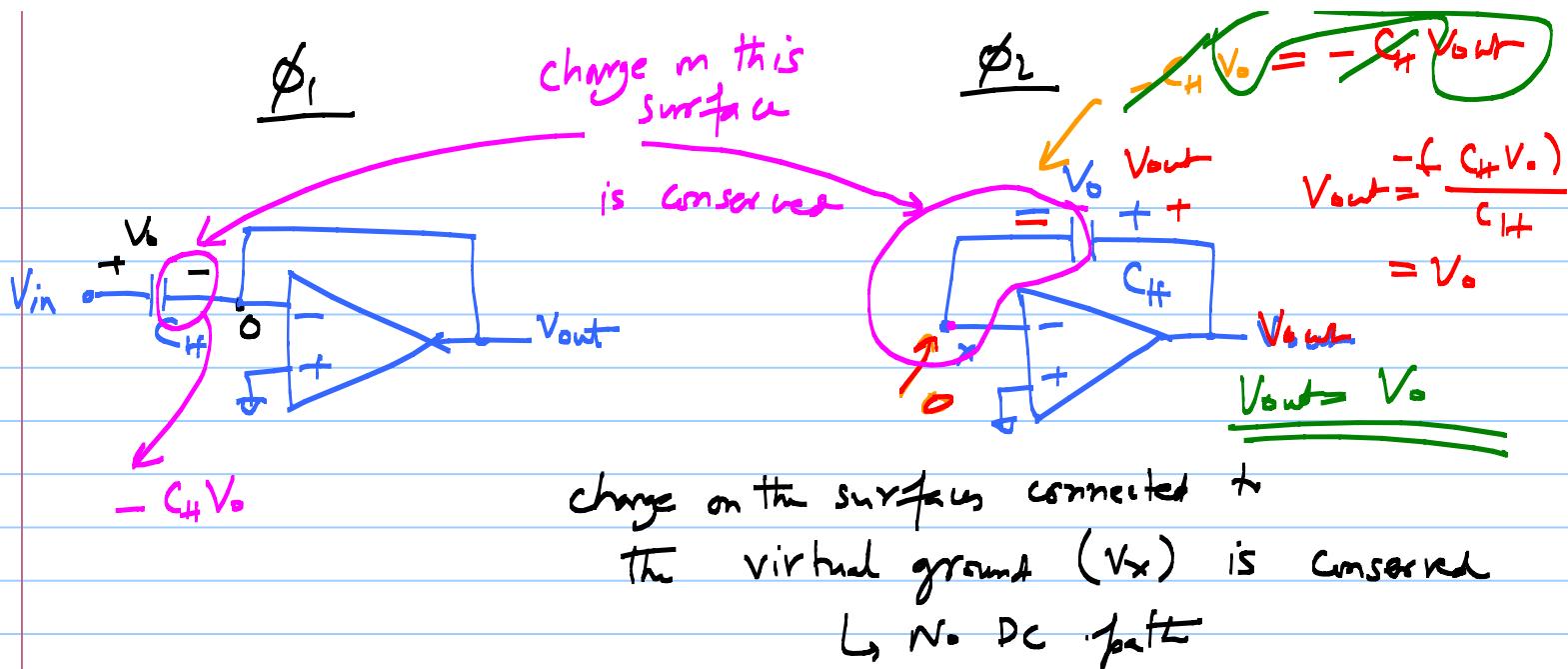
Voltage across C_H tracks V_{in}

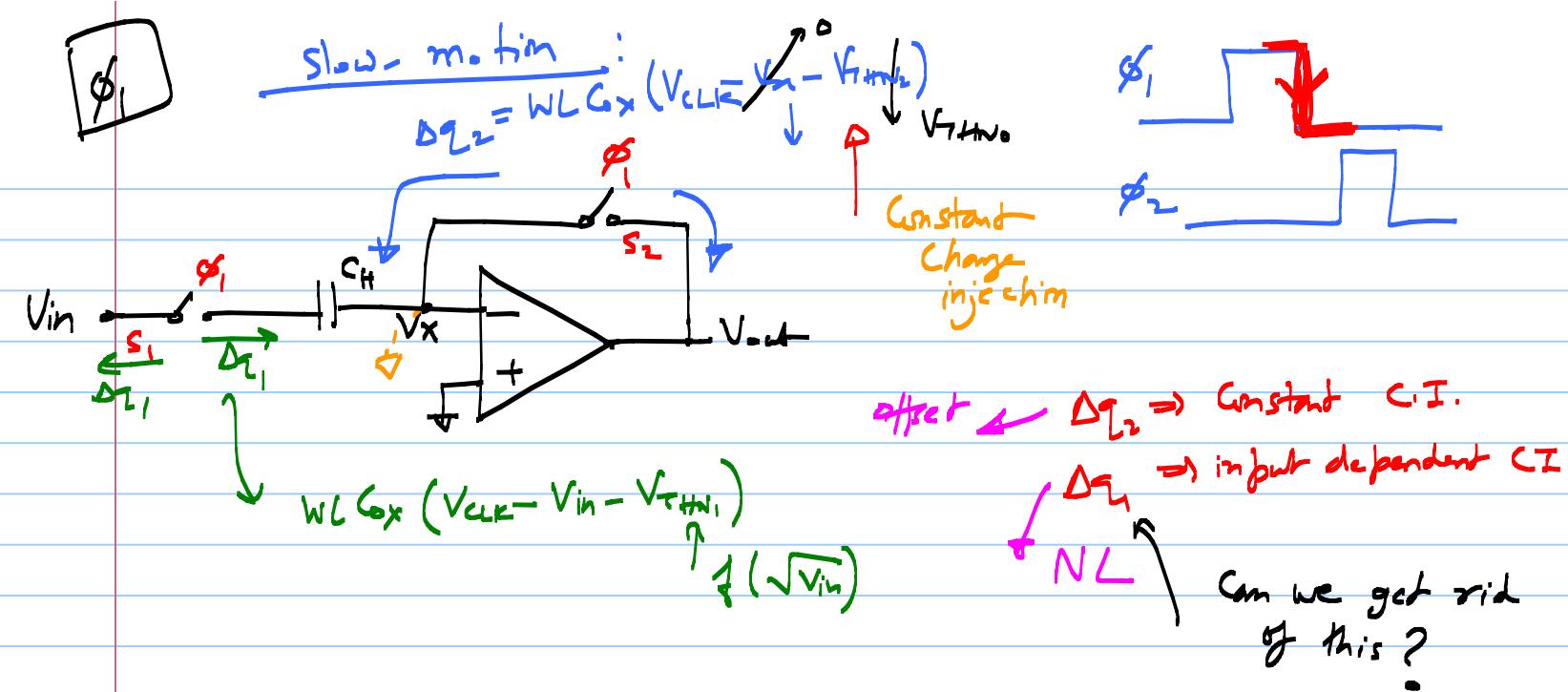
@ $t = t_0$, $\phi_1 \downarrow \rightarrow V_{in} = V_o$ is stored in C_H



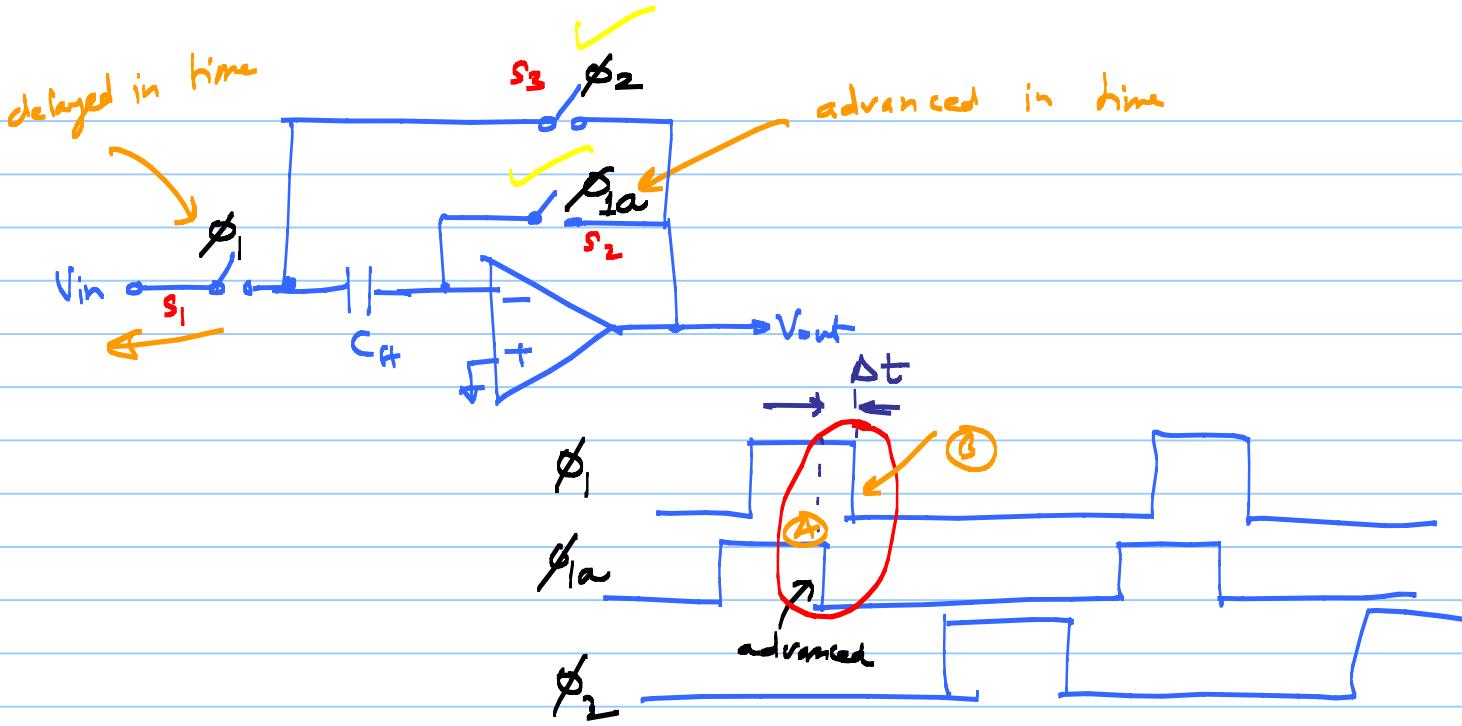
$V_{in} \Rightarrow$ V_{out} rises to $\underline{-V_o}$

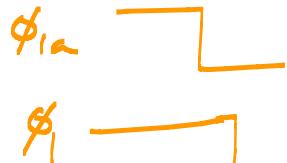
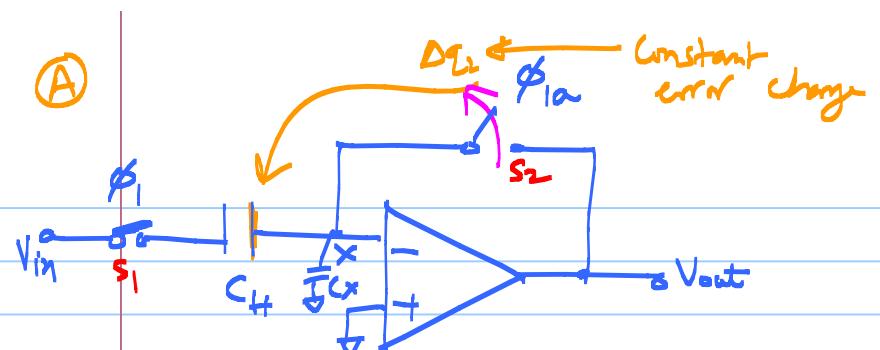
* This value is frozen and presented to Subsequent stages





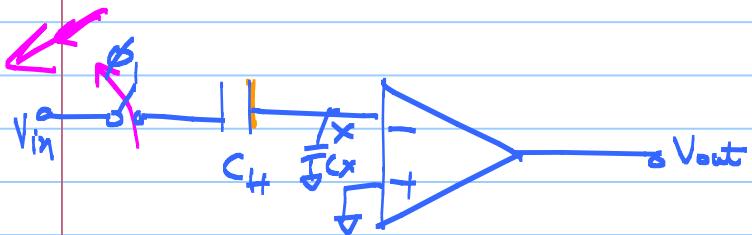
Trick : Delayed sampling clock

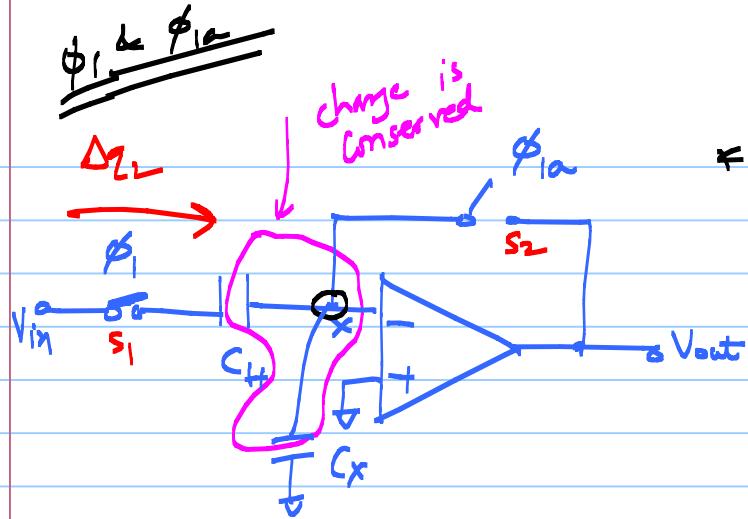




(B) charge sucked into the source

* avoids input-dependent charge injection

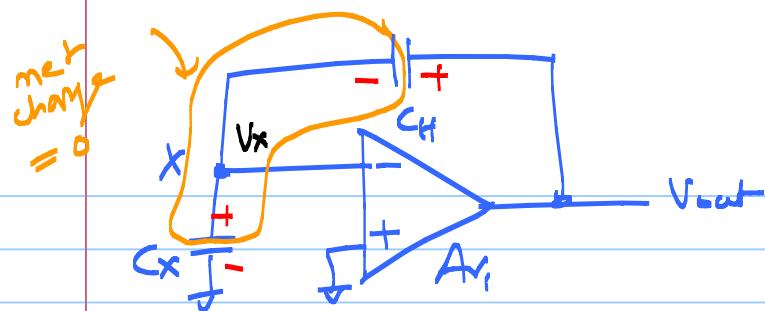




- * After S_2 is off.
- * Before S_1 turns off,
total charge on right plate of C_H
+ top plate of $C_x = 0$

Example $V_{in}=0$





Total charge @ node $X = 0$

$$\Rightarrow C_x V_x - (V_{out} - V_x) C_H = 0 \longrightarrow \textcircled{1}$$

$$\& V_x = -\frac{V_{out}}{A_{v_i}} \longrightarrow \textcircled{2}$$

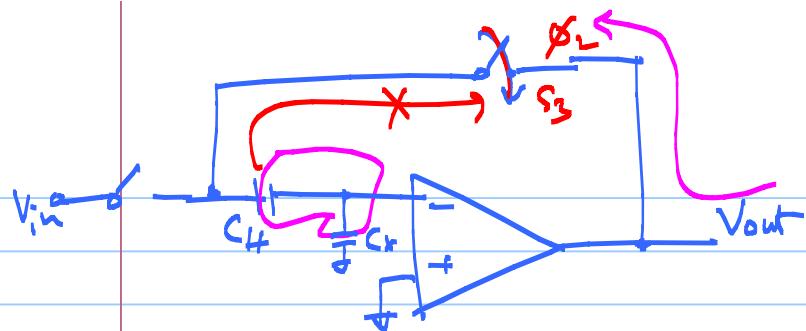
$$\Rightarrow \textcircled{1} \Delta \textcircled{2} =$$

$$- (C_x + C_H) \frac{V_{out}}{A_{v_i}} - V_{out} C_H = 0$$

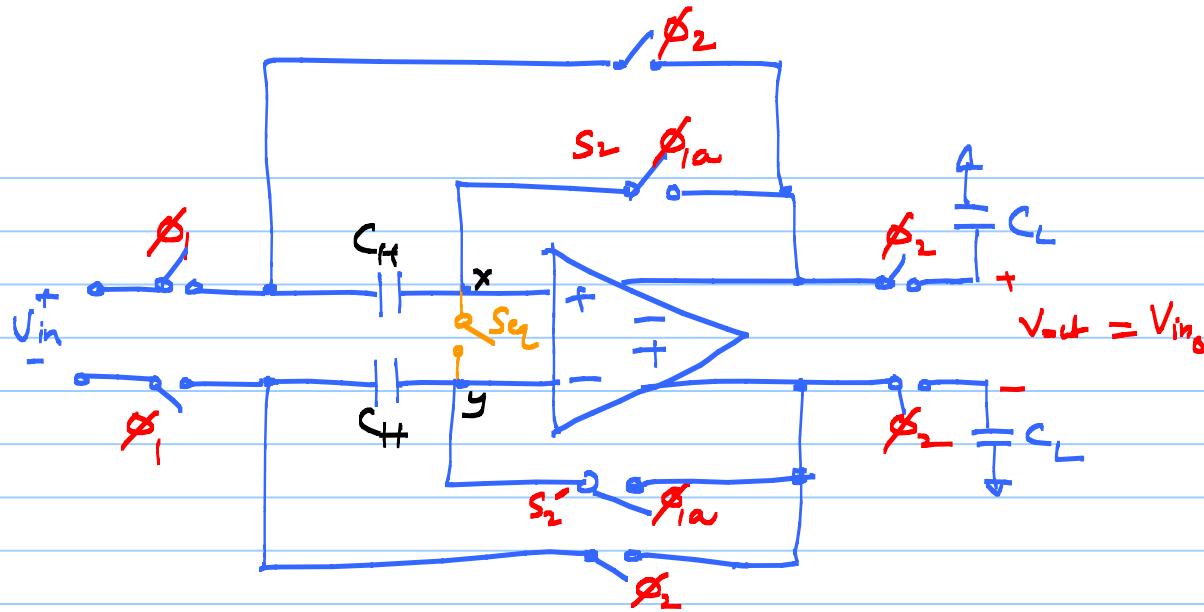
$$V_{out} (?) = 0$$

\Rightarrow charge injection Δq_2 (by S_1)
introduces no error as
 $"S_2"$ is turned off first.

$$\boxed{V_{out} = V_o} \leftarrow \text{indep. of } \Delta q_2, C_x, A_{v_i}$$

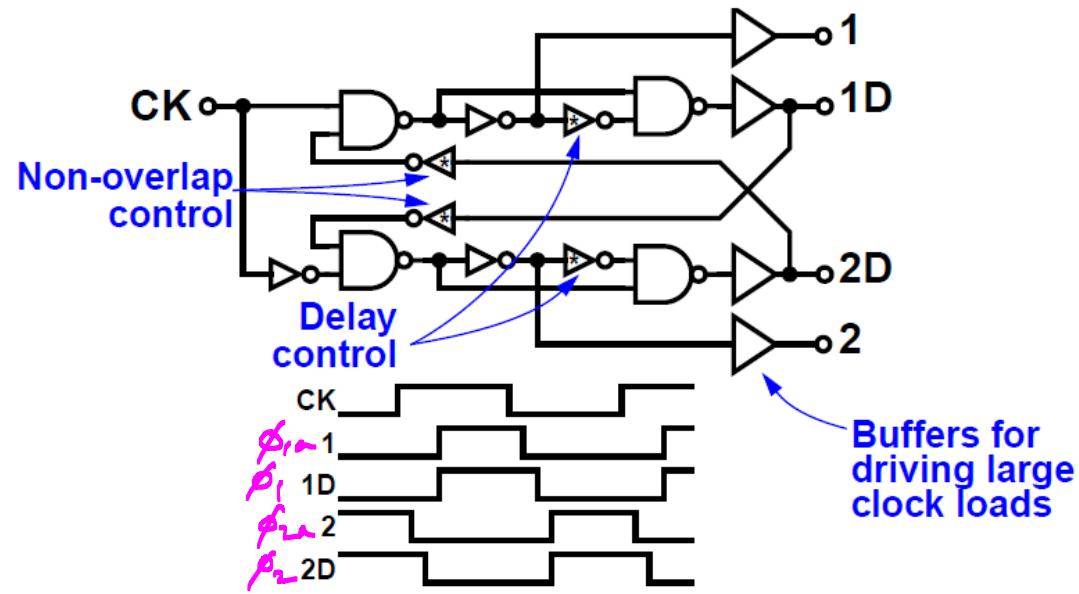


when S_2 goes high
 the inversion layer charge for S_3
 is completely supplied by $\underline{\underline{V_{out}}}$
 (opamp)



- * NL due to the input-dependent charge injection is mitigated
- * any fixed charge injected at x & y is a CM-disturbance
- * in reality $S_2 \& S_2'$ exhibit finite charge injection mismatch
 - ↳ add another switch S_{eq}
 - ↳ turns off slightly after $S_2 \& S_2'$
 - ↳ bulk before $S_1 \& S_1'$

Professional Clock Generator



- To maximize the time available for settling, make the early and late phases start at the same time