Project 2

ECE 614 – Advanced Analog IC Design (Fall 2012)

Due on Thursday, Dec 14, 2012.

Design of a 10-bit Pipelined ADC: Design a pipelined ADC for the following design specifications:

Table 1: Pipelined ADC specifications.

Parameter	**Specified Value**
Technology	IBM 130-nm CMOS
Supply voltage, V_{DD}	1.2 V
ADC sampling rate (f_s)	$50\,MS/s$
Target ADC resolution (N_{eff})	10 bits
Target SNDR	$\geq 50\,dB$
Target SFDR	$\geq 60\,dB$
Power consumption	<50 mW

- Select a suitable architecture for your pipelined ADC (number of stages, number of bits per stage, switched-capacitor topologies, capacitor sizing and any other design techniques or optimization used) and justify your choices.
- At least the first MDAC should be a transistor-level design and you may use behavioral models for the rest. Include opamp design considerations ($A_{OL,DC}$, f_{un}, PM, CMFB, $SR_{+/-}$, offset, input-referred noise, etc.) for the first stage. List the opamp specifications required from the rest of the MDAC stages. Include noise analysis and discussion on sampling capacitors selection. You can use any method of choice for digital backend implementation.
- Select appropriate analysis methods and test-benches characterization of your design. Use the references pipelined ADCs on the course web page.
- Clearly show your neatly drawn schematics and present your calculations and result plots with proper labels and annotation. Clear presentation of your design choices, analysis and simulation-based verification of design perfromance will significantly determine the project grade.