Project 1

ECE 614 – Advanced Analog IC Design (Fall 2012)

Due on Thursday, Nov 15, 2012.

Design of a precision gain amplifier: A pipelined ADC stage (an MDAC) incorporates a discrete-time amplifier with precise gain of 2^M, where $M \geq 1$ is the number of bits per stage. In this project, a precision switched-capacitor gain stage of **2** will be designed for the first stage of a 50 MSPS, 10-bit pipelined ADC. The target specifications for the precision amplifier are as follows:

Table 1: Precision gain stage design specifications.

Parameter	**Specified Value**
Technology	IBM 130n CMOS
Supply voltage, V_{DD}	1.2 V
Target ADC sampling rate (f_s)	$50\,MHz$
Gain	2
Target ADC resolution (N_{eff})	10 bits
Target ADC SNDR	$\geq 6.02N_{eff} + 1.76 = 62\,dB$
Power consumption	Minimum

Use the provided 130n CMOS process with $V_{DD} = 1.2\,V$ for all the problems. Clearly show your neatly drawn schematics and present your calculations and result plots with proper labels and annotation. Include noise analysis, discussion on sampling capacitor selection and opamp design considerations ($A_{OL,DC}$, f_{un}, PM, CMFB, $SR_{+/-}$, offset, input-referred noise, etc.) for the circuit application. Your amplifier should **ensure the SNDR and linearity required for 10-bit accuracy**. Clear analysis and simulation-based verification of your design choices will significantly determine the grade.