Homework 4

ECE 614 – CMOS Analog IC Design

October 23, 2012

Note: Use the provided 130n CMOS process with $V_{DD} = 1.2\,V$ for all the problems.

Problem 1: Develop a macro-model for single-pole fully-differential opamp. The macro-model should include configurable parameters including - open-loop DC gain (A_v), unity-gain frequency (f_{un}), input-referred offset, slew-rate (SR), input parasitic capacitance (C_{in}) etc.

Problem 2: Simulate the operation of a fully differential bottom-plate sampling circuit operating at 50 MHz clock rate:

1. Use transistor-level switches and the opamp macro-model. Try two topologies with:
   (a) Two-clock phases (ϕ_1 and ϕ_2) only.
   (b) Clock phases (ϕ_1, ϕ_{1a} and ϕ_2), where ϕ_{1a} is the *advanced* sampling phase for charge-injection noise mitigation.
2. Using and input sine wave of $1\,V_{pp}$ and $f_{in} = 1\,MHz$, compare sampled outputs from the two circuits.
3. Compare harmonic distortion from the two circuits. Use FFT with a test-bench using coherent sampling.
4. Simulate and comment on the effect of the opamp A_v, f_{un}, C_{in} on the settling accuracy of the circuit. What is the impact of opamp slewing on settling accuracy and distortion?
5. Estimate the rms thermal noise in the output.

Problem 3: Using the opamp macro-model and transistor-level switches, implement:

1. Inverting and non-inverting amplifiers of gain 4, operating at 50 MHz frequencies. Verify operation using transient as well as PAC analysis.
2. Determine the opamp specifications for 0.1% settling accuracy for these amplifiers. Is charge-injection an issue in these circuits?
3. Estimate the rms thermal noise in the output for these circuits.

Problem 4: Using the opamp macro-model and transistor-level switches, design a parasitic-insensitive switched-capacitor integrator operating at 50 MHz and with $\frac{C_1}{C_2} = 2$.

1. Verify operation using transient as well as PAC analysis.
2. Derive the ideal transfer function for the integrator $I(z) = \frac{V_{out}(z)}{V_{in}(z)}$ and show the pole-zero plot.
3. What is the impact of finite opamp gain and f_{un}on the integrator's frequency response?

Problem 5: Design a non-overlapping clock generator required to generate all the clock phases for S/H circuit in problem 2. The clock generator should provide consistent performance in all process corners.