Homework 3

ECE 614 – CMOS Analog IC Design

Due on Tuesday, Oct 23, 2012

Note: Use the provided 130n CMOS process with $V_{DD} = 1.2\,V$ for all the problems. Clearly show your neatly drawn schematics and present your calculations and result plots with proper labels and annotation.

Problem 1: Noise Simulations:

1. Simulate input referred noise of a resistive voltage divider formed using two 1K resistors and compare the results with your hand-calculations.
2. Make one of the resistors noiseless in your simulation and repeat part (1).
3. Load the output of the divider in part (1) with a 1pF capacitor and find the output rms noise voltage ($V_{n,out,rms} = \sqrt{\int \overline{V_{n,out}^2}(f) \cdot df}$). Compare with hand-calculations.
4. Size a CMOS switch to charge and discharge a 1pF capacitor using a 10 MHz clock. Estimate and simulate (try PSS with PNOISE) the output rms noise voltage ($V_{n,out,rms}$) stored in the capacitor at the end of tracking phase (i.e. when the clock goes low). Will flicker ($\frac{1}{f}$) noise have any effect on the sampled noise?

Problem 2: For the opamp designed in HW1:

(a) For the bias current and sizing of the input diff-pair (NMOS) transistors used, plot the input referred noise PSD ($\overline{V_n^2}$). What is the corner frequency for the flicker noise? For a PMOS sized for the same g_m as the NMOS, plot and compare the noise PSD.

(b) Simulate and plot the output noise PSD ($\overline{V_{n,out}^2}$) and the input referred noise PSD ($\overline{V_{n,in}^2}$) with $\frac{V^2}{Hz}$ and $\frac{V}{\sqrt{Hz}}$ units. Calculate the RMS output noise voltage ($V_{n,out,rms} = \sqrt{\int \overline{V_{n,out}^2}(f) \cdot df}$) in nV for the closed-loop amplifier.

(c) Which transistor pairs are the major noise contributors? What changes would you make in your design to reduce input referred noise voltage by 25%?

(d) Run a noise report, excluding the bias resistors. Plot a pie chart of noise contribution from each of the *transistor pairs* and compare with part (c). Use a frequency setting of >10 MHz in the tool to avoid flicker noise.

Problem 3: Calculate the input-referred thermal noise voltage ($\overline{V_{n,in}^2}$) for each of the circuit below. Assume $\lambda = \gamma_{body-effect} = 0$ for (a) and (b). How would you minimize the value of ($\overline{V_{n,in}^2}$) for each of the circuits?

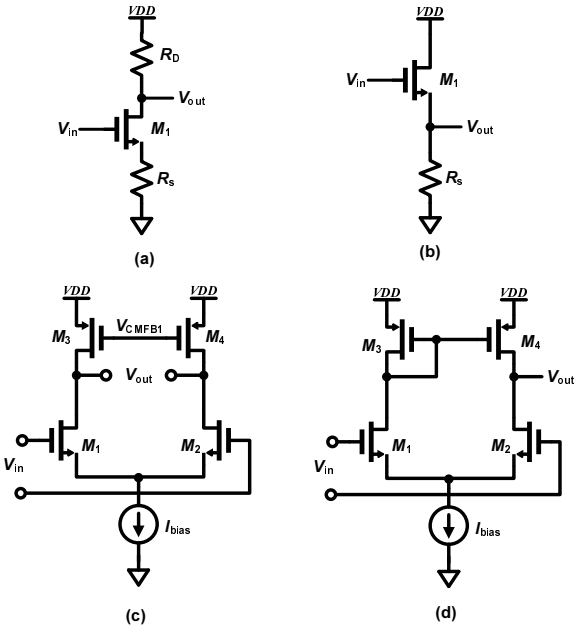

Figure 1: Circuits for problem 3.

Problem 4: Calculate the input-referred thermal noise voltage ($\overline{V_{n,in}^2}$) and current ($\overline{I_{n,in}^2}$) for each of the circuit below. Assume $\lambda = \gamma_{body-effect} = 0$. How would you minimize the value of ($\overline{I_{n,in}^2}$) for each of the circuits?

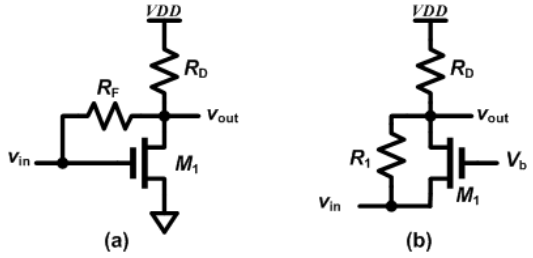

Figure 2: Circuits for problem 4.

Following extra problems are meant for your exam practice. No need to turn them in.

Extra Problem 1: Determine the small-signal voltage gains, input-referred thermal and $\frac{1}{f}$ noise voltages of the circuits shown below and compare the results. Assume that the circuits draw equal supply currents.

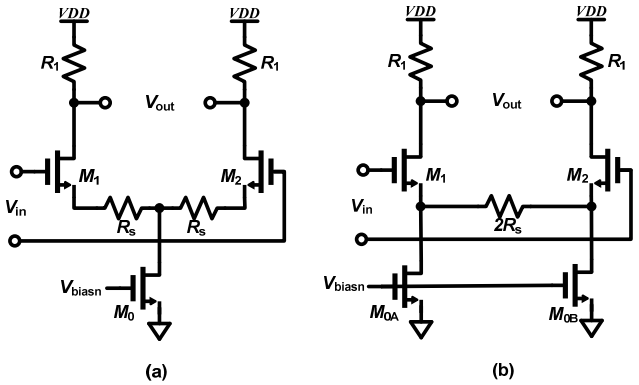

Figure 3: Circuits for problem 5.

Extra Problem 2: Draw PMOS versions of the fully-differential Telescopic and Folded-cascode opamps discussed in class. Estimate their input-referred thermal and $\frac{1}{f}$ noise voltages using the simplifying techniques discussed in the lecture.