Revision History

Ver. #	Rev. Date	Rev. By	Comment
0.0	9/29/2012	Kehan Zhu	Initial draft
1.0	9/30/2012	Kehan Zhu	Continue SC-CMFB analysis; PAC analysis
2.0	10/1/2012	Kehan Zhu	Continue PAC; start PSTB and problem2
3.0	10/2/2012	Kehan Zhu	Add comments and make a conclusion

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1 Two-stage Fully-Differential Opamp with SC-CMFB

1.1 Spec. and Requirement

- ✓ **Process**: IBM 130nm CMOS, 1.2V nominal power supply voltage.
- ✓ **Specification**: Open loop gain and unity-gain frequency are > 74dB and 3~5 times sampling clock frequency ($f_s = 5MHz$), respectively. $C_L = 1pF$.
- ✓ **Requirements**: Based on the opamp designed in HW1, discuss the impact of sizing of capacitors in SC-CMFB on loop stability and transient settling. Use PSS and PSTB for sampled circuit stability analysis.
- ✓ **Simulation list**:

  1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
  2. Common-mode loop(s) gain-magnitude and phase. Indicate the phase margin.
  3. Transient response of the unity-gain inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times).
  4. Transient response of the unity-gain inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times).

1.2 Circuit Design and Test Bench

The two-stage fully differential circuit topology is the same as HW1, but with SC-CMFB implementation. The main advantages of SC-CMFB are it imposes no voltage swing restrictions and highly linear, it doesn't load the main opamp much and will not introduce additional poles in the CMFB loop. What's more, it burns no DC current. It is suited for mid-speed sampled systems for $f_{unit\ y}$ should be 3~5 times the f_s.

1.2.1 SC-CMFB Circuit

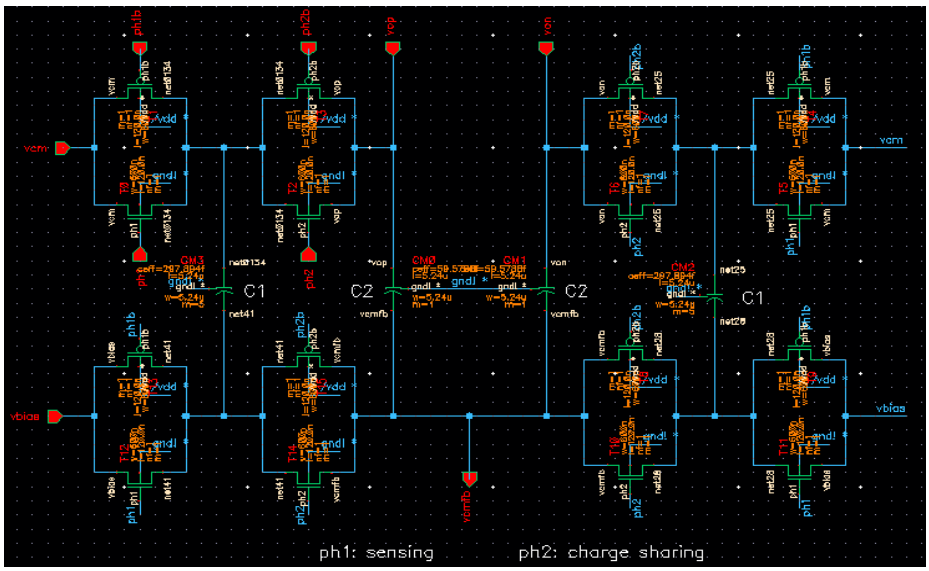

Figure 1 SC-CMFB circuit.

As illustrated in figure 1, the idea of SC-CMFB uses C2 for common-mode averaging at phase 1 and C1 transfer the stored charges to C2 at phase 2.
At clock phase 1

$$Q_{2C_1} = 2 \cdot (V_{CM} - V_{bias}) \cdot C_1$$
$$Q_{2C_2} = (V_{op} - V_{cmfb}) \cdot C_2 + (V_{on} - V_{cmfb}) \cdot C_2$$

At clock phase 2

$$Q_{total} = (V_{op} - V_{cmfb}) \cdot (C_1 + C_2) + (V_{on} - V_{cmfb}) \cdot (C_1 + C_2)$$

$$Q_{total} = Q_{2C_1} + Q_{2C_2}$$

Finally, we could get

$$V_{cmfb} = \frac{V_{op} + V_{on}}{2} + V_{CM} - V_{bias}$$

By making $V_{cmfb} = V_{bias}$, we can force $\frac{V_{op}+V_{on}}{2} = V_{CM}$.

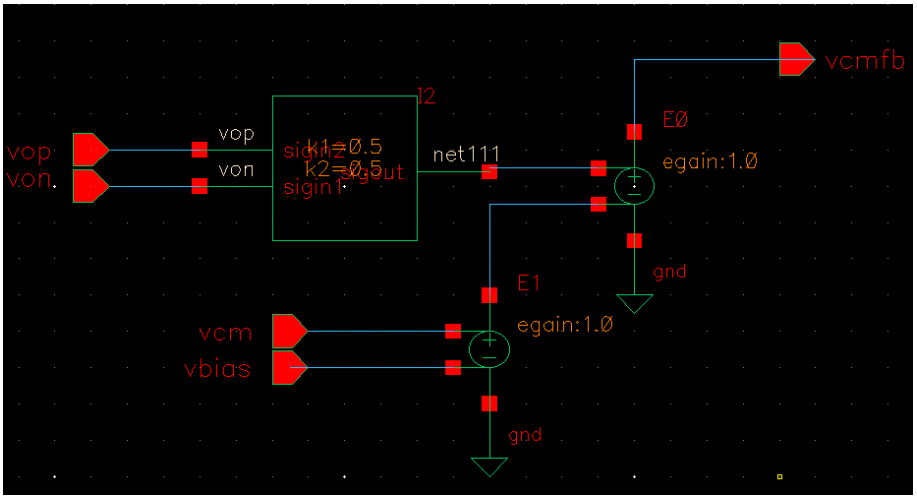

Figure 2 Ideal CMFB can be used for AC analysis.

1.2.1.1 Sizing C_1

The above equations are derived in steady-state condition. However, considering the charge injection, there will have certain amount of charge Δq being injected into C_1 and C_2 that cannot be cancelled out and left in the equation below.

$$2 \cdot (V_{CM} - V_{bias}) \cdot C_1 + \Delta q = (V_{op} - V_{cmfb}) \cdot C_1 + (V_{on} - V_{cmfb}) \cdot C_1$$

So that

$$\left(V_{CM} - \frac{V_{op} + V_{on}}{2}\right) + \frac{\Delta q}{C_1} = V_{bias} - V_{cmfb}$$

From above, we can make the conclusion that increase C_1 to minimize charge injection. CMFB loop gain and bandwidth should be large and high enough for better accuracy when V_{CM} reaches steady state. Literatures in [1] and [2] also showed that by increasing C_1 could reduce the steady state errors. However, the bandwidth of the CMFB will be affected.

1.2.1.2 Sizing C_2

C_2 must be kept less than 10% of C_L for it loads the main opamp at both phase 1 and phase 2. However, it won't be too small for it affects the CM loop gain. Let's define CM loop gain as T_{cm}. For 1st stage CMFB, we have:

$$T_{cm,1st} = \frac{C_{cm}}{C_{cm} + C_{gs,tail}} \cdot g_{m,tail} \cdot R_{out,1st} = \frac{C_{cm}}{C_{cm} + C_{gs,tail}} \cdot A_{dm,1st} \cdot \frac{g_{m,tail}}{g_{m,input}}$$

C_{cm} is C_2 at phase 1 and $(C_1 + C_2)$ at phase 2. $C_{gs,tail}$ (about 492fF in my case) is the gate capacitor of split tail current source NMOS for 1st stage CMFB control. For example, 1mV static error for 1.2V power supply means T_{cm} needs to be larger than 1000. good news

is that T_{cm} is a fraction of A_{dm}. When A_{dm} is large, T_{cm} is relative easy to meet. That's the case for the 1st stage.

For 2nd stage CMFB in the opamp HW1, we have:

$$T_{cm,2\text{nd}} = \frac{C_{cm}}{C_{cm} + C_{gs,pmos}} \cdot g_{m,pmos} \cdot R_{out,2\text{nd}}$$

$C_{gs,pmos}$ (about 31fF in my case) here is the gate capacitor of current injection PMOS for the 2nd stage CMFB control. That PMOS won't be very large for it loads the output, so that $g_{m,pmos}$ (37.78μS in my case) is small. The loop gain for 2nd stage CMFB will be intrinsically much smaller.

The minimum MIM capacitor (made of M2 and M3) value is 60fF in the PDK of IBM 130nm process. So let's choose $C_2 = 60fF$.

The larger the C_1, the faster for the outputs to reach the CM voltage level. Which can be seen in the figure below with C_1/C_2 ratio changes from 3, 5 to 7. As a rule of thumb, $C_1 \approx 5C_2$. Let's choose $C_1 = 300fF$ for the first stage CMFB. The ratio could be increased in the second stage CMFB for increase the loop gain.

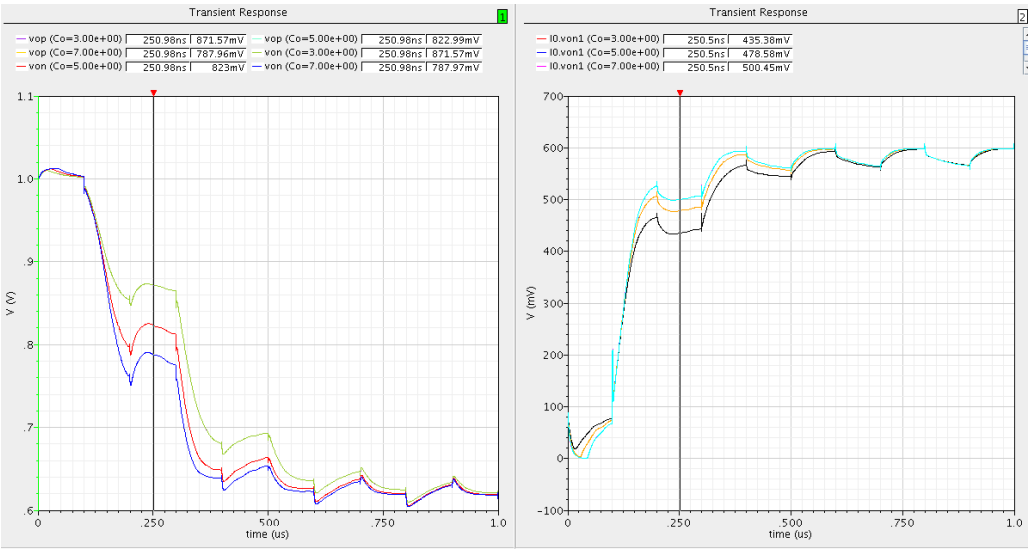

Figure 3 Common mode output waveforms with different C_1/C_2 ratios.

1.2.1.3 Sizing *Switches*

The size of the switches should be minimized in order to reduce charge injection, but the turn-on resistance which affects the RC time constant should also be considered.

$$RC \ll T_s/2$$

For $f_s = 5MHz, C = 300fF, R \ll 333k\Omega$. Which is quite easy to meet.

For $f_s = 100MHz, C = 300fF, R \ll 167\Omega$.

In this process, in order to obtain R_{on} of the TG (transmission gate) less than 166Ω at the voltage range of $|V_{th,p}| \sim (V_{DD} - V_{th,n})$, let the width of PMOS twice the NMOS, the width of NMOS should be larger than10μm. the parasitic cap will be more than 25*f*F.

Here, for the first stage CMFB, W_N and W_P are set to be 8μ and 16μ, respectively. Sizes for the second stage are tuned for the loop response accordingly.

1.2.2 Two-Stage Fully Differential Circuit

As stated before, the 2nd stage CMFB scheme for class AB output stage inherited from HW1 is not well fit at here for SC-CMFB due to intrinsically low loop gain. What's more, the replica bias in the 2nd stage CMFB has voltage ripples, V_{bias} can't be very close to V_{cmfb}, so that systematic offset build in.

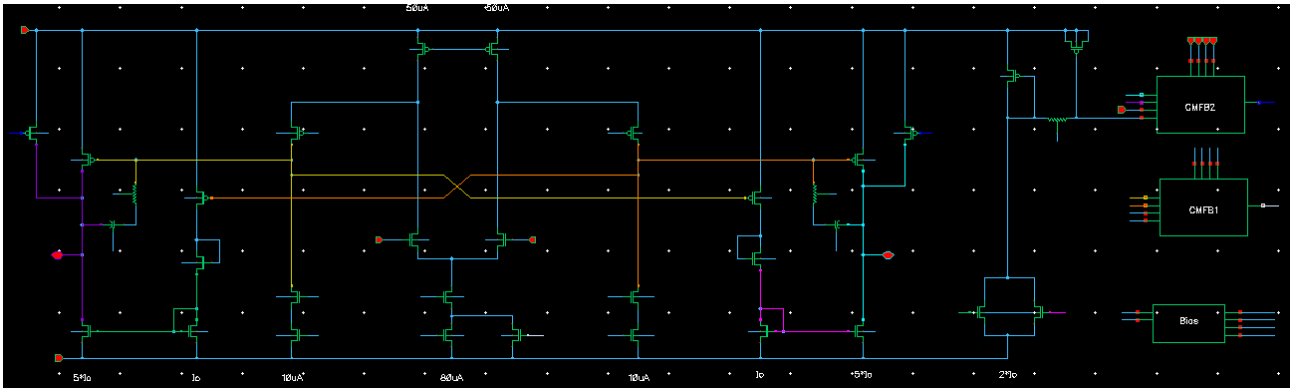

Figure 4 Schematic of 2-stage fully differential circuit with SC CMFB.

1.2.3 Simulation Test Benches

We have to resort to Periodic Steady State (PSS) analysis to analyze the stability of the sampled circuits. PSS should be performed before all PAC and PSTB analysis, which directly computes and finds a periodic steady-state of the circuit in "tstab" seconds later. Either iterative shooting Newton method or harmonic balance method can be employed for the analysis. The basic idea of the harmonic balance is to solve equations in the frequency domain first instead of directly solving equations in the time domain[3].
Page 27 in [4] gave some suggestion for high accuracy simulation. Go to Simulation →Options→ Analog →Main in the ADE window to setup tolerance options accordingly. If the frequency of periodic small signal analyses followed by PSS is high (e.g. 1G), the *maxacfreq* parameter (options→accuracy) of the PSS can be used to specify the highest frequency, otherwise, the frequency analysis in PAC/PSTB maybe truncated.

Open loop analysis are performed with PSS + PAC and AC analyses. We can set Maximum sideband to 0 in PAC for we only care about the frequency response at fundamental. For PSS we can only set the number of harmonics to 0 by choosing Shooting method, for HB method the number of harmonics should be set ≥ 1.

Loop stability analyses are performed with PSS + PSTB. For plotting bode plot, go to Results→Direct Plot→Main Form in the ADE window to plot the magnitude and phase of the selected probe in PSTB setting. Stability summary function can't be displayed, but it can be found in end the Output Log file.

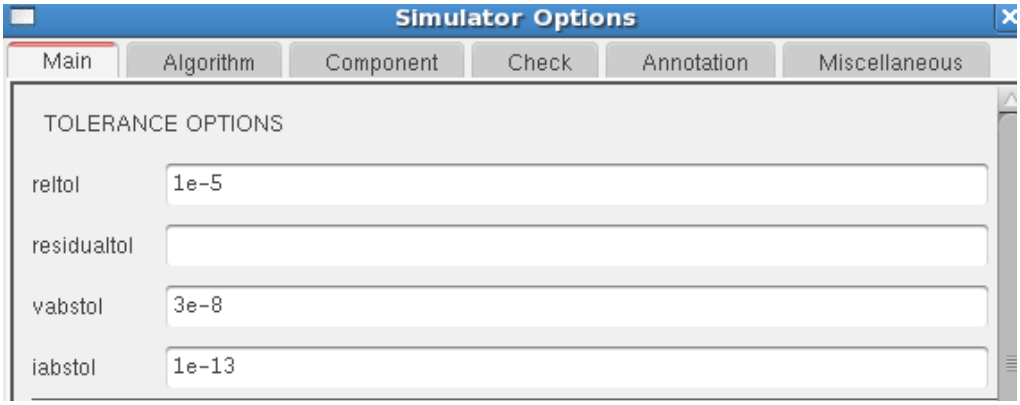

Figure 5 Periodic accuracy suggestion.

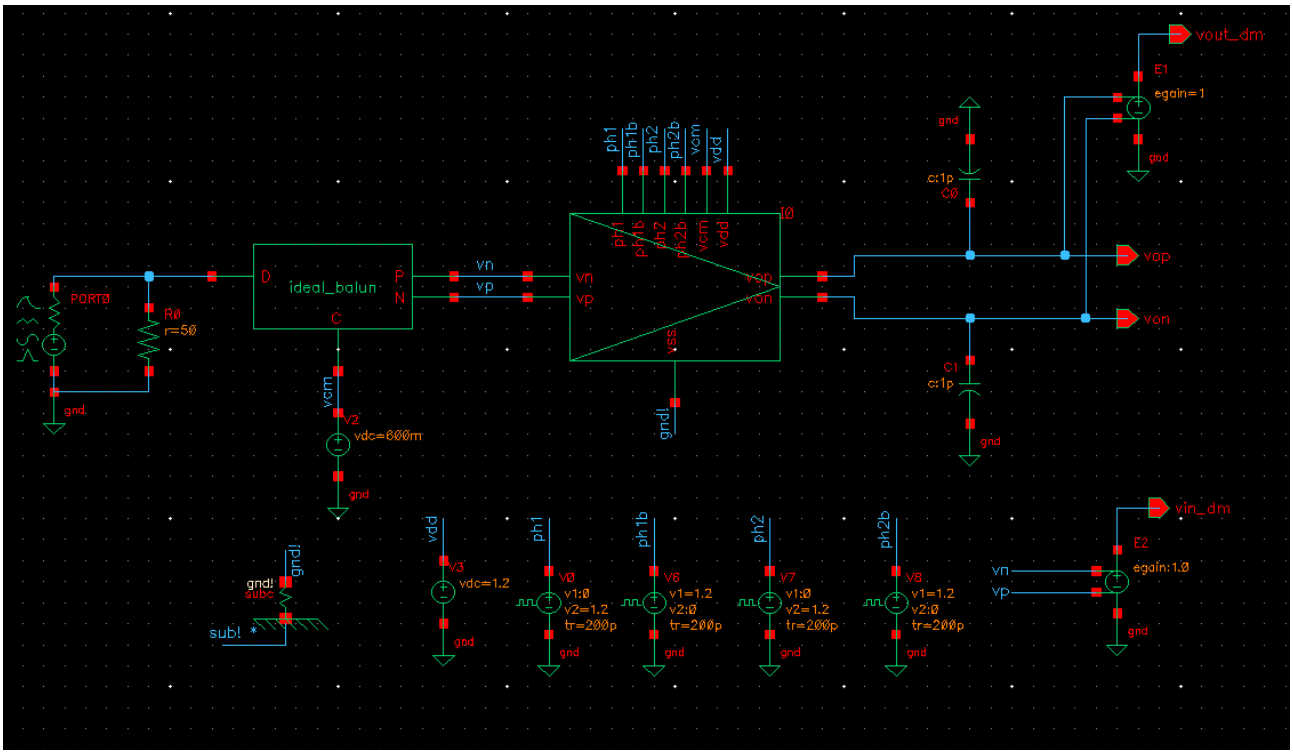

Figure 6 Differential open loop PAC/AC simulation test bench.

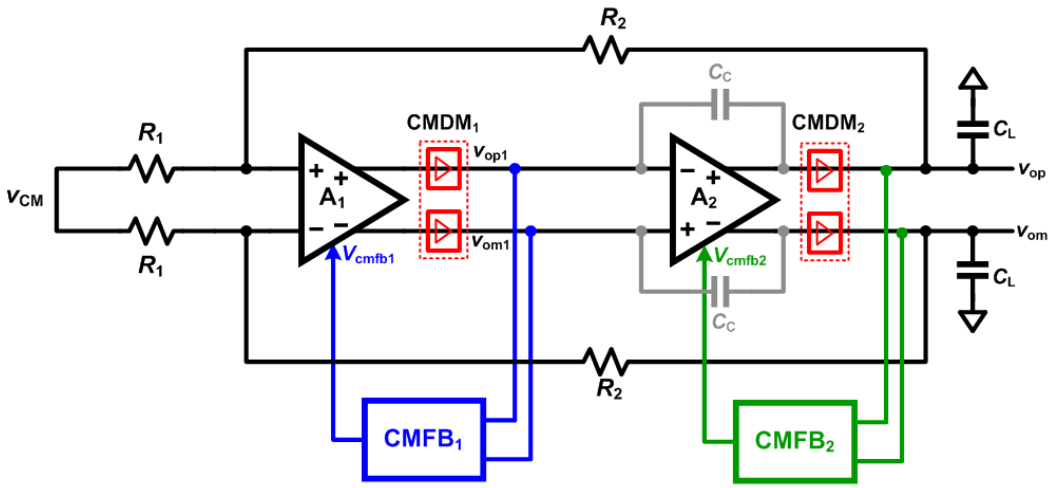

Figure 7 Top level schematic for differential closed loop PSTB analysis.

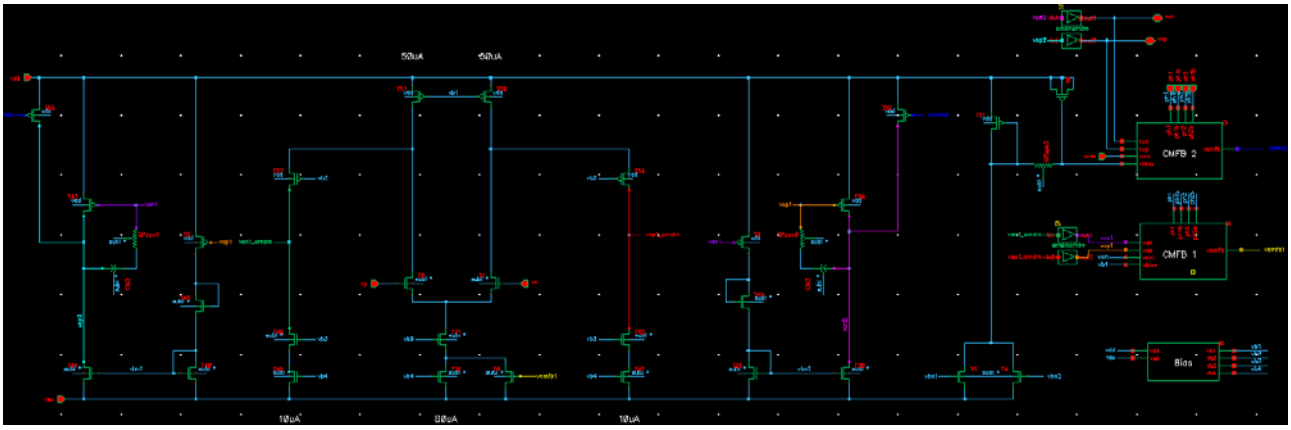

Figure 8 PSTB analysis test bench for CMFB loops.

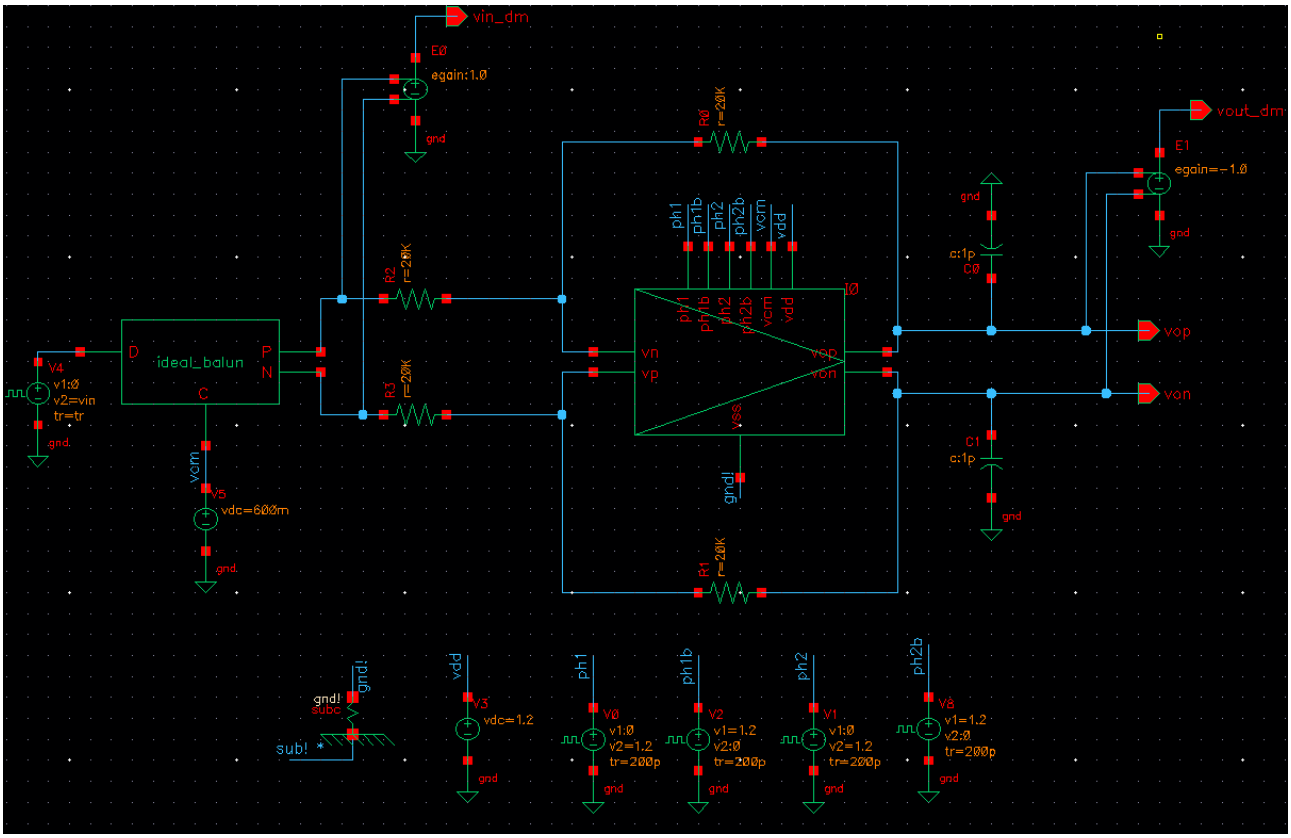

Figure 9 Unity-gain inverter transient simulation test bench for differential mode step response.

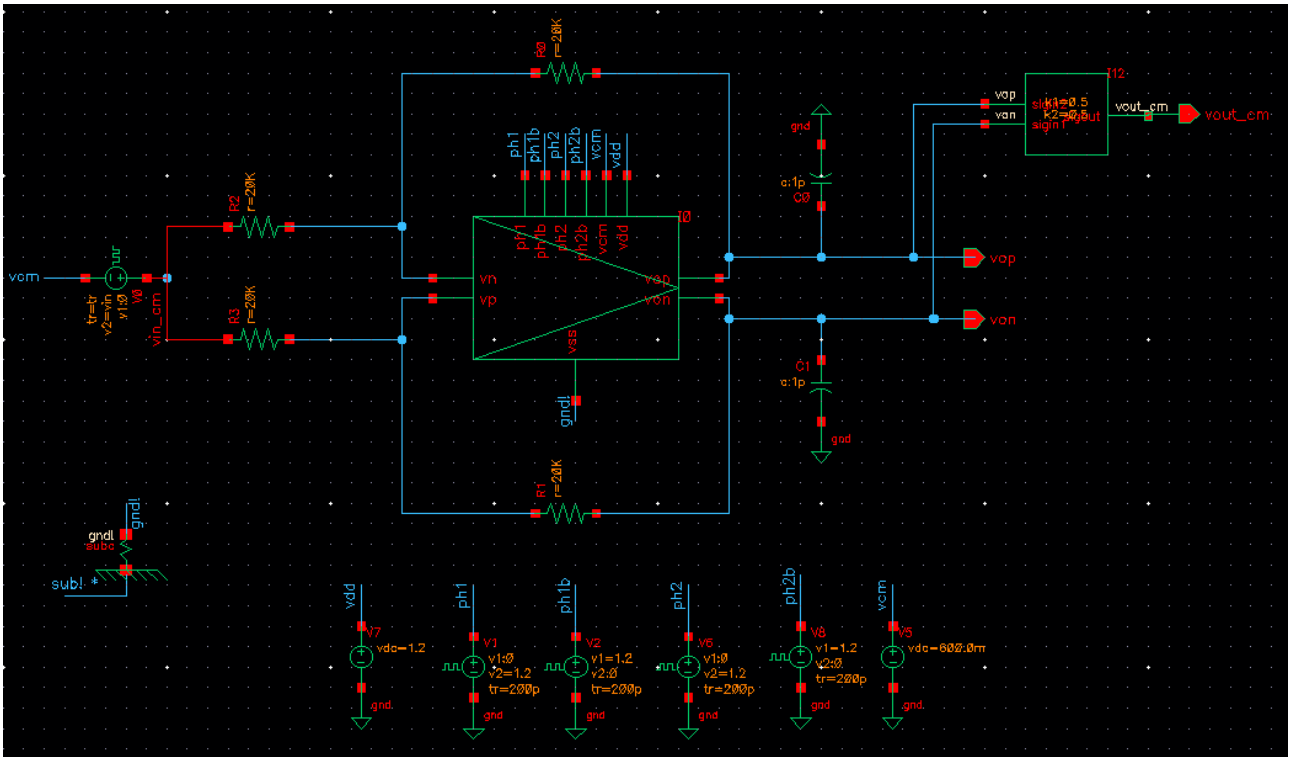

Figure 10 Unity-gain inverter transient simulation test bench for common mode step response.

1.3 Simulation Results and Summary

Since we only targeted for $f_s = 5MHz$ at here. The unity frequency in the configured application should be larger than 3~5 times f_s. Simulated result shows $f_{unity} = 49MHz$. Results for open loop, loop stability and transient response are given below with comments.

1.3.1 Open loop PAC Analysis

AC/PAC analysis in open loop opamp doesn't show any valuable information but only the open loop DC gain. What's more, the DC gain of PAC analysis is dependent to f_s for open loop. It drops as increasing f_s. For higher f_s, I don't think the PAC result is reliable at all. An ideal CMFB with real CMFB loading is used to perform AC analysis for comparison. Once more, the phase margin and unity bandwidth should be analyzed in real application, for open loop it doesn't mean anything.

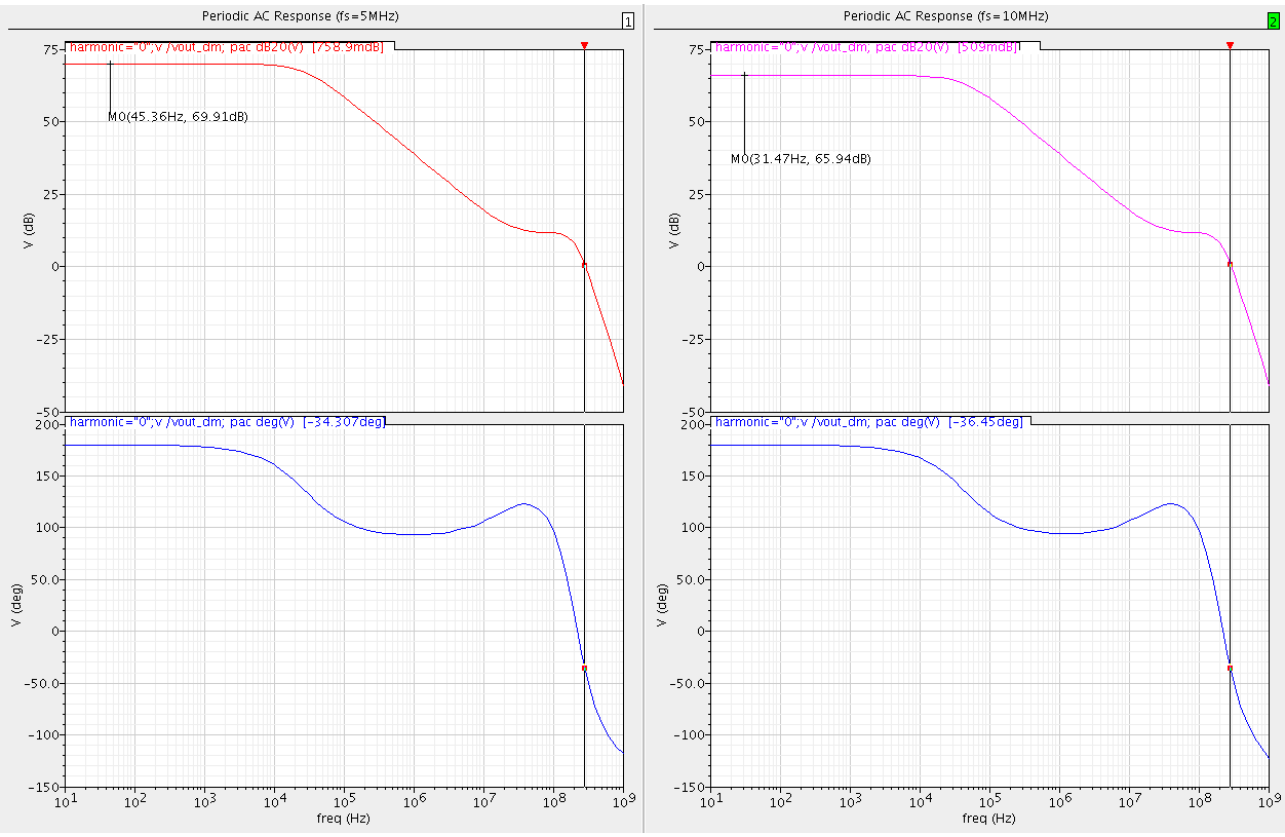

Figure 11 Differential open loop bode plot with PSS+PAC analysis.

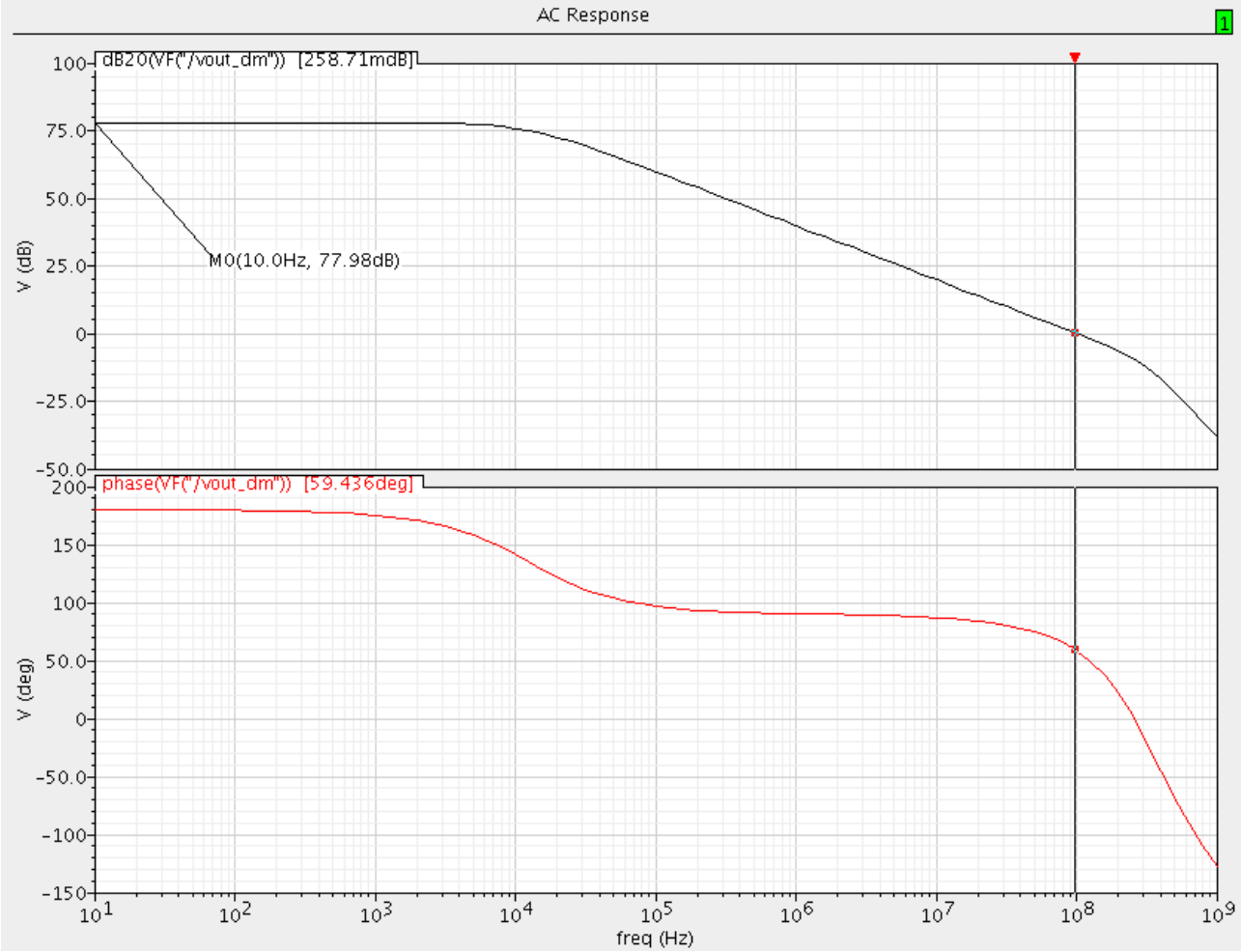

Figure 12 Differential open loop bode plot with ideal CMFB AC analysis.

Table 1 Open loop frequency analysis summary.

Items	DC Gain (dB)
AC with ideal CMFB	77.98
$f_s = 5MHz$	69.93
$f_s = 10MHz$	65.98

1.3.2 Loop PSTB Analysis when Configured at Resistive Feedback

Differential mode and individual CMFB loop stabilities are characterized. DM phase margin is tuned close to 63° for best transient settling. f_{unity} of 49MHz is enough for 5MHz sampling. Both CMBF loops are single stage, so that the phase margin and gain are high and low, respectively. Low gain and f_{unity}, high PM, especially for the 2nd stage CMFB loop, degrades the performance of the opamp.

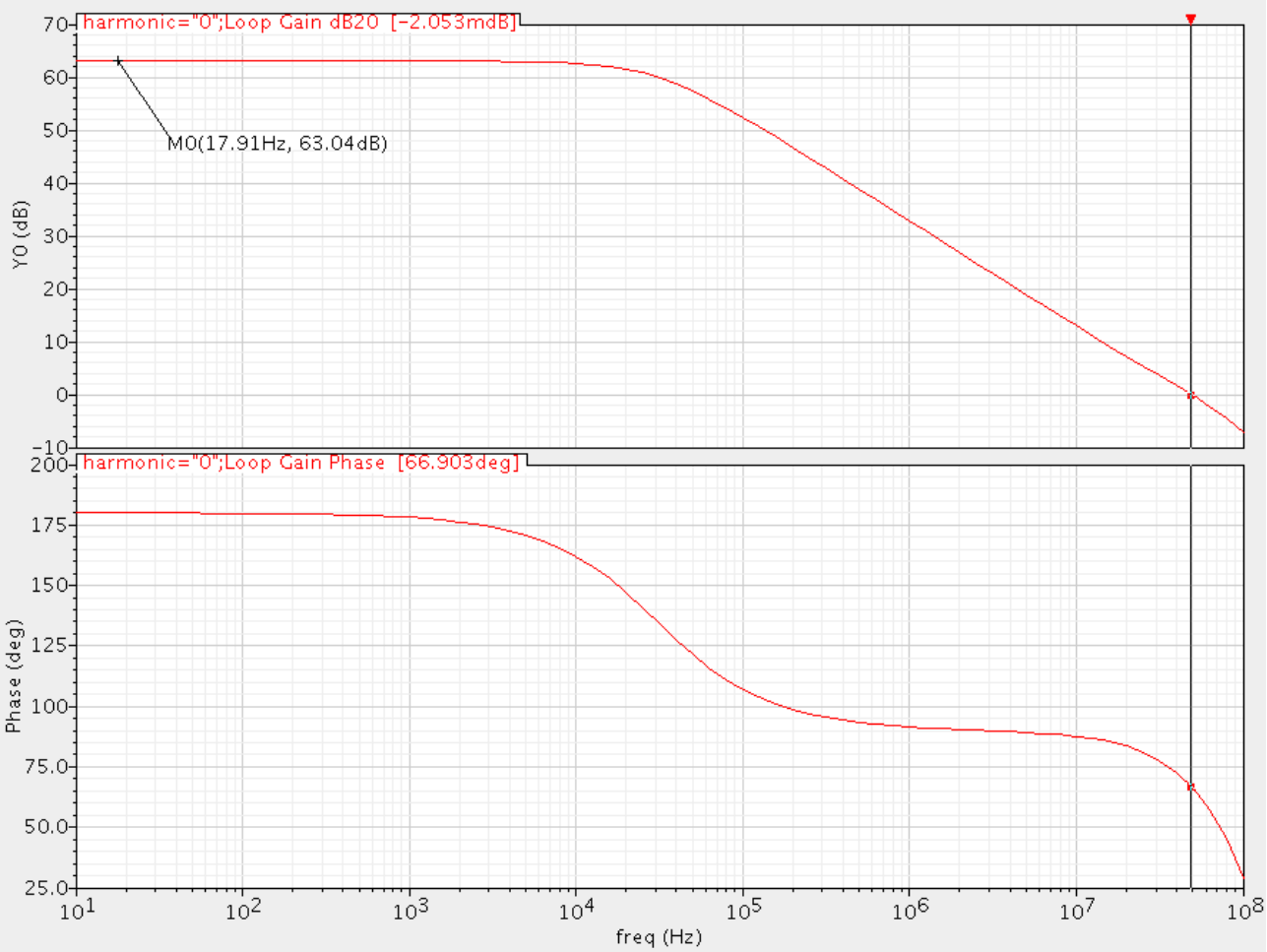

Figure 13 DM loop bode plot with pstb analysis.

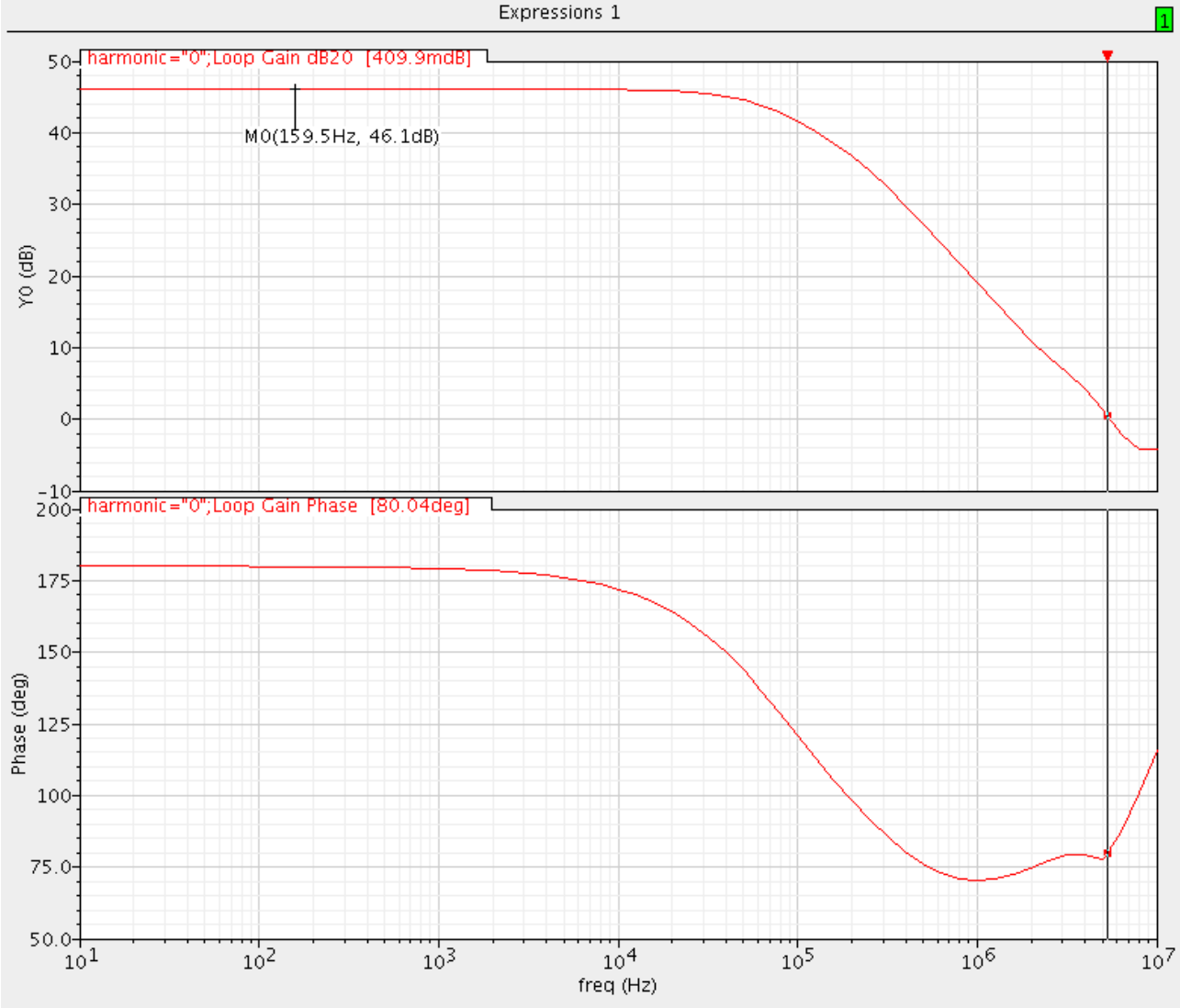

Figure 14 CM loop bode plot for 1st stage CMFB with cmdmprobe.

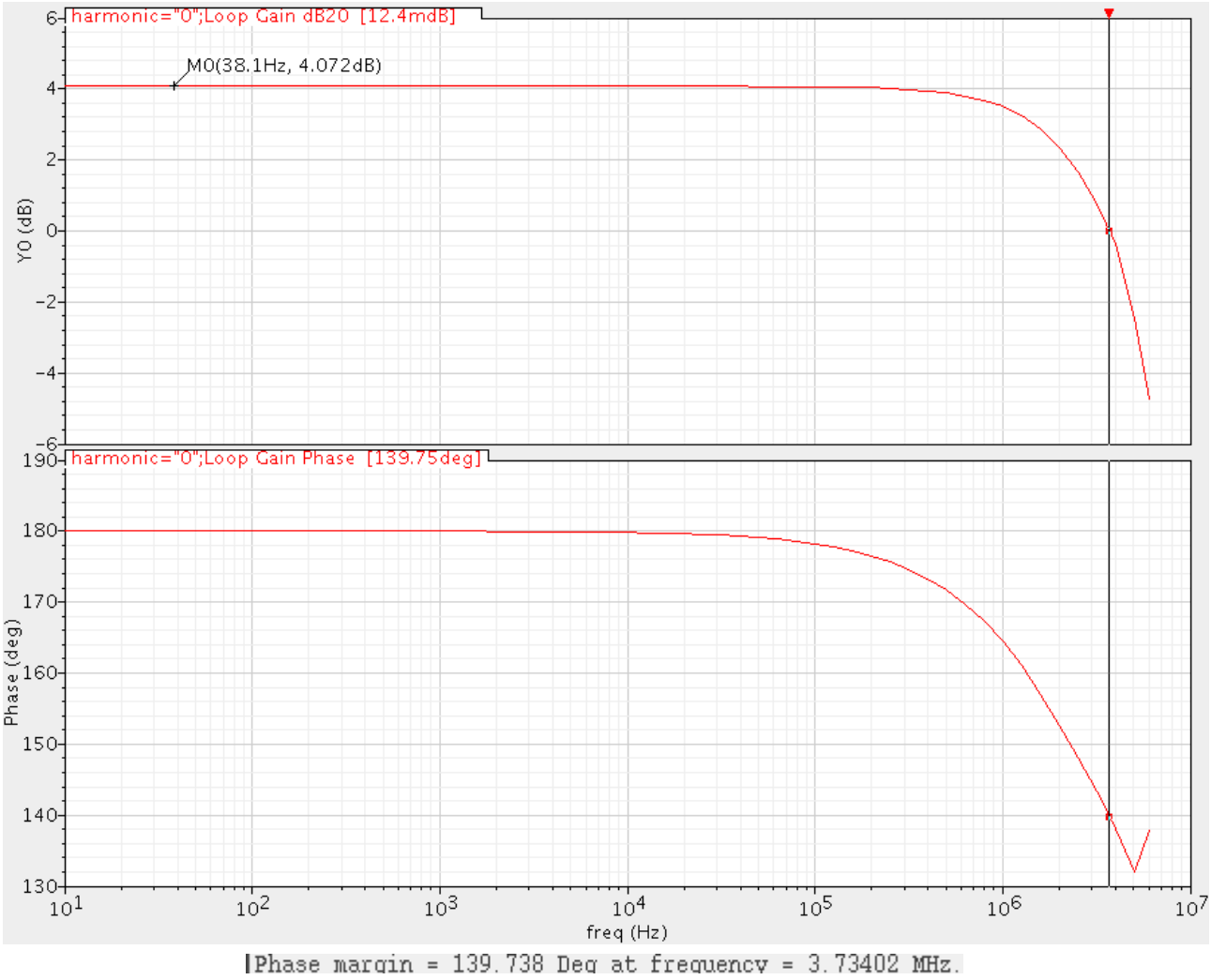

Figure 15 CM loop bode plot for 2nd stage CMFB with cmdmprobe.

Table 2 Summary of pstb analysis for the three feedback loops in resistive feedback.

Items	DC Gain (dB)	PM (°)	GBW (MHz)	CMDM options
1st stage CMFB	46.1	79	5.3	CMDM=1
2nd stage CMFB	4.1	139.7	3.7	CMDM=1
DM loop	63	67	48.6	CMDM=-1

1.3.3 Differential/Common Mode Transient Response

Differential and common mode pulse responses with pulse width and period of 200n and 400n as input stimulus are simulated to check the output responses.

There have some ringing for the differential mode one which may due to inefficient 2nd stage CMFB loop.

For output common mode voltage, it has about 18mV ripple with 100mV input disturbance. The attenuation is only 14.8dB, which is not good as expected.

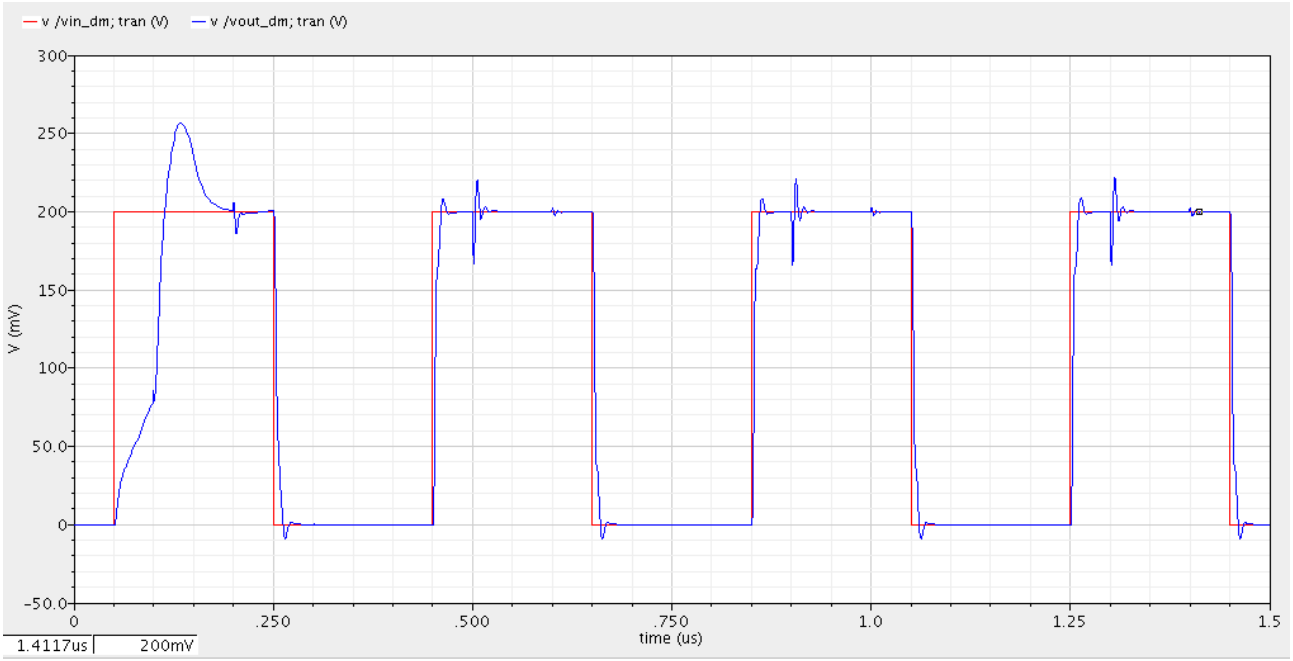

Figure 16 Unity- gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse with=200ns, in test bench set output VCVS gain=-1).

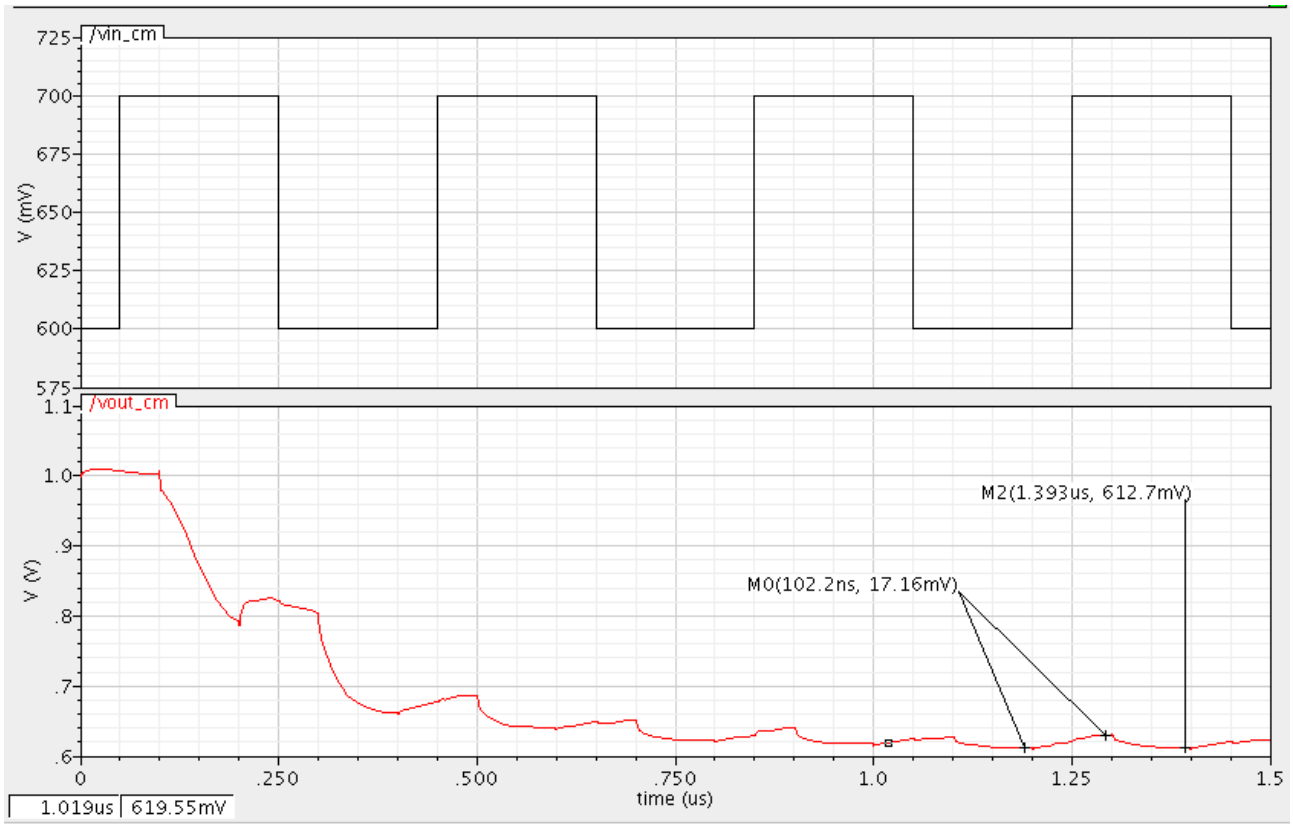

Figure 17 Unity- gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse with=200ns, in the test bench veriloga adder is used for averaging).

2 Sample Hold Circuit Implementation

- ✓ **Requirements**:
  Use the opamp in problem 1 in the sample hold circuit show below. Use f_s of 5 MHz and $C_H = C_L = 0.5pF$. May use ideal switches with on resistance of 1kΩ.
- ✓ **Simulation list**:
  1. Verify DM and CM loop stability and show relevant plots.
  2. Simulate the transient response of the circuit for a sinusoidal input with $1.2V_{pp}$ differential amplitude and input frequencies of $f_{in} = \frac{1}{4}MHz$ and $f_{in} = \frac{11}{4}MHz$. Plot the output waveforms.

2.1 Simulation Test Benches

Opamp put into sample hold configuration for loop stability and transient are simulated. Loop stability should be checked again since it is in different application. Some device parameters are changed to achieve optimal phase margin.
Ideal switches are used so that parasitic capacitances are ignored.

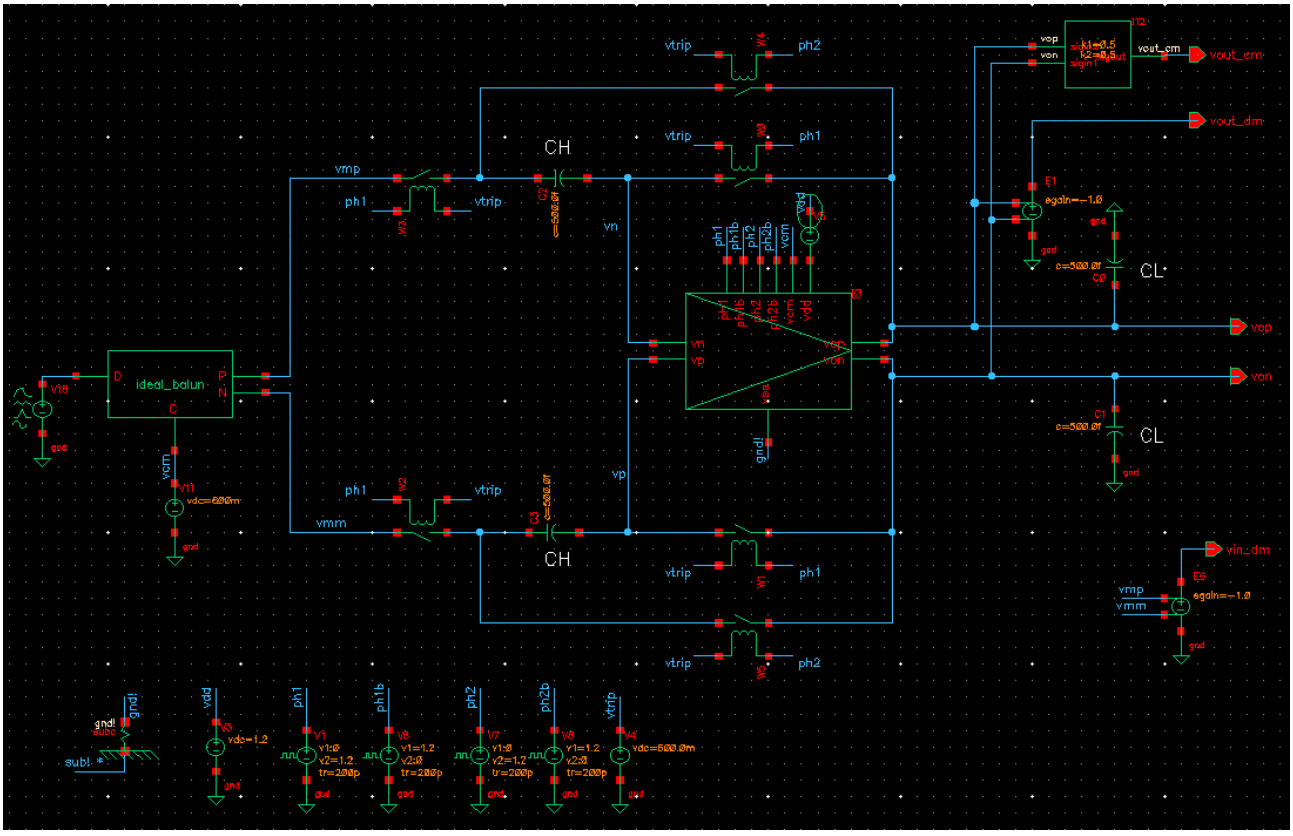

Figure 18 SH configuration transient analysis test bench.

2.2 Simulation Results and Summary

Loop stability characteristics are changed a lot by comparing to the resistive feedback one. f_{unity} of DM increased to 125MHz, one reason is C_L is halved.
For easy comparison, loop stability summaries for resistive feedback are repeated in table 3 with for sample hold circuit.
It can be seem that the 2nd stage CMFB performance is even worse.

Table 3 Summary of pstb analysis for the three feedback loops in sample hold circuit.

Application	Items	DC Gain (dB)	PM (º)	GBW (MHz)
Sample hold	1st stage CMFB	45.9	84.6	6.1
	2nd stage CMFB	1.31	158.4	1.5
	DM loop	62.9	64.1	125
Resistive feedback	1st stage CMFB	46.1	79	5.3
	2nd stage CMFB	4.1	139.7	3.7
	DM loop	63	67	48.6

Transient responses with input sine waves at 250KHz and 2.5MHz (Nyquist frequency) with differential mode peak-to-peak amplitude of 1.2V are checked.

2.2.1 Loop Stability Analysis

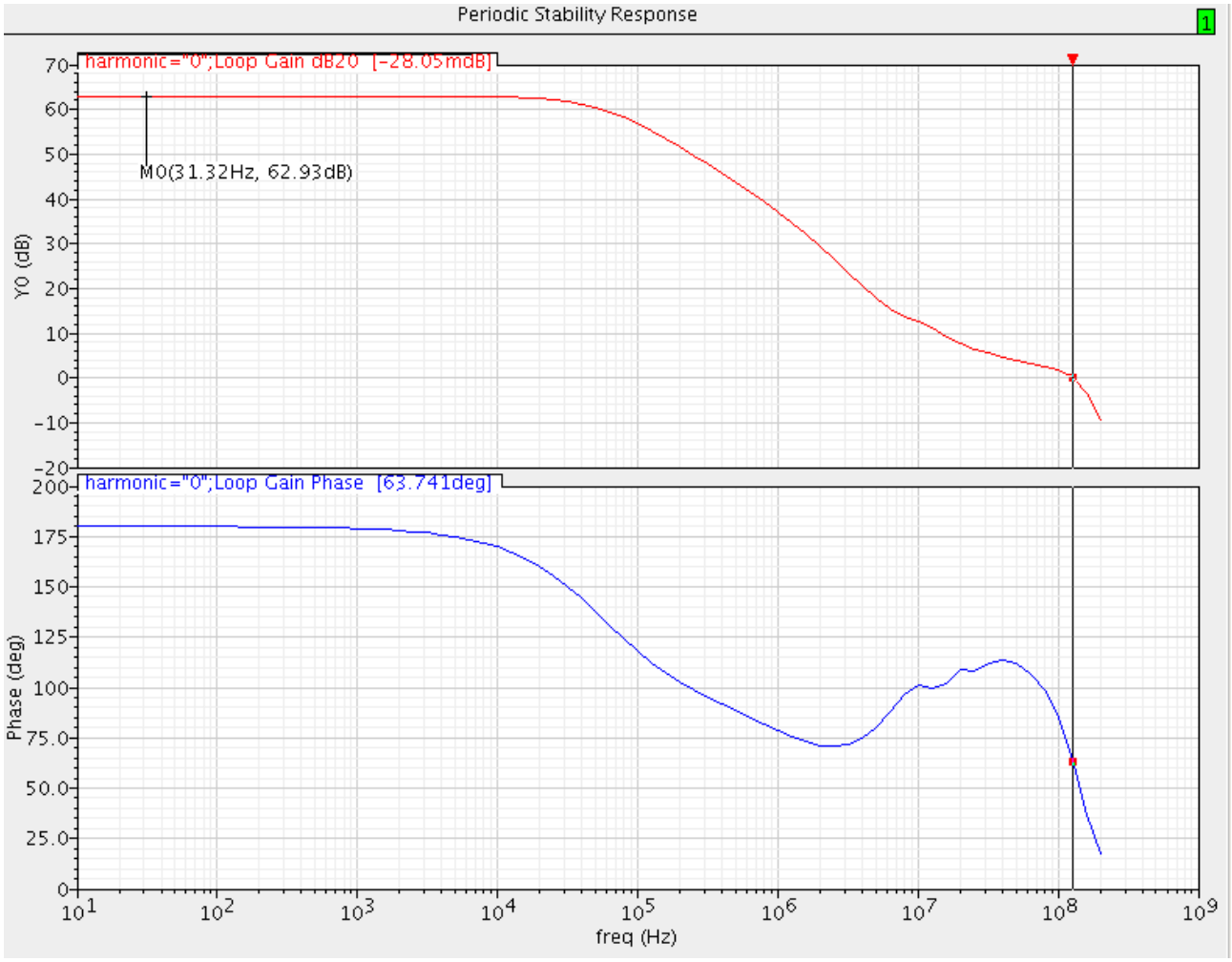

Figure 19 Sample-Hold DM loop stability.

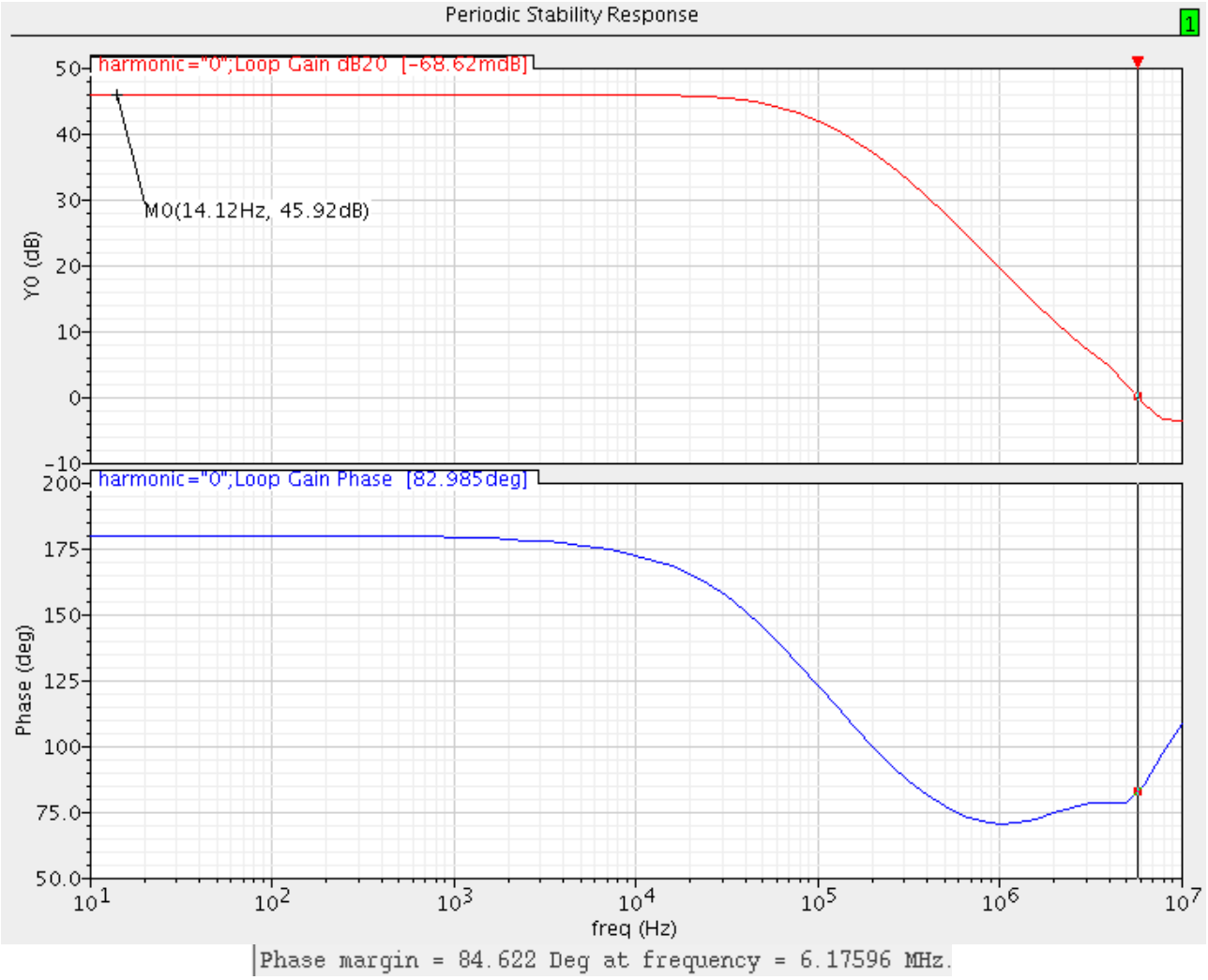

Figure 20 Sample-Hold 1st stage CMFB loop stability.

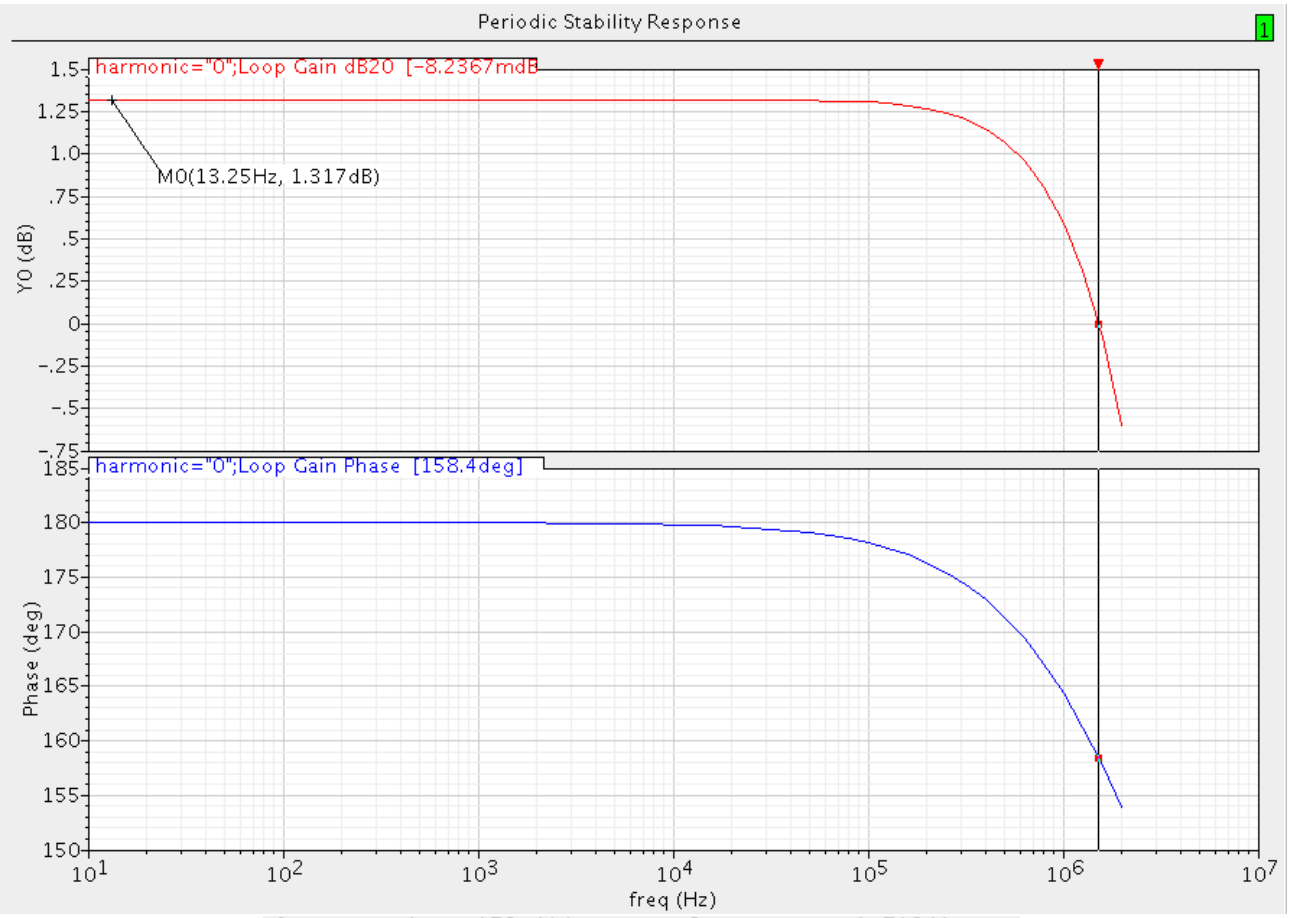

Figure 21 Sample-Hold 2nd stage CMFB loop stability.

2.2.2 Transient Analysis

The common mode output voltage seems correct for both cases, but differential mode output is not well behaved for the latter.

Question: Since the DM bandwidth looks enough, CM loop limitation can affect DM response?

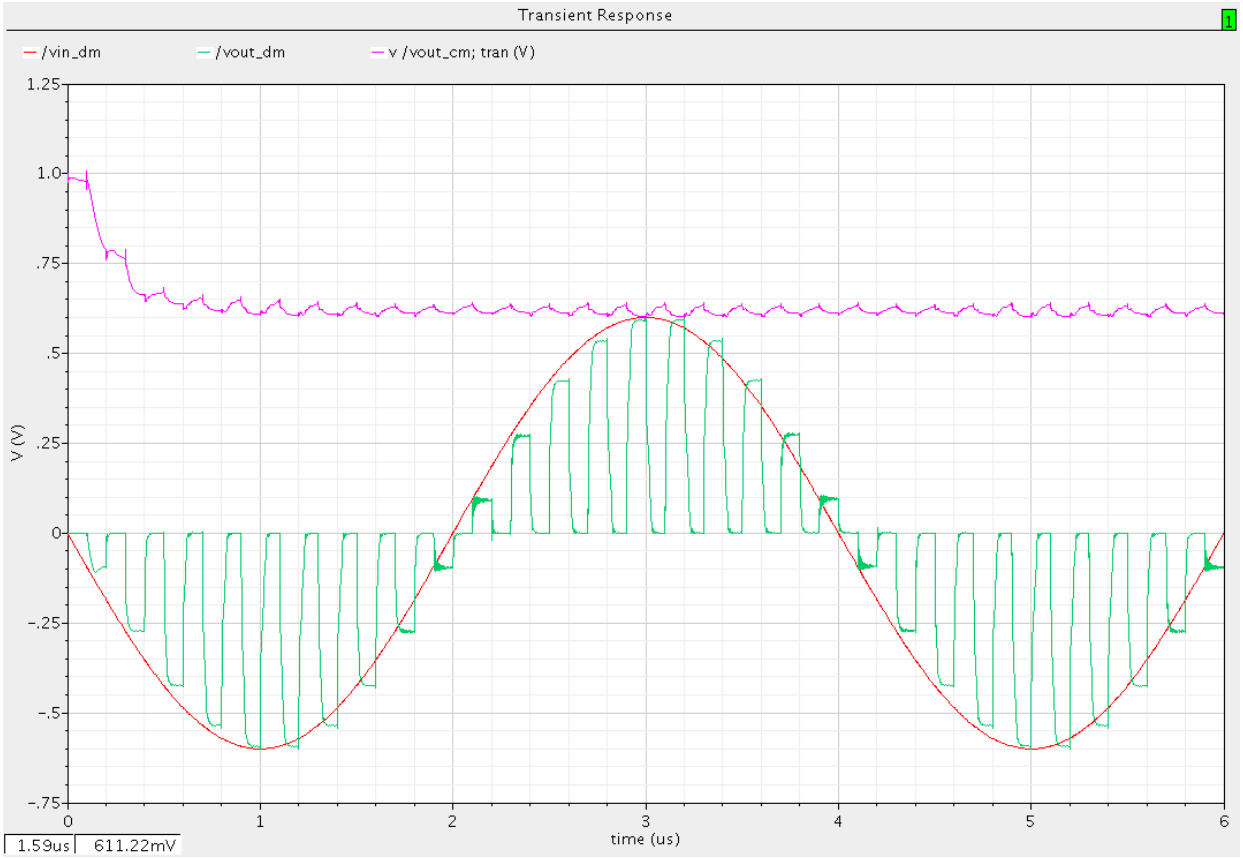

Figure 22 DM and CM outputs waveforms when $f_{in} = 1/4MHz$.

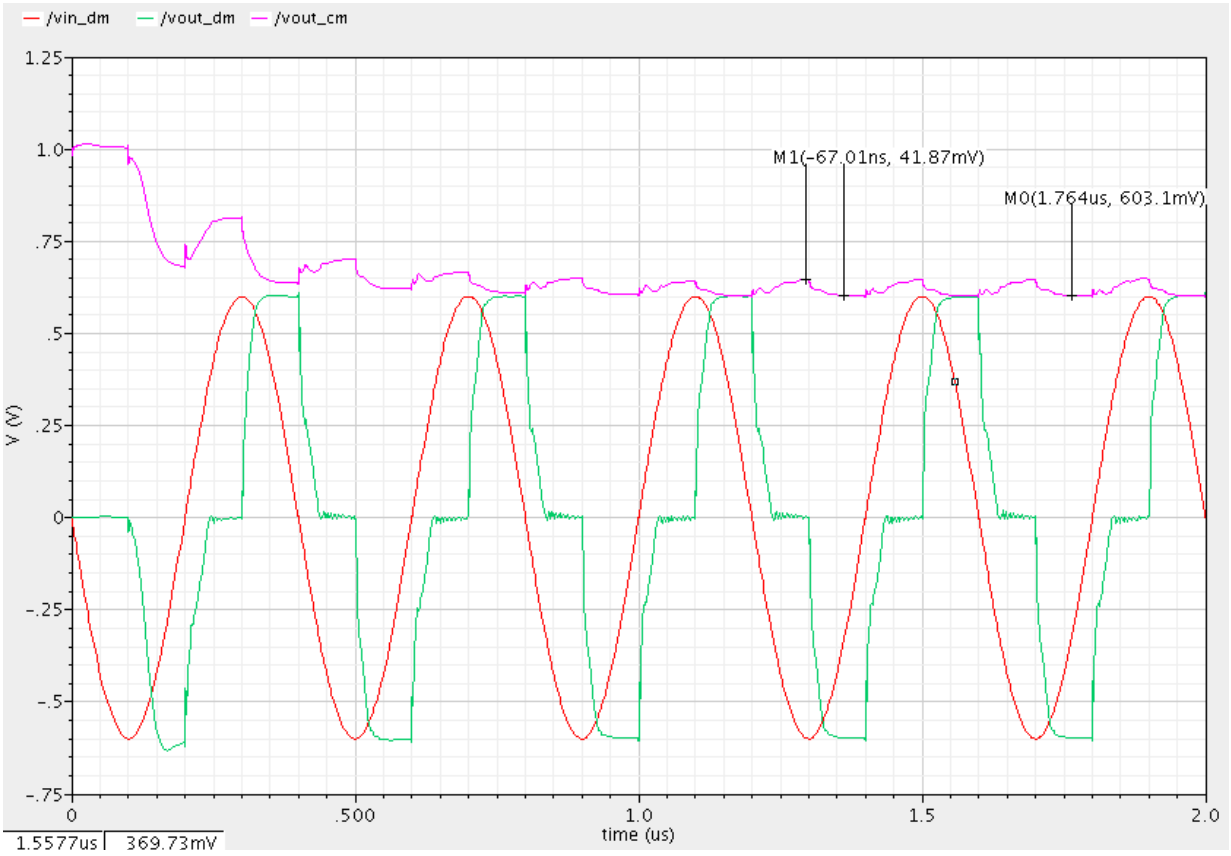

Figure 23 DM and CM outputs waveforms when $f_{in} = 10/4MHz$.

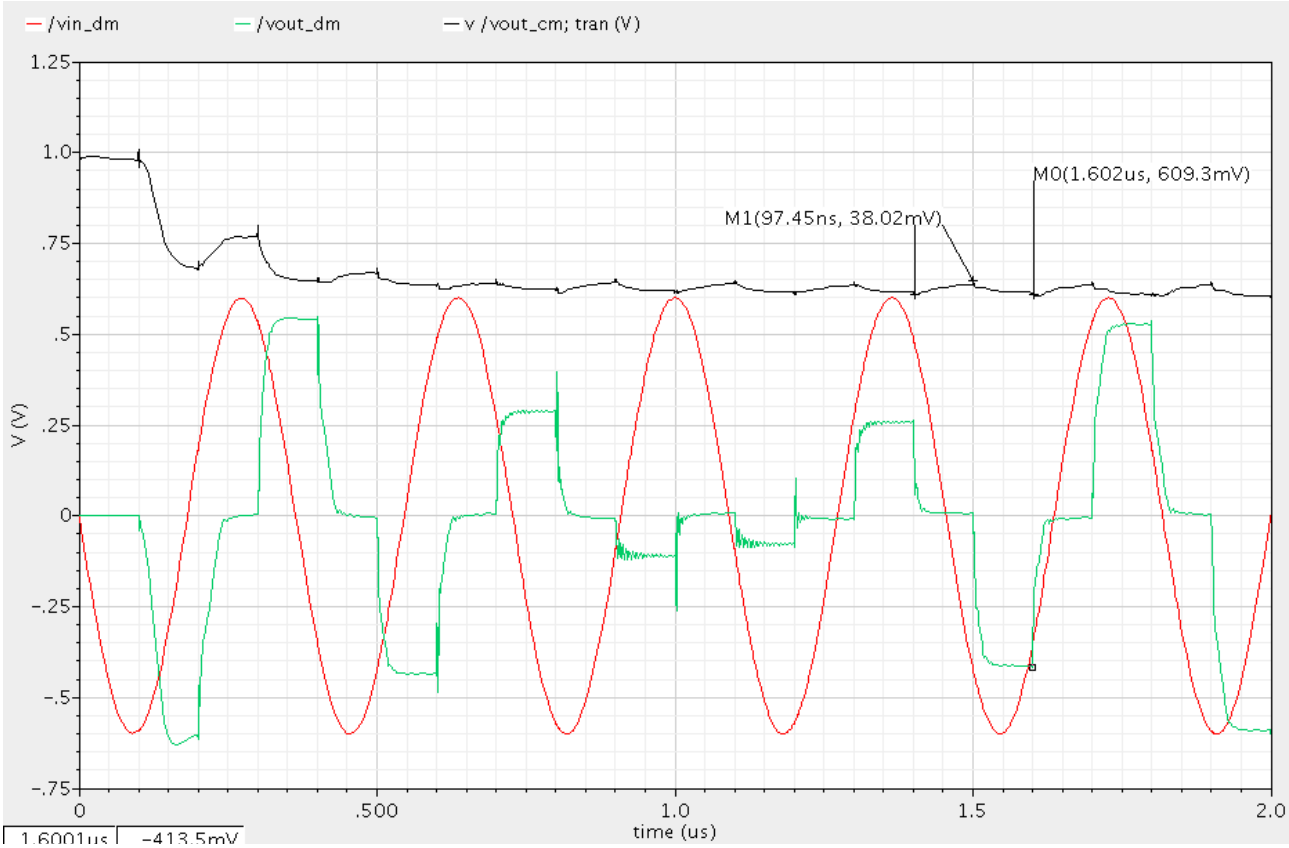

Figure 24 DM and CM outputs waveforms when $f_{in} = 11/4MHz$.

3 Conclusion

The 2nd stage CMFB is very low gain and bandwidth but didn't affect differential mode that obvious. Even the overall CM response looks not bad, either. For higher 2nd stage CMFB loop gain and bandwidth, we should resort to other methods such as insert a gain stage between SC-CMFB output and the gates of those PMOS, or use single CMFB in 2-stage opamp.

The speed is low which may due to slew rate limitation and should be analyzed in the future. PSS+PSTB are performed for stability analyses, which is essential for sampled circuit.

The rms current of the opamp excluding bias generator is 1.36mA.

4 References

1. Choksi, O. and L.R. Carley, *Analysis of switched-capacitor common-mode feedback circuit.* Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, 2003. **50**(12): p. 906-917.
2. Bula, C. and M. Jimenez, *Practical Considerations for the Design of Fully Differential OTAs with SC-CMFB*, in *IEEE Latin American Symposium on Circuits and Systems*. 2010.
3. *Harmonic Balance Release Note*. 2010, Cadence Design Systems.
4. http://www.seas.gwu.edu/~vlsi/ece218/SPRING/reference/tutorial_cadence_sparameters.pdf.