# Homework 2

ECE 614 – CMOS Analog IC Design

Due on Thursday, Oct 11, 2012

**Note**: Use the provided 130n CMOS process with $V_{DD} = 1.2\,V$ for all the problems. Clearly show your neatly drawn schematics with transistor types and sizes. Present your calculations and result plots with proper labels and annotation.

**Problem 1:** In the opamp designed in HW1, replace the common-mode feedback circuits by switched-capacitor common-mode CMFB. You can relax the load specification to 1 pF. Use a clock frequency ($f_s$) of 5 MHz. Appropriately size the switches and capacitors in the SC-CMFB circuit. Use PSS and PSTB for sampled circuit stability analysis.

**(a)** Discuss the impact of sizing of $C_1$ and $C_2$ capacitors in SC-CMFB on loop-stability and transient settling.

**(b)** Plot the following results:

1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
2. Common-mode loop (s) gain-magnitude and phase. Indicate the phase margin.
3. Transient response of the unity-gain inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times).
4. Transient response of the unity-gain inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times).

**Problem 2:** Use the opamp configuration in problem 1 in the sample-and-hold circuit shown in Figure 1. Use ($f_s$) of 5 MHz and $C_H = C_L = 0.5$ pF. You may use ideal switches with on resistance of $1k\Omega$.

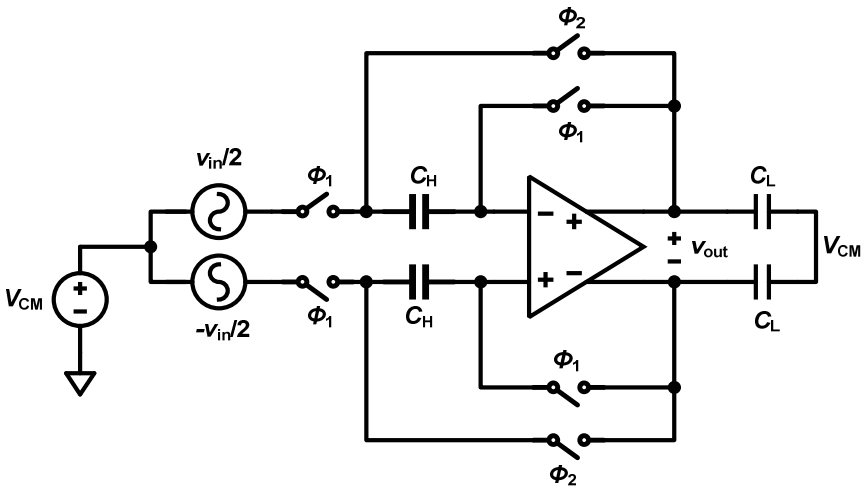


**Figure 1:** Fully-differential opamp in feedback configuration.

**(a)** Verify loop DM and CM loop-stability and show relevant plots (Be creative with simulation test-benches here).

**(b)** Simulate the transient reponse of the circuit for a sinusoidal input with $1.2\,V_{pp}$ differential amplitude and input frequencies of $f_{in} = \frac{1}{4}$MHz and $\frac{11}{4}$MHz. Plot the output waveforms.