Revision History

Ver. #	Rev. Date	Rev. By	Comment
0.0	9/15/2012	Kehan Zhu	Initial draft
1.0	9/16/2012	Kehan Zhu	Remove class A part
2.0	9/17/2012	Kehan Zhu	Comments and problem 2 added
3.0	10/3/2012	Kehan Zhu	cmdmprobe re-simulation, add supplement

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1 Two-stage fully-differential Opamp design

1.1 Spec. and Requirement

- ✓ **Process**: IBM 130nm CMOS, 1.2V nominal power supply voltage.
- ✓ **Specification**: Closed loop gain and -3dB bandwidth are 2 and 20MHz, respectively. $C_L = 5pF$. Rail-to-rail output swing. Open loop gain 70dB. $V_{CM} = V_{DD}/2$.
- ✓ **Requirements**: individual CMFB loops; No systematic offset in CMFB loops; Compensate all the three feedback loops for PM of 60º. Pass tt and ssf corners.
- ✓ **Simulation list**:

1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
2. Differential closed loop gain-magnitude and phase. Indicate the -3 dB bandwidth.
3. First stage common-mode loop gain-magnitude and phase. Indicate the phase margin.
4. Second stage common-mode loop gain-magnitude and phase. Indicate the phase margin.
5. Transient response of the unity-gain inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times).
6. Transient response of the unity-gain inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times).

1.2 Circuit Design and Test Bench

In order to go through the CFMB and compensation theory, Class A output is first designed. Then Class AB output stage is implemented. Here, only class AB topology result is shown. ADE XL is used to do corner simulation. Schematic simulation are performed at 1.2V power supply, 40ºC temperature, tt and ssf corners.

1.2.1 Bias Circuit

Bias circuit generates voltages for vb1, vb2, vb3, vb4 used to bias the current source/sink used in the fully differential opamps. Assume we get a reference voltage of 600mV and a 10 µA@27ºC PTAT current from BGR. As a rule of thumb, set the temperate coefficient of the PTAT current to be 0.067µA/ºC in the simulation.

A regulated current reference with external precision 60K Ohm resistor to generate a 10µA current into high swing current source to generate bias voltages for the opamp.

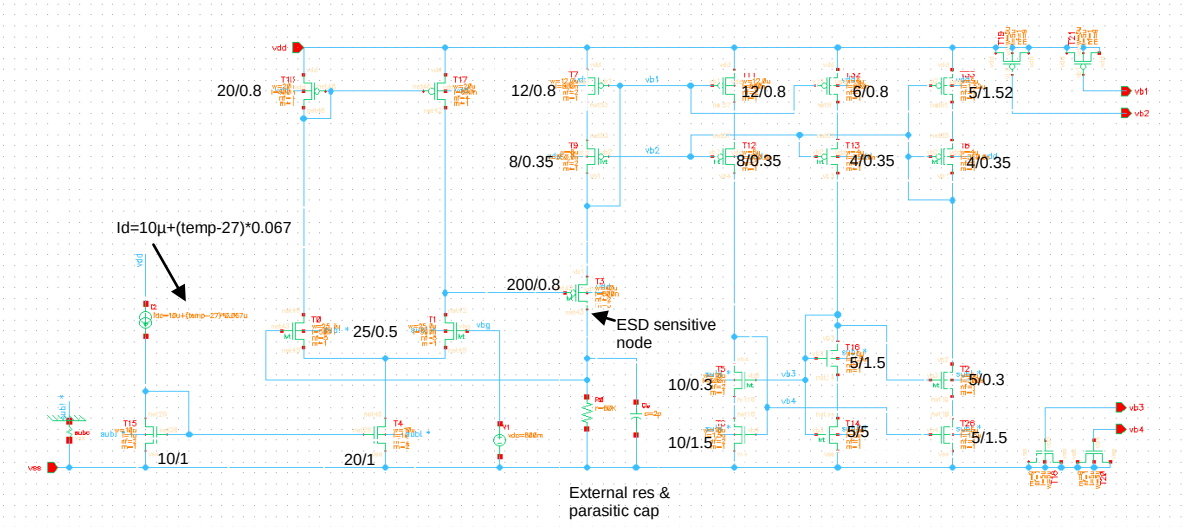


Figure 1 Bias generation circuit schematic.

1.2.2 Two-Stage Fully Differential Circuit

- Opamp topology:
  Folded-cascode opamp topology is chosen as the first stage for 1.2V nominal power supply and to obtain high DC gain. Class AB output stage is used to extend the signal swing. Separate CMFB scheme is used for both stages to set each output to well defined common mode voltage level, here is 600mV. The quiescent output voltage at nodes vop1 and von1 sets the quiescent currents in the second stage[1].
  Look at the common mode picture as shown in Fig 3, at high frequencies, the 2nd-stage compensation capacitor $2C_C$ can be considered as short, the common mode output impedance of the class AB consists of the parallel combination of the positive resistance of the diode connected (through $2C_C$) transistor M8 and the negative resistance formed by the loop M4-M6-M7. In the presence of mismatches, it is possible for the common mode output impedance to have a negative real part and lead to instability. To prevent this and ensure stability and reliable operation of the CMFB loop, quiescent current in the upper PMOS, which contributes to the positive resistance, should be made larger than quiescent current in the lower NMOS [1]. My design missed this point!
- CMFB topology:
  Since the output swings of the first stage is modest in closed loop applications, the linearity of the common mode detector is not critical[1]. we can use Dual-Diff amp scheme to merge the CM detector and the error amplifier as a one. And it doesn't load the first stage that much.
  For class AB output stage, since the signal swings are large, linear operation of the CMFB mechanism is ensured by using resistive averaging to detect the output common mode. Parallel cap is added to form high frequency path to cancel the pole introduced by the parasitic cap of the error amplify input pair. The resistor should be large enough to ensure high output impedance. The feedback node is acting as a VCCS to control the gate of a PMOS by injecting current to tune output common mode level.
- Compensation:
  There are two internal common mode feedback loops and one external feedback loop, so that the circuit should be compensated to ensure stability. For the 2-stage opamp and 1st-stage CMFB loop, miller compensation is simply used.
  The 2nd-stage CMFB loop is also a 2-stage opamp as can be clearly seen in the CM picture illustrated in Fig 3. In order to make sure the loop is stable and avoid using miller cap loading the output, I just change the load of the error amplify to diode connected, make it one pole system but sacrifice the gain. Actually, it may be better to use miller compensation for higher gain and smaller systematic offset introduced by matching. But I have limited time to go back and re-simulate.
- Minimize systematic offset:
  The current density in the error amplify should be matched to the current density in the main stage opamp. The gates bias of current source of the second stage CMFB error amplify are tied as shown in Fig2. Since it's diode connected load, the W/L of the PMOS load is a little different with the W/L of the feedback controlled PMOS.

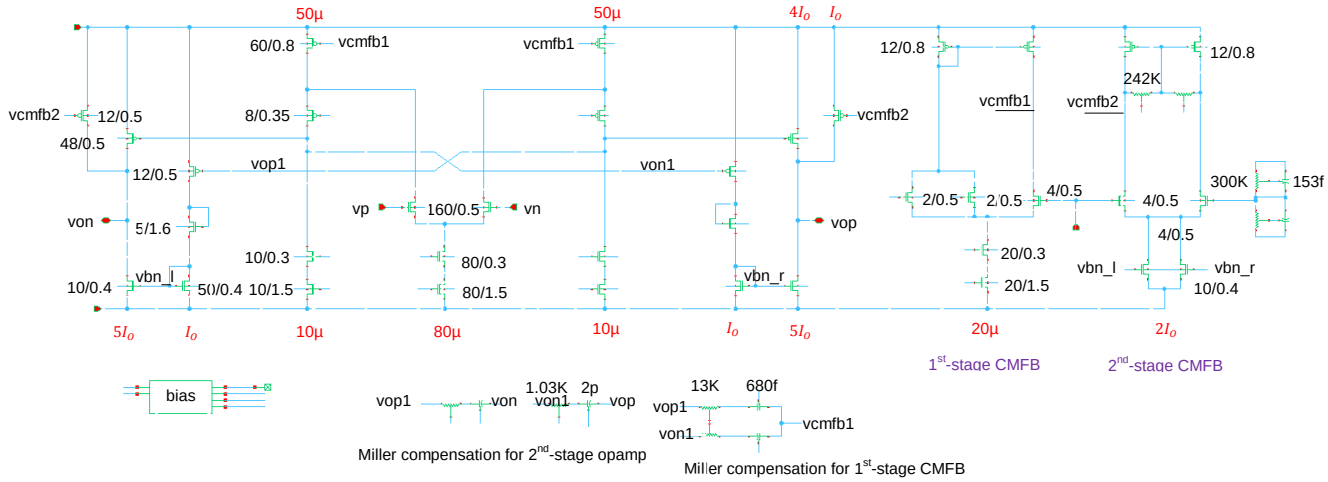


Figure 2 Schematic of 2-stage fully differential circuit with class AB output stage.

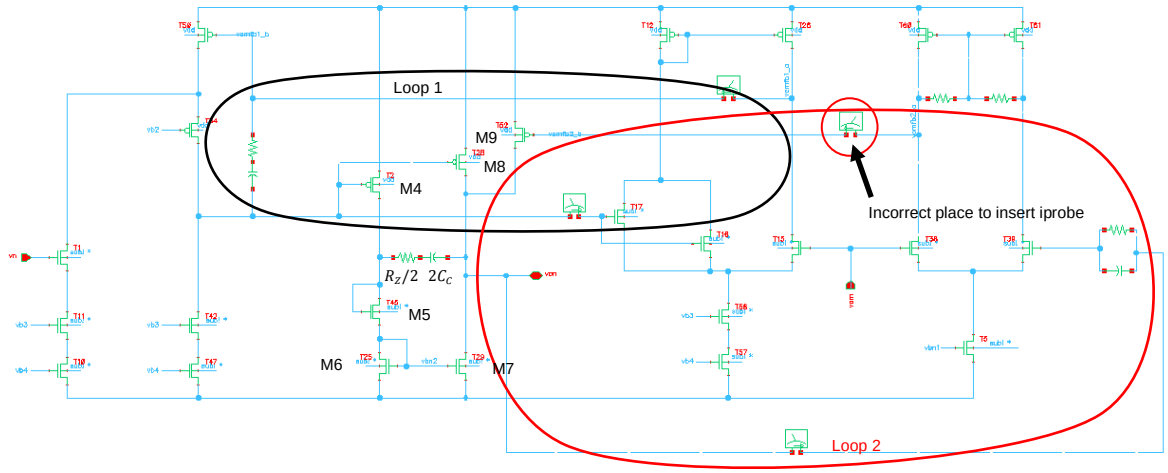


Figure 3 Two-stage common-mode picture.

1.2.3 Simulation Test Bench

Open loop and closed loop frequency analysis are performed by AC simulation.

Fig 4 is used to perform stability analysis for common mode loop and closed loop of the fully differential opamp. For CMFB loop, usually there have two places can break the loop, which are differential input sensing nodes or single-ended control node at the output of the error amplify. For differential nodes, we use cmdmprobe and set CMDM=1, for single-ended node, we simply use iprobe. One thing worth to mention is that, if probe is placed between two high impedance nodes, results obtained by using cmdmprobe and iprobe are all the same (eg. Loop 1). While, for loop 2, the output of the error amplifier is not a high impedance node, so that it's not correct to use iprobe (indicated in Fig 4) for the second stage CMFB stability analysis.

Differential mode and common mode transient responses are checked in the end.

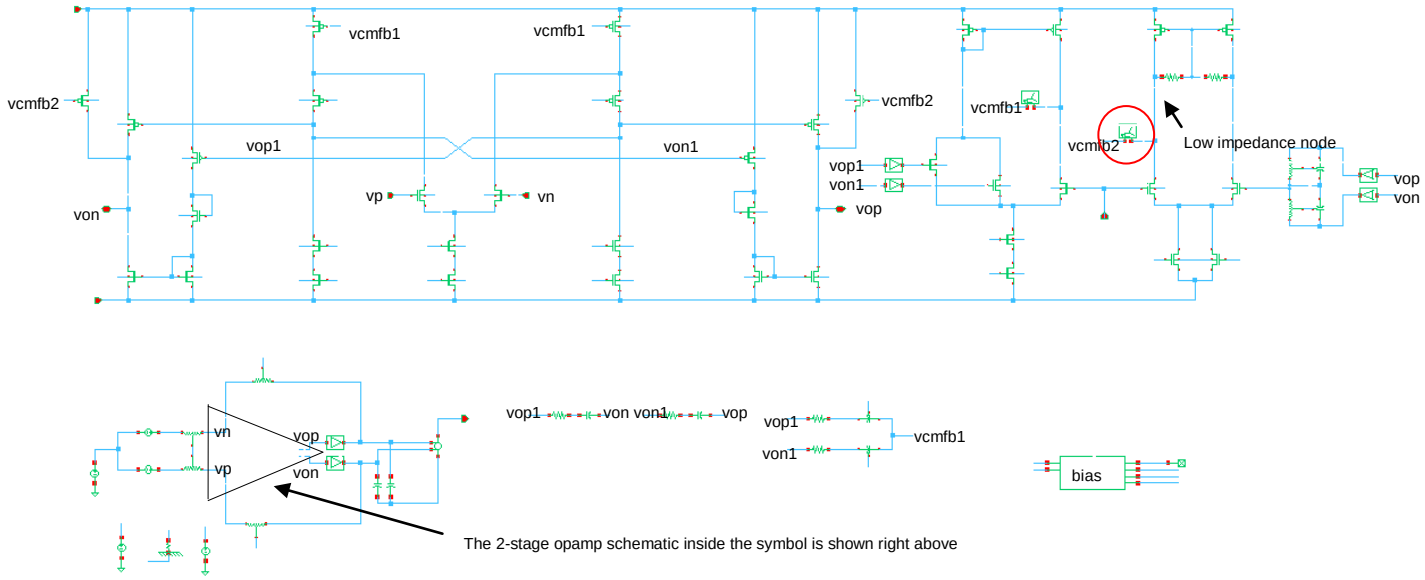


Figure 4 Closed loop stability analysis test bench.

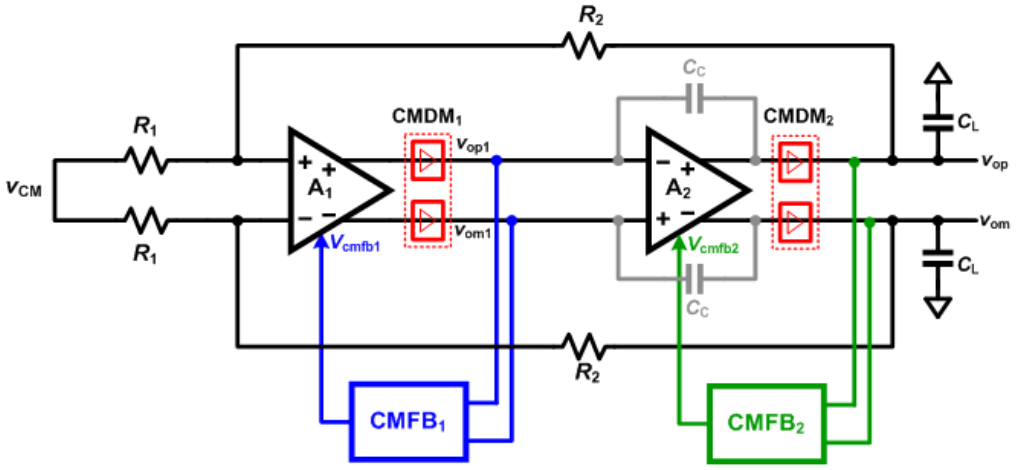


Figure 5 Closed loop stb analysis test bench using cmdmprobe method 1.

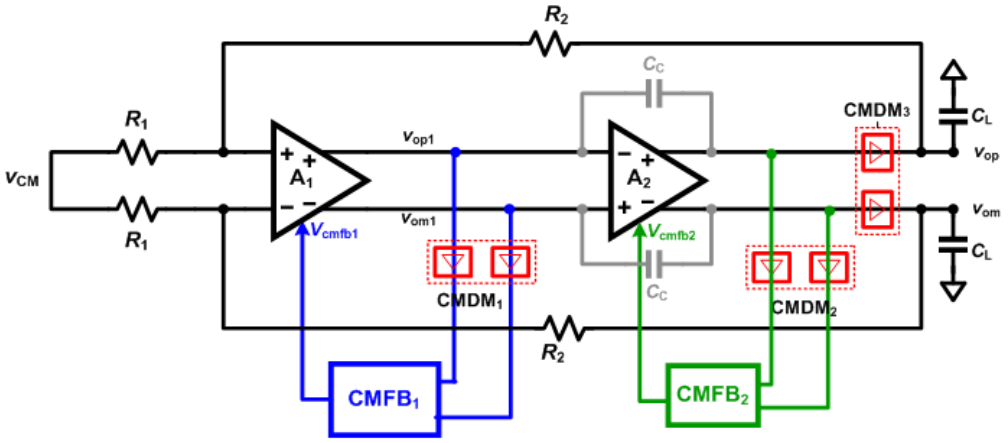


Figure 6 Closed loop stb analysis test bench using cmdmprobe method 2

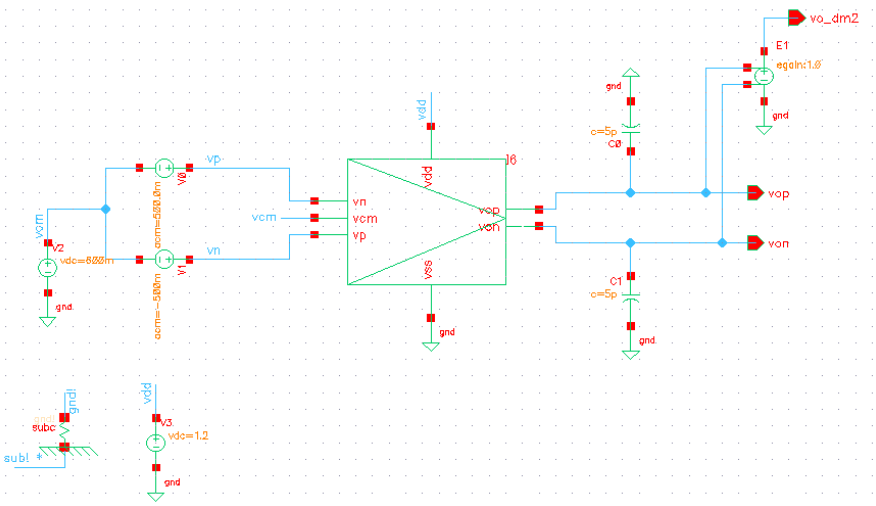


Figure 7 Differential open loop AC simulation test bench.

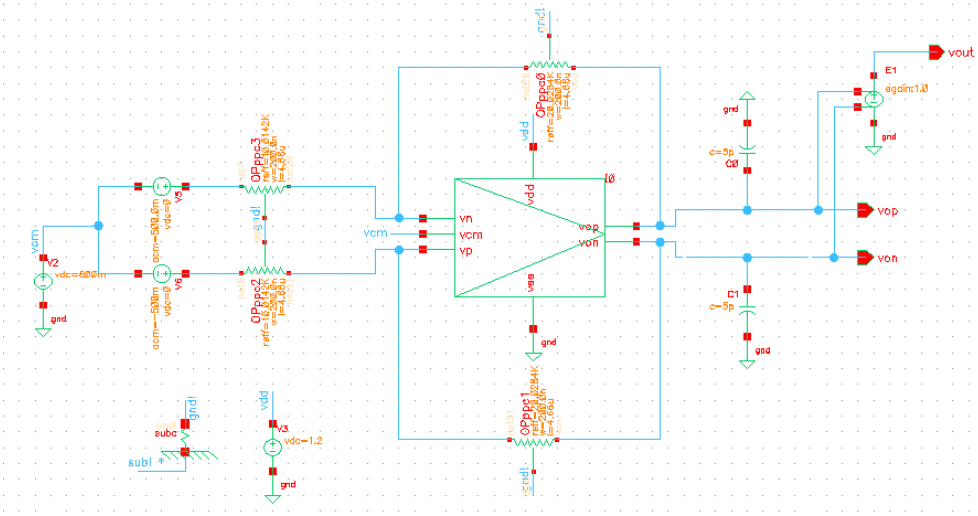


Figure 8 Differential closed loop AC simulation test bench.

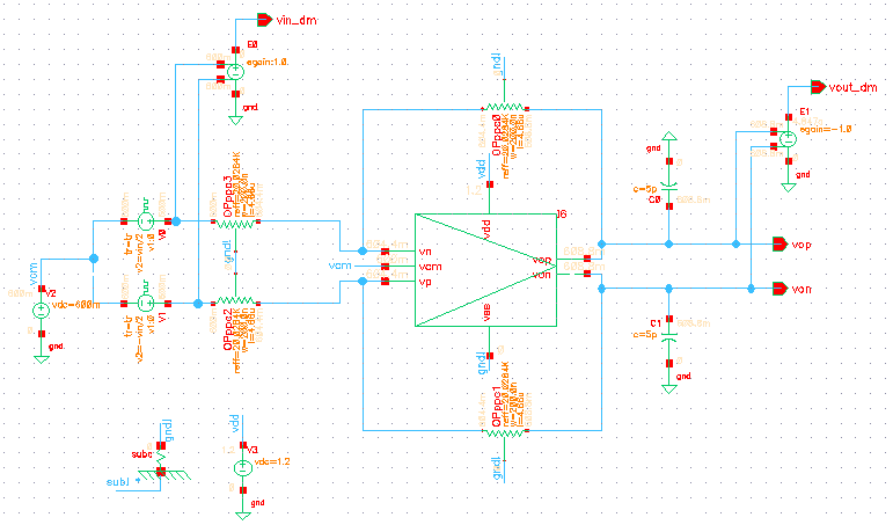


Figure 9 Unity-gain inverter transient simulation test bench for differential mode step response.

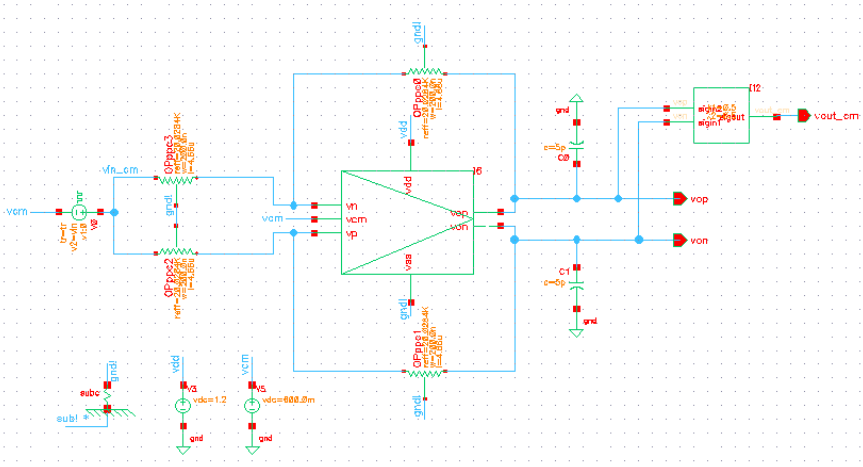


Figure 10 Unity-gain inverter transient simulation test bench for common mode step response.

1.3 Simulation Results and Summary

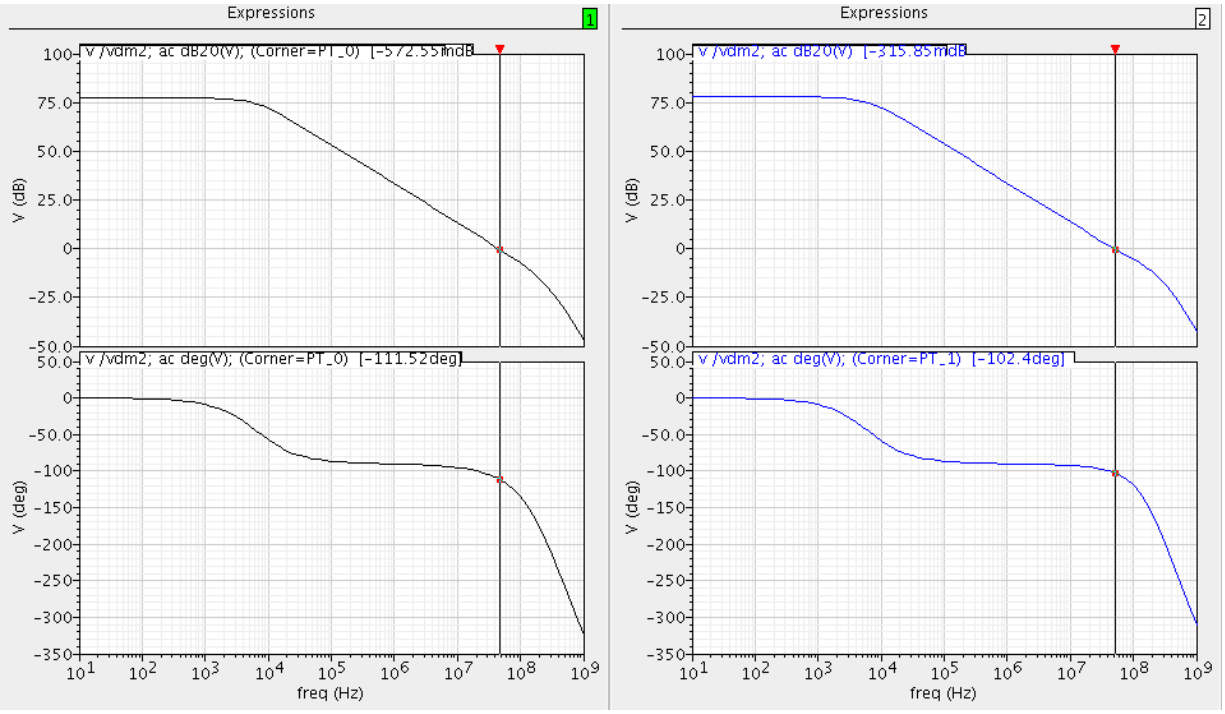
Simulation results are obtained with the test benches described above. First, by using DC and AC simulation to check the DC node voltages and open loop opamp specifications. In resistive feedback AC simulation, as shown in Fig11, the calculator expression seems not match the bode plot.

Then, closed loop stability analysis is followed to ensure the three feedback loops in the system are stable. Last, transient simulation is performed to see the differential and common mode responses.

In conclusion, all simulation under 40ºC, 1.2V power supply, ssf and tt corner, the open loop DC gain is higher than 70dB. Table 1 summarized and compared the aforementioned three loops by using cmdmprobe and iprobe stb analysis. It shows that for CMFB loop 2, iprobe is not accurate due to low impedance node, its PM got from cmdmprobe seems too large and it should be improved later on .

DC current consumption of the fully differential opamp at ssf and tt corner is 1.35mA and 1.86mA, respectively, all at 1.2V power supply and 40ºC.

1.3.1 Open loop AC simulation

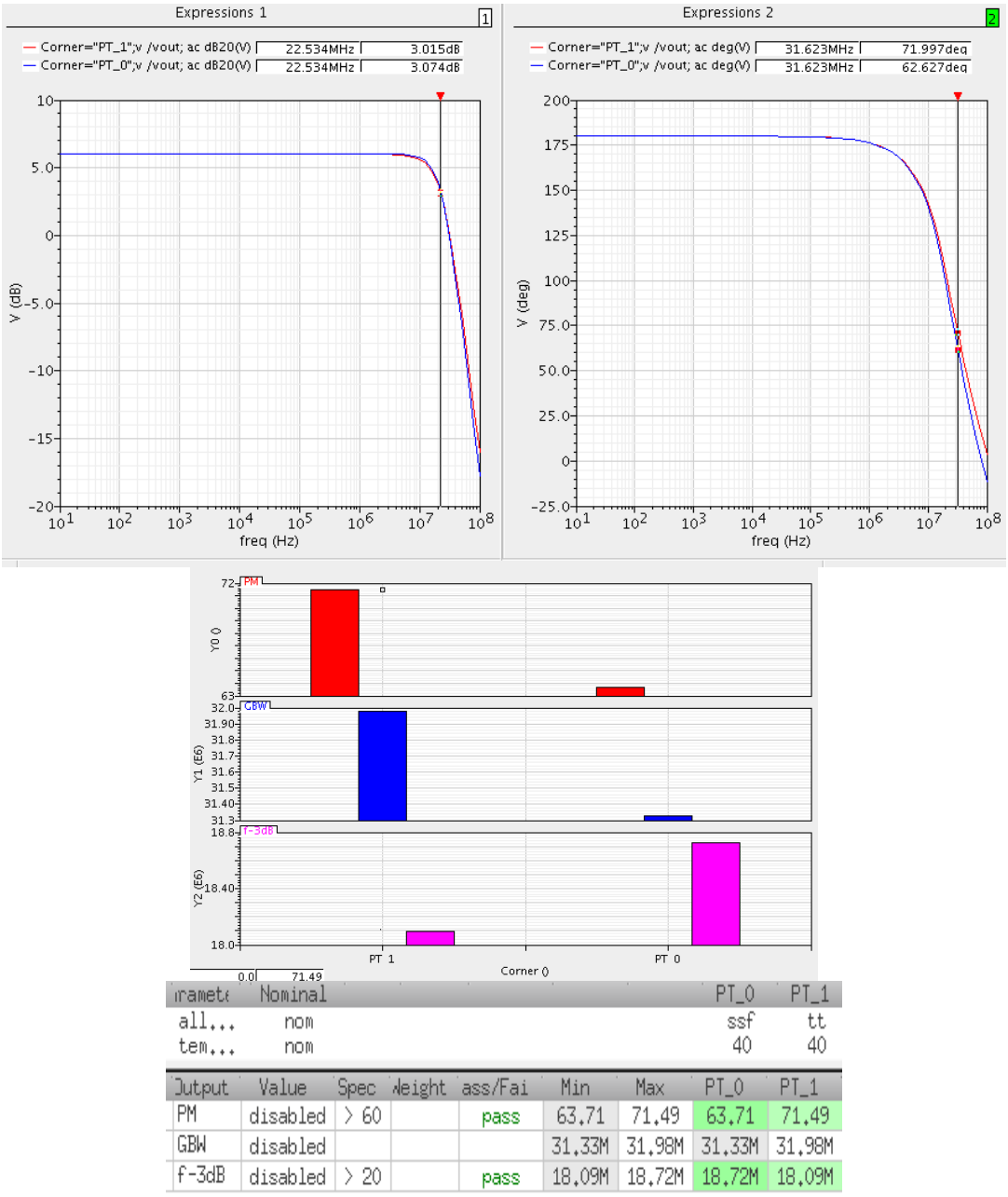


Parameter	Nominal	PT_0	PT_1
allModels.scs	nom	ssf	tt
temperature	nom	40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
v /vdm2: ac dB20(V)	disabled							
v /vdm2: ac deg(V)	disabled							
phasemargin	disabled	> 60		pass	69.82	78.24	69.82	78.24
Overall_Gain	disabled	> 70		pass	77.33	77.88	77.33	77.88
1st_stage_gain	disabled	> 50		pass	53.78	54.94	53.78	54.94
GBW	disabled				45.45M	49.79M	45.45M	49.79M

Figure 11 Differential open loop bode plot.

1.3.2 Resistive Feedback AC simulation



ıramet	Nominal						PT_0	PT_1
all...	nom						ssf	tt
tem...	nom						40	40

Jutput	Value	Spec	Weight	ass/Fai	Min	Max	PT_0	PT_1
PM	disabled	> 60		pass	63.71	71.49	63.71	71.49
GBW	disabled				31.33M	31.98M	31.33M	31.98M
f-3dB	disabled	> 20		pass	18.09M	18.72M	18.72M	18.09M

Figure 12 Close loop AC simulation bode plot and summary.

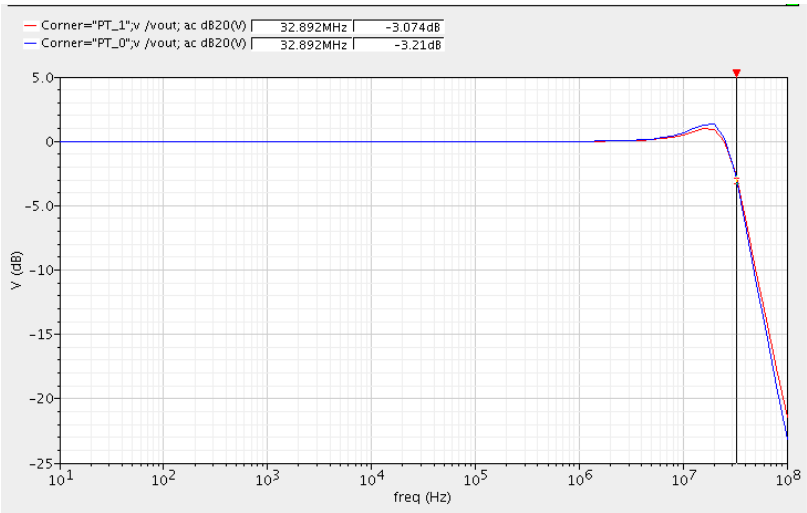


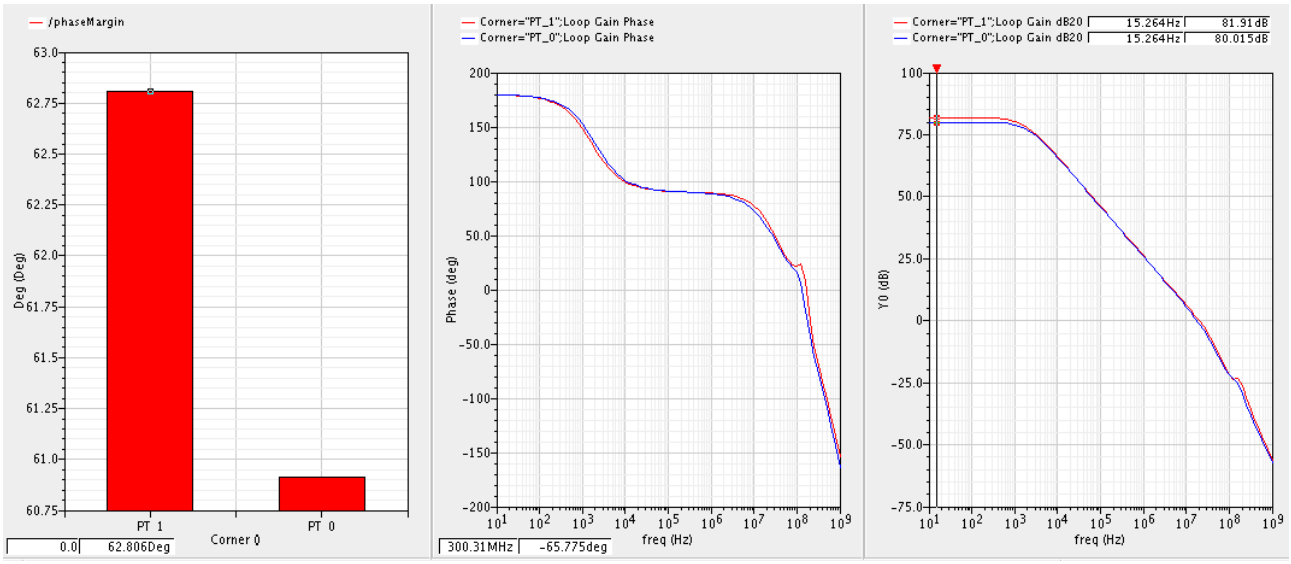
Figure 13 Close loop AC simulation magnitude plot when configured at unity-gain.

1.3.3 Fully Differential Opamp in feedback loop stability analysis

When analysis common mode loop stability, CMDM should be set as 1 in the cmdmprobe property.

For first stage CMFB loop, the results obtained by using cmdmprobe and iprobe match quite well (refer to Fig 14 and Fig 15).

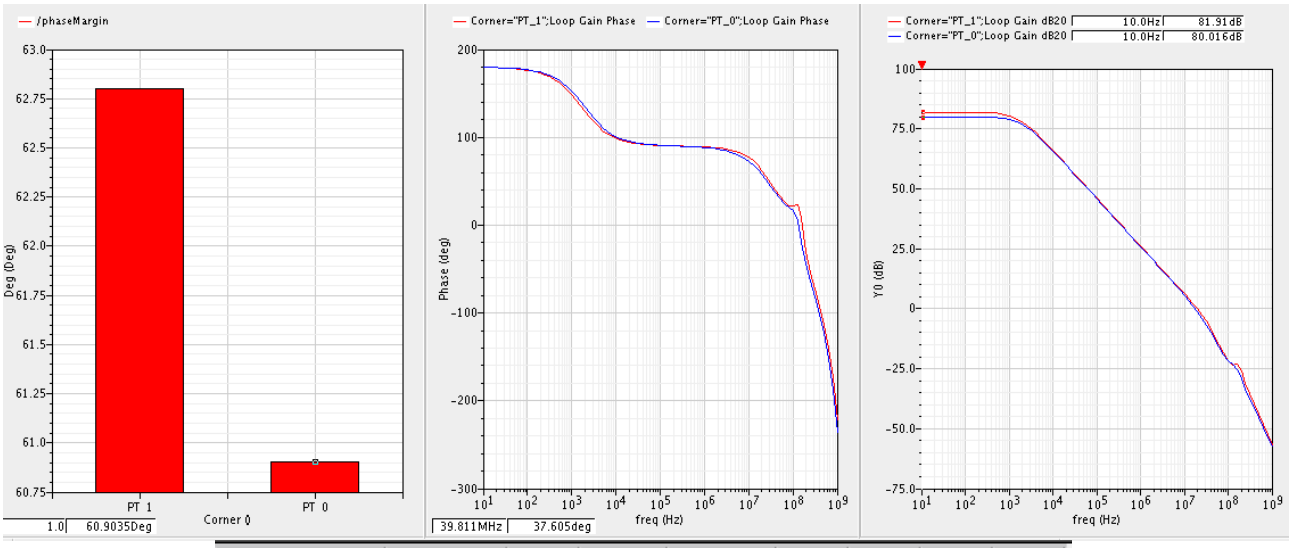
While, for the second stage CMFB loop, the results got by using different probes are different (see Fig.16 and Fig 17) due the low impedance node at output of the 2nd stage error amplifier as shown in Fig 4.



Parameter	Nominal						PT_0	PT_1
allModels.scs	nom						ssf	tt
temperature	nom						40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
Phase Margin	disabled	> 60		pass	60.91	62.81	60.91	62.81

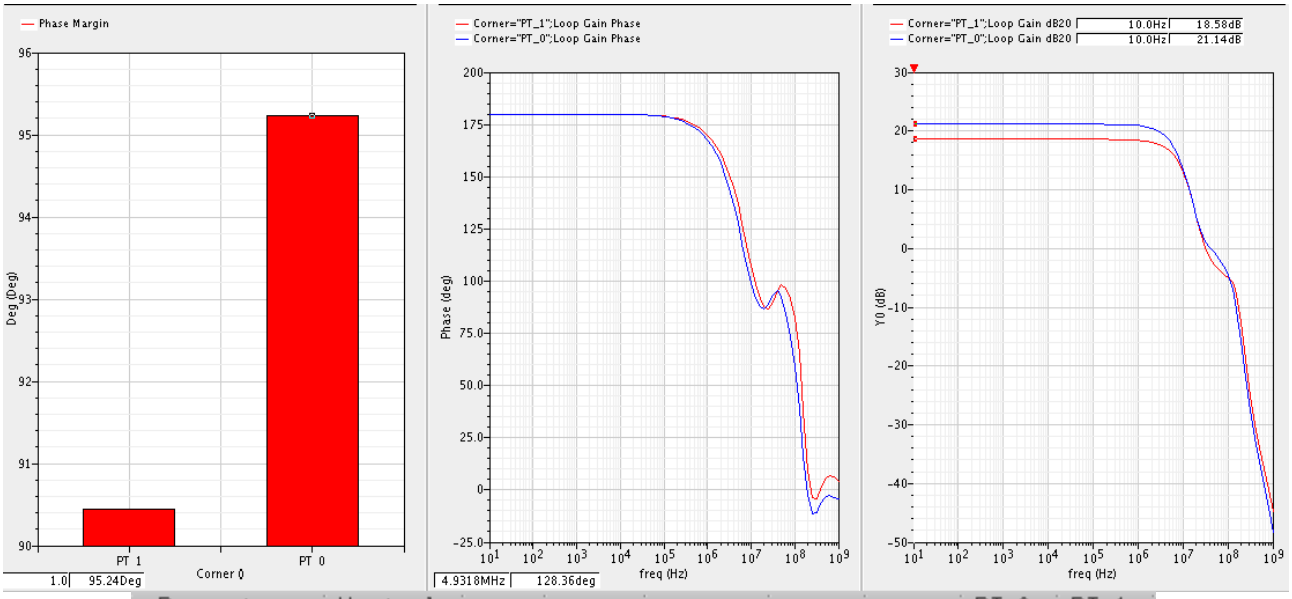
Figure 14 First stage CMFB stb analysis with cmdmprobe.



Parameter	Nominal						PT_0	PT_1
allModels.scs	nom						ssf	tt
temperature	nom						40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
Phase Margin	disabled	> 60		pass	60.9	62.8	60.9	62.8

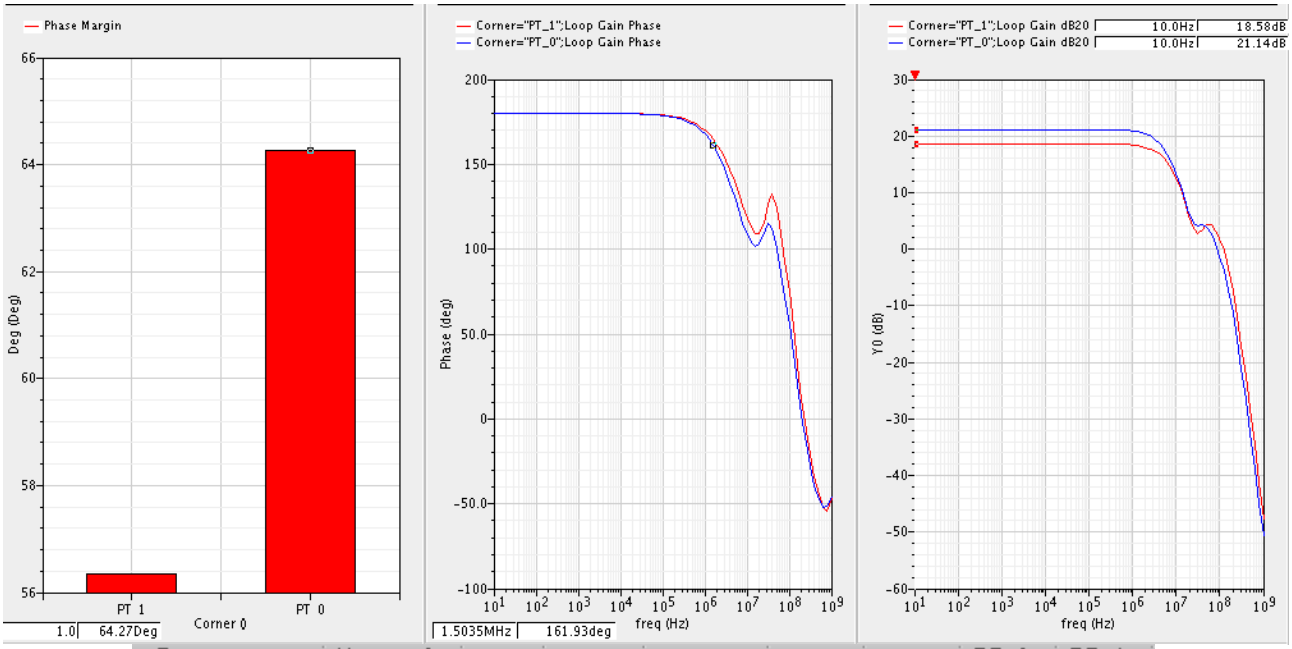
Figure 15 First stage CMFB stb analysis with iprobe.



Parameter	Nominal						PT_0	PT_1
allModels.scs	nom						ssf	tt
temperature	nom						40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
Phase Margin	disabled	> 60		pass	90.44	95.24	95.24	90.44

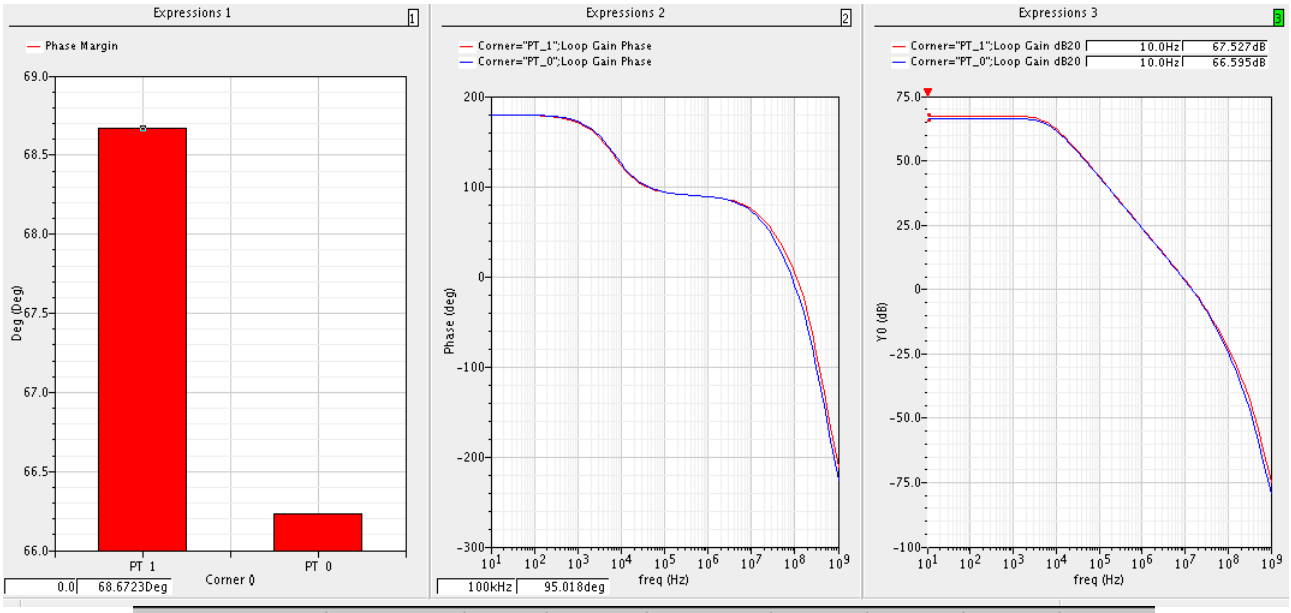
Figure 16 Second stage CMFB stb analysis with cmdmprobe.



Parameter	Nominal	PT_0	PT_1
allModels.scs	nom	ssf	tt
temperature	nom	40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
Phase Margin	disabled	> 60		near	56.34	64.27	64.27	56.34

Figure 17 Second stage CMFB stb analysis with iprobe.



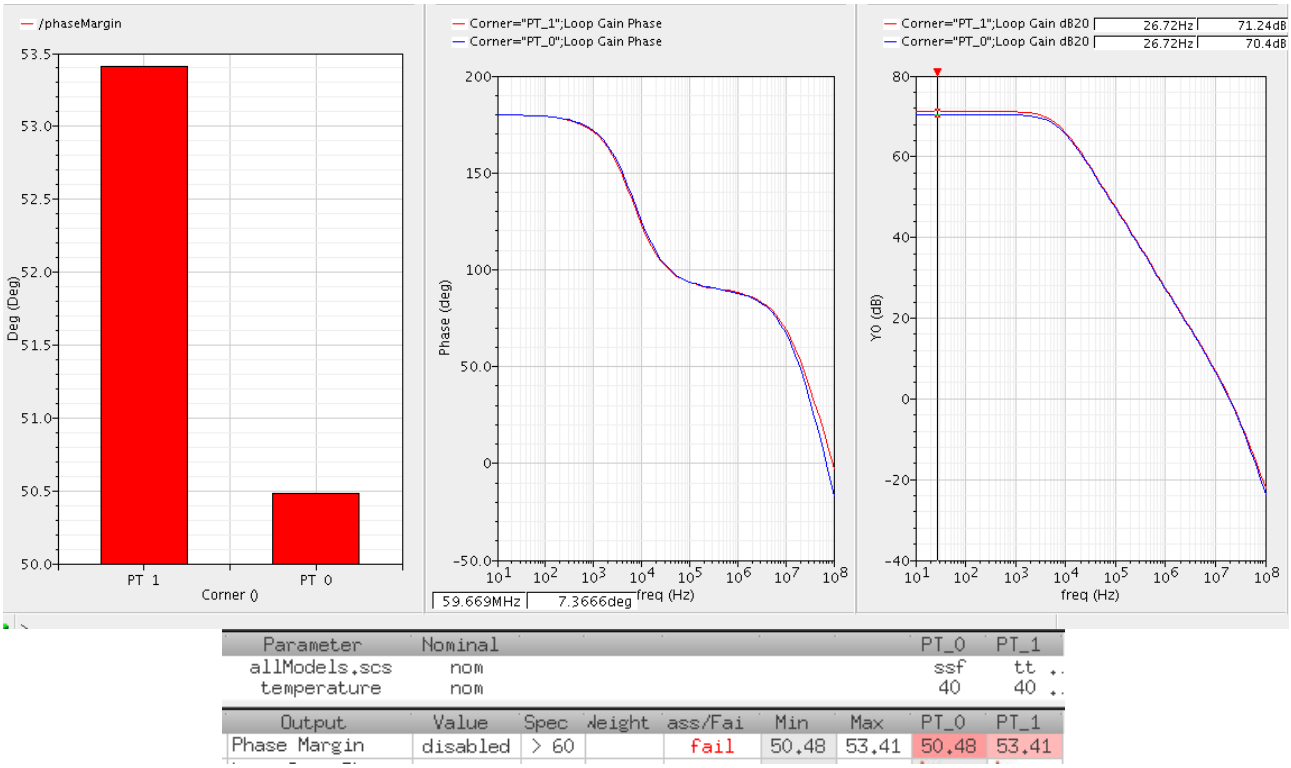
Parameter	Nominal	PT_0	PT_1
allModels.scs	nom	ssf	tt
temperature	nom	40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
Phase Margin	disabled	> 60		pass	66.23	68.67	66.23	68.67

Figure 18 Two-stage class AB closed loop stb analysis with cmdmprobe.

Table 1 Summary and comparison of stb analysis for the three feedback loops at tt corner.

Items	DC Gain (dB)	PM (º)	GBW (MHz)	stb options
1st stage CMFB	81.91	62.81	19.88	CMDM=1
	NA	NA	NA	CMDM=-1
	81.91	62.8	19.88	iprobe
2nd stage CMFB	18.58	90.44	32.08	CMDM=1
	NA	NA	NA	CMDM=-1
	18.58	56.34	123.2	Misused iprobe
Closed loop	-106.07	NA	NA	CMDM=1
	67.53	68.67	**14.87** (correct?)	CMDM=-1



Parameter	Nominal	PT_0	PT_1
allModels.scs	nom	ssf	tt
temperature	nom	40	40

Output	Value	Spec	Weight	Pass/Fail	Min	Max	PT_0	PT_1
Phase Margin	disabled	> 60		fail	50.48	53.41	50.48	53.41

When it configured as unity-gain feedback, the phase margin drops!

Figure 19 Closed loop bode plot configured as unity gain inverter using cmdmprobe stb analysis.

1.3.4 Differential/Common Mode Transient Response

Transient simulations are performed to test differential mode and common mode responses when the opamp is configured in unity gain with resistive feedback. 200mV differential pulse and 100mV common mode pulse with 0.1ns rise/fall times and 100ns pulse width are simulated, resulting waveforms are plotted in Fig 19 and Fig 20, respectively.

For differential mode response, as shown in Fig 19, there is a overshoot and undershoot about 40mV, and the slew rate is limited due to 5pF load. The under damping maybe caused by less phase margin when configured to unity-gain.

For common mode response, as shown in Fig 20, the common mode disturbance at the input is attenuated by more than 40dB at ssf corner.

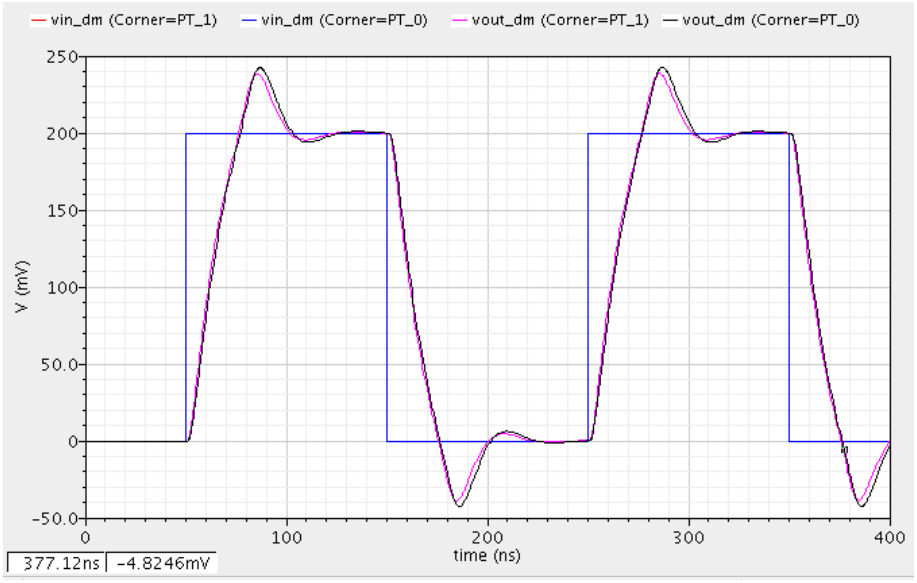


Figure 20 Unity- gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse with=100ns, in test bench set output VCVS gain=-1).

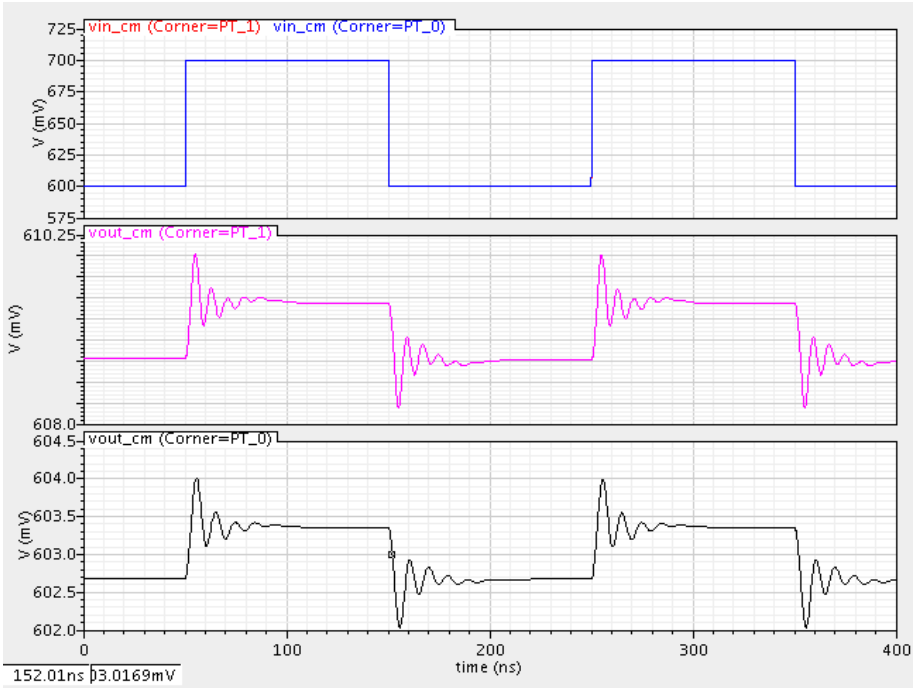


Figure 21 Unity- gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse with=100ns, in the test bench veriloga adder is used for averaging).

2 Paper Digest

For each of the example common-mode feedback loop designs shown in the CMFB Examples handout: Explain the operation of the CMFB loops in both the opamp stages, and comment on their relative advantages and disadvantages.

2.1 Paper 1[1]

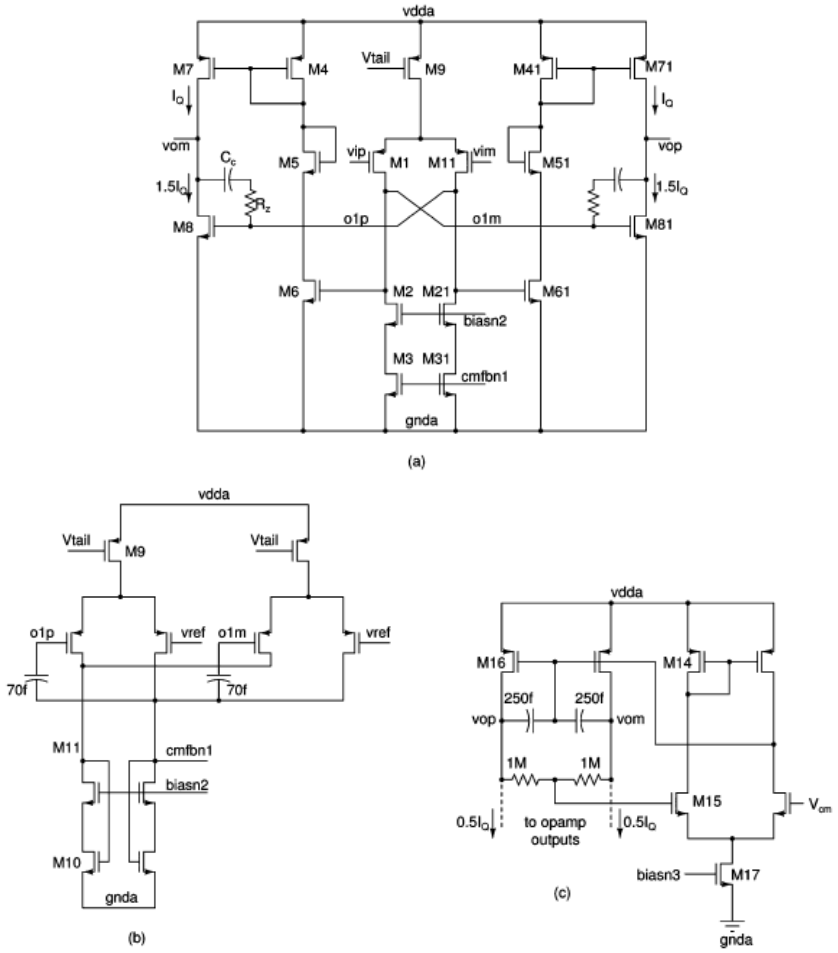


Figure 22 Operational amplifier used in the first integrator. (a) Main amplifier. (b) Common-mode feedback (CMFB) for the first stage. (c) Second-stage CMFB circuit.

Telescopic cascode opamp with class AB output stage.

1st-stage CMFB is dual diff-amp topology.

- Pros:
  Eliminating large resistors; less loading introduced to the main opamp; Common-mode detector and error amplifier as a one.
- Cons :
  Large signal swings will cause linearity issue.

2nd-stage CMFB is resistive averaging common-mode detector with output voltage from error amplifier to control the current of common-source PMOS injecting to the fully differential outputs.

- Pros:
  Resistive detector can sense large signal swings to alleviate linearity issue to the

error amplifier; clever way to use current to adjust the output common-mode level so that each stage can do CMFB separately.

- Cons :

  Resistors should be large enough that will occupy considerable silicon areas; the gate(biasn3) of NMOS current source of the error amplifier is not a replica of the second-stage quiescent current so that current densities may not be well matched and systematic offset will be introduced in the CMFB loop.

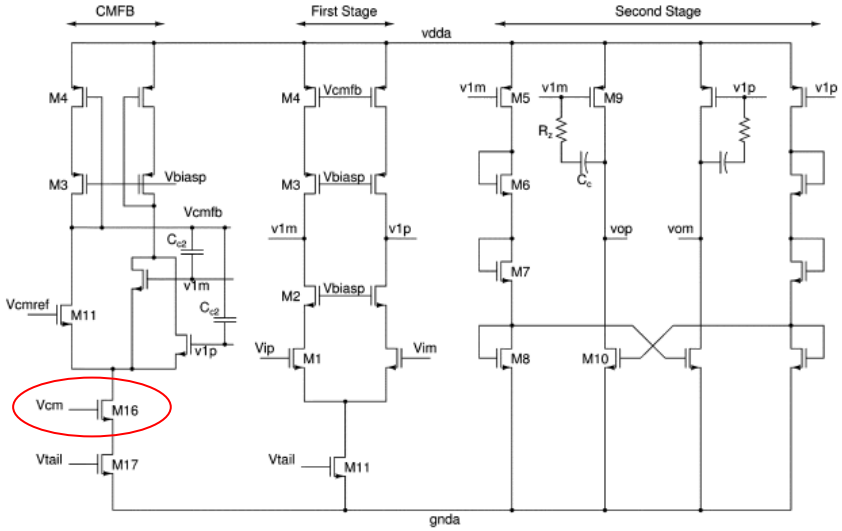


Figure 23 Schematic of the operational amplifier used in the second and third integrators and the summing amplifier.

NMOS input version, second stage CMFB is similar with the previous one. Two diode-connected NMOS transistors (M6 and M7) are stacked to increase the drain voltage at M5, make it better matches with the quiescent current in the second stage CMFB error amplifier. One potential problem is that the first stage CMFB is not an exactly replica of the first stage of the main opamp which may cause systematic offset for the CMFB loop of the first stage.

2.2 Paper 2[2]

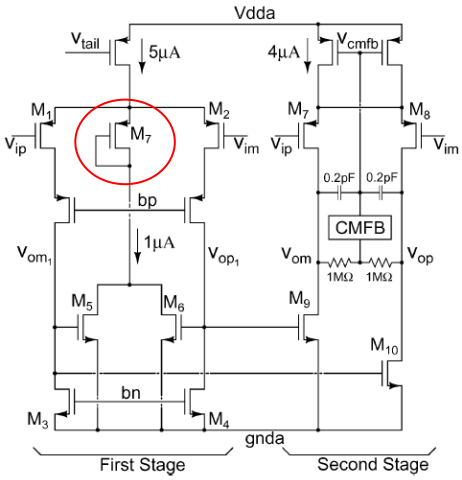


Figure 24 Operational amplifier used in the first integrator in paper 2.

Feedforward compensation with clever first stage CMFB, it uses transistors (M5 and M6) to detect common-mode voltage and sources a portion of current from the tail current of the first stage main opamp. $M_{5,6}$ are replicas of $M_{9.10}$ and operate in saturation region. Since the

gate voltages of $M_{9.10}$ and $M_{5,6}$ are the same. In order to let $M_{9.10}$ and $M_{5,6}$ have the same V_{DS}, diode-connected transistor M7 (indicate in red circle) is inserted to match the M7 in the second stage.

- Pros:
  Very compact CMFB scheme for the first stage; second stage current is reused for feedforward compensation which achieves higher unity gain frequency than miller compensation for a given power.
- Cons :
  The first stage common-mode level may not be well defined since there is no reference voltage to be compared in the feedback loop; the feedforward transistors $M_{7.8}$ connected between input and output nodes which restricts the differential peak-to-peak output swing to four time the threshold voltage.

2.3 Paper 3[3]

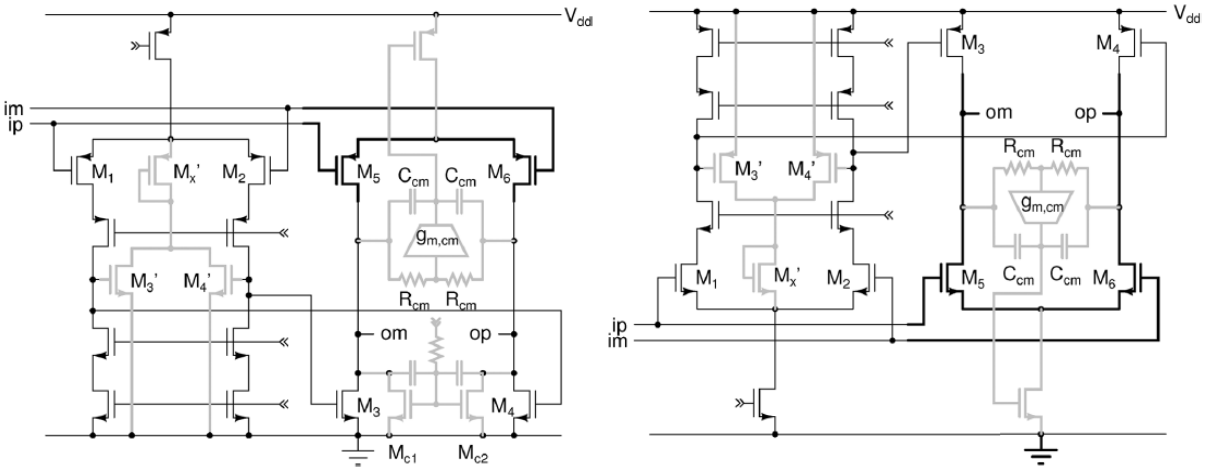


Figure 25 Feedforward compensated opamp used in the paper 3. Feedforward path is shown in bold, and CMFB paths are shown in gray.

This is basically the same topology as proposed in paper 2. For the left one, transistors $M_{c1.c2}$ are augmented act as a low-impedance nodes for high frequencies.

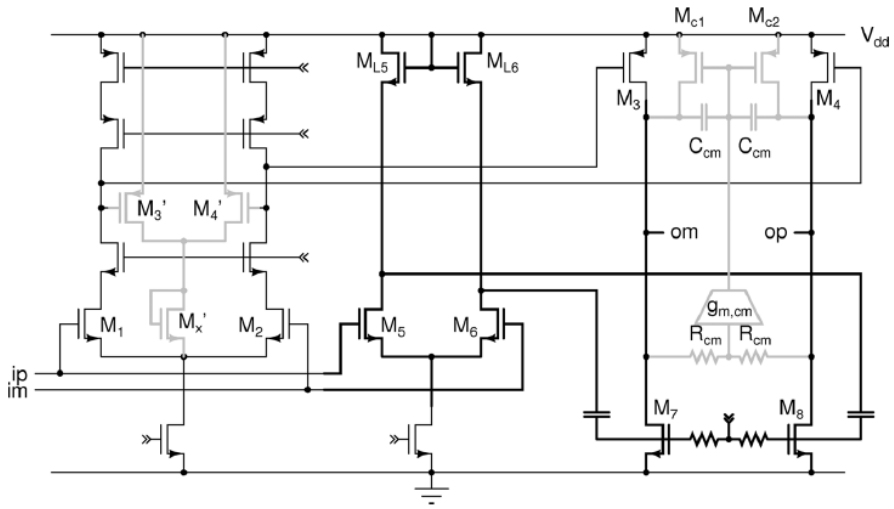


Figure 26 Feedforward compensated opamp used in the summing amplifier. Feedforward path is shown in bold, and CMFB paths are shown in gray.

The feedforward stage is modified to have two stages, a low gain high speed stage $M_{5,6}$ followed by common source amplifiers $M_{7,8}$, in order to support high output swing. The latter permits a high output swing while the former provides common mode rejection.

2.4 Paper 4[4]

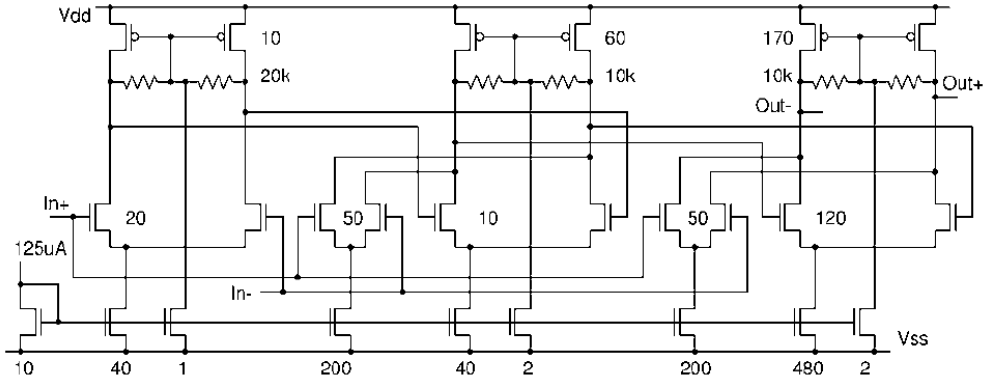


Figure 27 Feedforward opamp schematic, including common-mode feedback.

This is a three-stage fully differential opamp with two feedforward stages for compensation. A small current is injected into each common-mode feedback summing node to raise the common-mode level at extreme cases.

- Pros:
  Simple local common-mode feedbacks save power.
- Cons :
  No flexibility to set the output common mode; small resistors lower the gain while large resistors occupy area; feedforward amplifier burns more power than the first stage opamp.

2.5 CMFB Using Triode Devices[5]

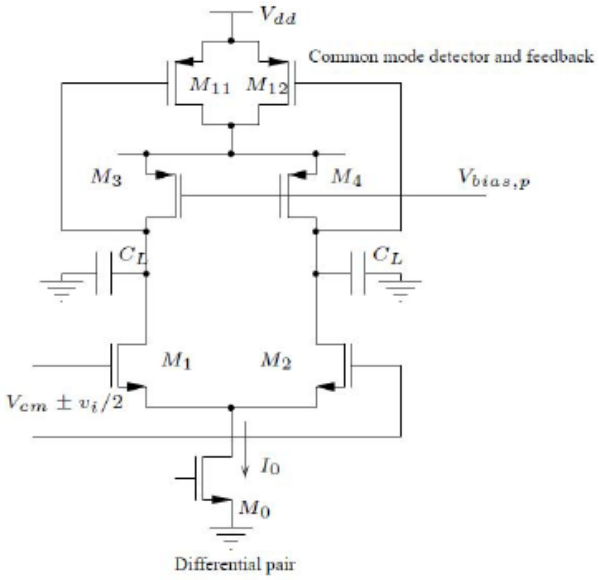


Figure 28 CMFB using triode devices.

This simple feedback Resistance looking at the drain of the common mode detector

transistors is

$$R_S = R_{o11}||R_{o12} = \frac{1}{KP_p\frac{W}{L}_{11,12}(V_{op}+V_{on}-2V_{TH})}$$

Also $R_{o11}||R_{o12} = \frac{V_{dd}-V_{bias,p}-V_{SG3,4}}{2I_0}$

$$V_{ocm} = \frac{V_{on}+V_{op}}{2} = \frac{I_0}{KP_p\frac{W}{L}_{11,12}(V_{dd}-V_{bias,p}-V_{SG3,4})} + V_{TH}$$

The sensed output voltage is PVT dependent. In order to be in triode region, the sense transistors should be large size that directly load the output. The output swing is also limited.

3 Simulation Supplement

Loop stability was simulated again in unity feedback configuration by placing cmdmprobes at different locations in the opamp. Some compensation parameters and second stage CMFB are changed. By placing cmdmprobes properly, results obtained from both methods are highly matched.

Transient responses are also re-simulated, for details refer to Vishal's Loop Stability slides.

3.1 Method 1

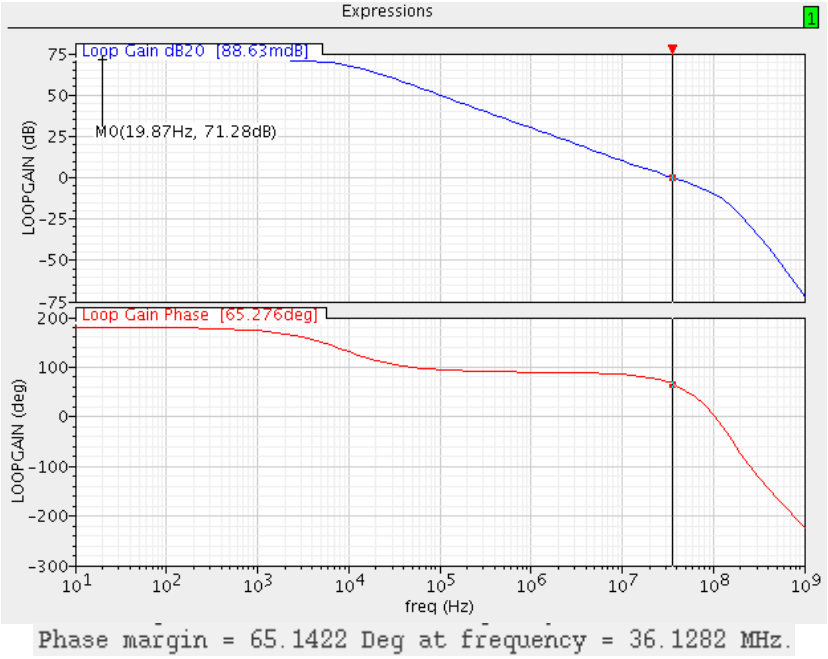


Figure 29 DM loop Method 1 and 2 the same.

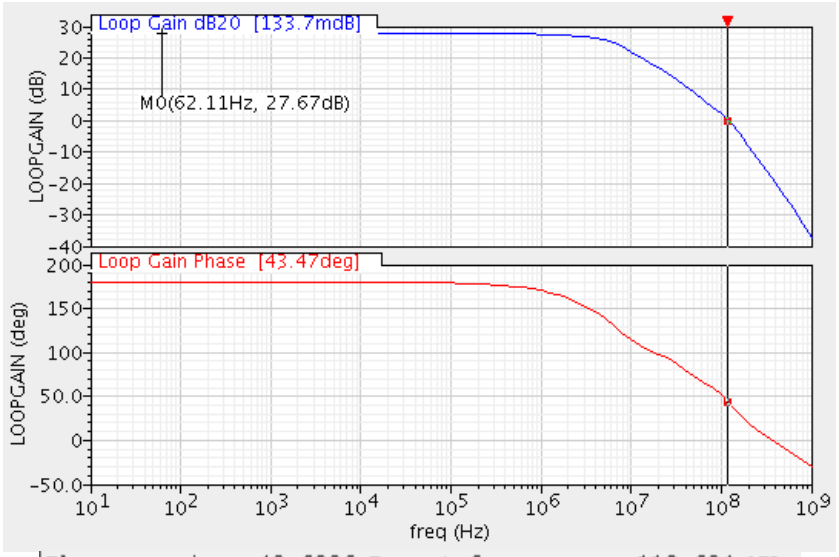


Figure 30 2nd stage CMFB Method 1.

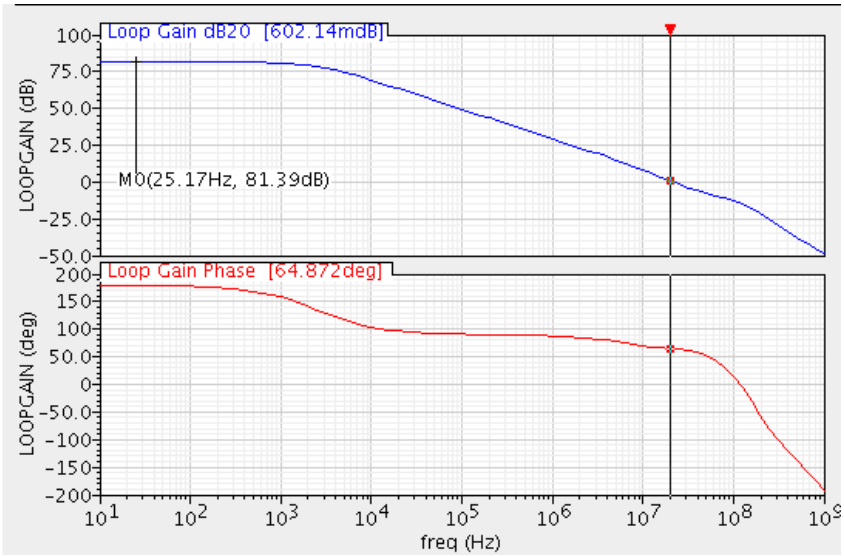


Figure 31 1st stage CMFB Method 1.

3.2 Method 2

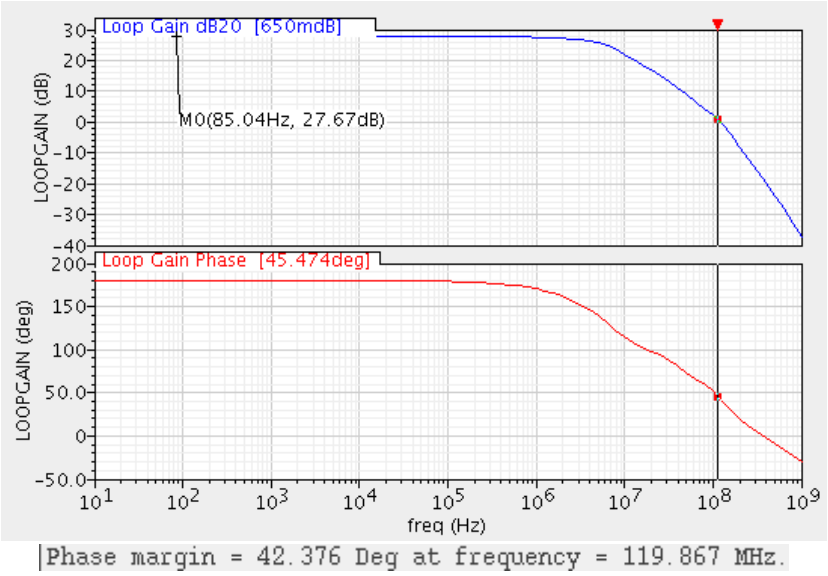


Figure 32 2nd stage CMFB Method 2.

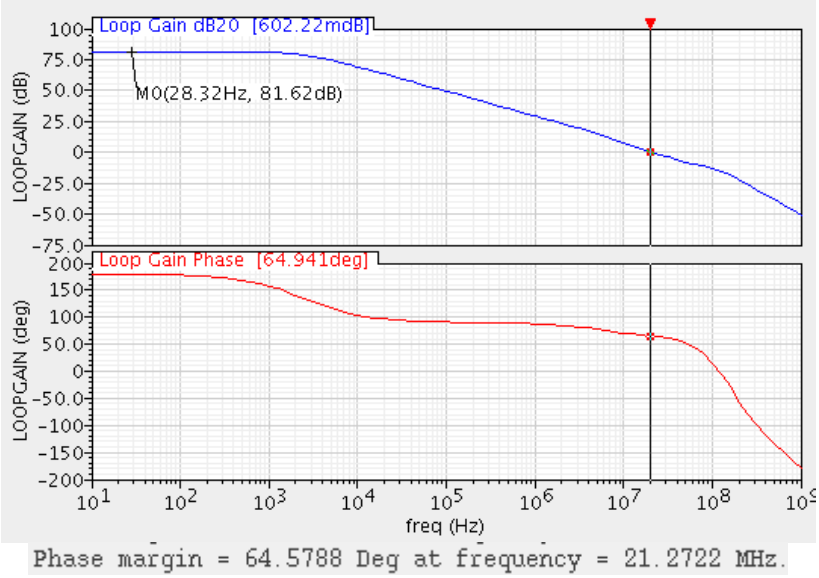


Figure 33 1st stage CMFB Method 2.

4 References

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2. Pavan, S. and P. Sankar, *Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique.* Solid-State Circuits, IEEE Journal of. **45**(7): p. 1365-1379.
3. Singh, V., et al., *A 16 MHz BW 75 dB DR CT Delta Sigma ADC Compensated for More Than One Cycle Excess Loop Delay.* Solid-State Circuits, IEEE Journal of. **47**(8): p. 1884-1895.
4. Harrison, J. and N. Weste. *A 500 MHz CMOS anti-alias filter using feed-forward op-amps with local common-mode feedback*. in *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*. 2003.
5. Razavi, B., *Design of Analog CMOS Integrated Circuits*.