Homework 1

ECE 614 – CMOS Analog IC Design

Due on Tuesday, Sep 18, 2012

Note: Use the provided 130n CMOS process with $V_{DD} = 1.2\,V$ for all the problems. Clearly show your neatly drawn schematics with transistor types and sizes. Present your calculations and result plots with proper labels and annotation.

Problem 1: A two-stage fully-differential Opamp needs to be designed to realize an amplifier of gain 2 and a closed-loop -3 dB bandwidth of $f_b = 20$ MHz driving a $C_L = 5\,pF$ load with rail-to-rail output swings. The open-loop DC gain of the opamp should be greater than $A_{OL} = 70\,dB$. The Use $R_1 = 10\,k\Omega$. Assume that the common mode reference voltage $V_{CM} = \frac{V_{DD}}{2} = 0.6V$ is available from a bandgap reference (BGR). Use zero canceling resistors in series with the Miller compensation capacitors.

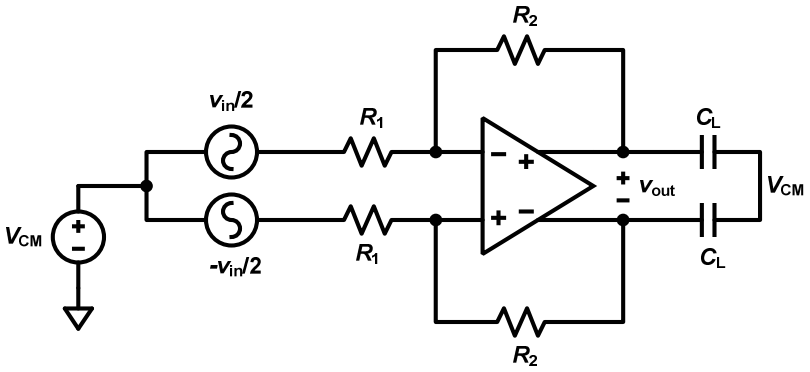

Figure 1: Fully-differential opamp in feedback configuration.

Select the appropriate topologies for the first and second stage amplifiers and individual common mode feedback (CMFB) loops. Ensure that there is no systematic offset in your CMFB loops. Compensate all the three feedback loops for a phase margin of 60°.

Clearly show/tabulate all the transistor sizes and the component values. Use STB analysis for all loops by appropriately placing the CMDM probe. Show all relevant testbench shematics. Show results for at least **tt** and **ssf** corners.

(a) Briefly discuss you design choices with relevant calculations and plots. Draw the differential half circuit for the opamp and the common mode equivalent circuits for both the CMFB loops.

(b) Plot the following results:

1. Differential open loop gain-magnitude and phase. Indicate the phase margin.
2. Differential closed loop gain-magnitude and phase. Indicate the -3 dB bandwidth.
3. First stage common-mode loop gain-magnitude and phase. Indicate the phase margin.
4. Second stage common-mode loop gain-magnitude and phase. Indicate the phase margin.
5. Transient response of the unity-gain inverting amplifier with a 200 mV differential step (use 0.1 ns rise/fall times)
6. Transient response of the unity-gain inverting amplifier with a 100 mV common mode step (use 0.1 ns rise/fall times)

Problem 2: For each of the example common-mode feedback loop designs shown in the *CMFB Examples* handout: Explain the operation of the CMFB loops in both the opamp stages (can use hand-sketches), and comment on their relative advantages and disadvantages. Bookmark these discussions for your design projects.