

# Pipelined Analog to Digital Converters

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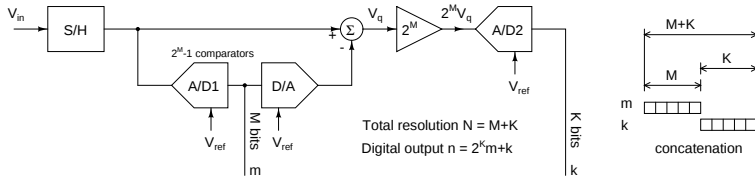
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# Motivation for multi step A/D conversion

- Flash converters:
  - Area and power consumption increase exponentially with number of bits  $N$
  - Impractical beyond 7-8 bits.
- Multi step conversion-Coarse conversion followed by fine conversion
  - Multi-step converters
  - Subranging converters
- Multi step conversion takes more time
  - Pipelining to increase sampling rate

# Two step A/D converter-basic operation

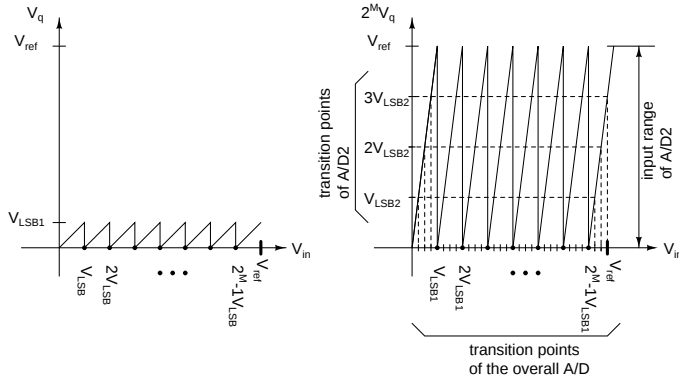


- Second A/D quantizes the quantization error of first A/D
- Concatenate the bits from the two A/D converters to form the final output

# Two step A/D converter-basic operation

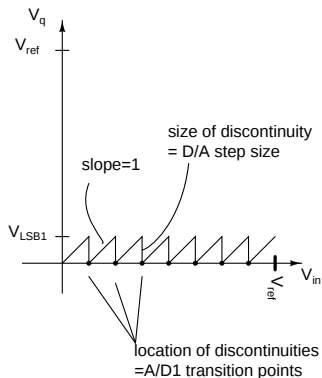
- A/D1, DAC, and A/D2 have the same range  $V_{ref}$
- Second A/D quantizes the quantization error of first A/D
  - Use a DAC and subtractor to determine residue  $V_q$
  - Amplify  $V_q$  to full range of the second A/D
- Final output  $n$  from  $m, k$ 
  - A/D1 output is  $m$  (DAC output is  $m/2^M V_{ref}$ )
  - A/D2 input is at  $k^{th}$  transition ( $k/2^K V_{ref}$ )
  - $V_{in} = k/2^K V_{ref} \times 1/2^M + m/2^M V_{ref}$
  - $V_{in} = (2^K m + k)/2^{M+K} V_{ref}$
- Resolution  $N = M + K$ , output  $\Rightarrow n = 2^K m + k \Rightarrow$   
Concatenate the bits from the two A/D converters to form the final output

# Two step A/D converter: Example with $M = 3$ , $K = 2$



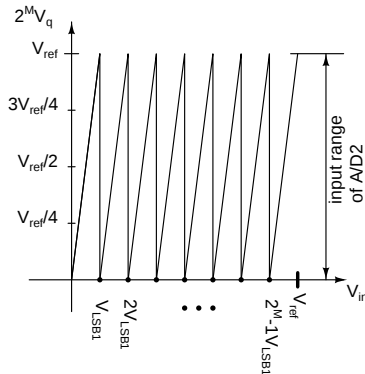
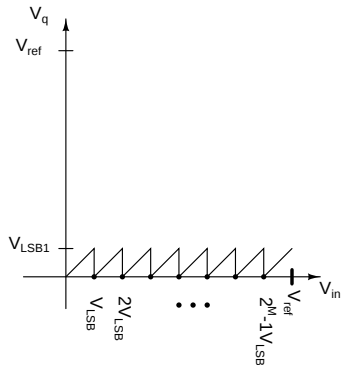
- Second A/D quantizes the quantization error of first A/D
- Transitions of second A/D lie between transitions of the first, creating finely spaced transition points for the overall A/D.

# Residue $V_q$



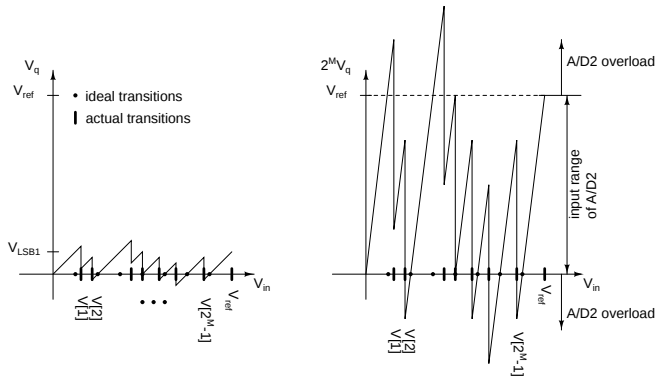
- $V_q$  vs.  $V_{in}$ : Discontinuous transfer curve
  - Location of discontinuities: Transition points of A/D1
  - Size of discontinuities: Step size of D/A
  - Slope: unity

# Two step A/D converter—ideal A/D1



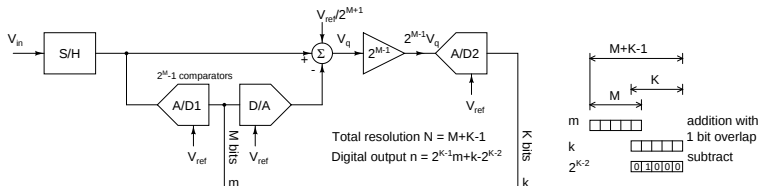
- A/D1 transitions exactly at integer multiples of  $V_{ref}/2^M$
- Quantization error  $V_q$  limited to  $(0, V_{ref}/2^M)$
- $2^M V_q$  exactly fits the range of A/D2

# Two step A/D converter—M bit accurate A/D1



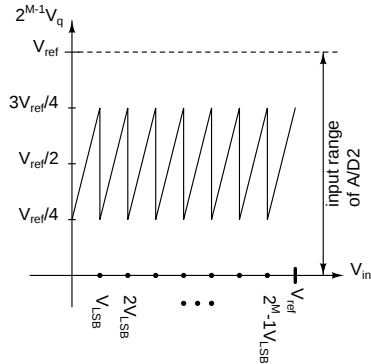
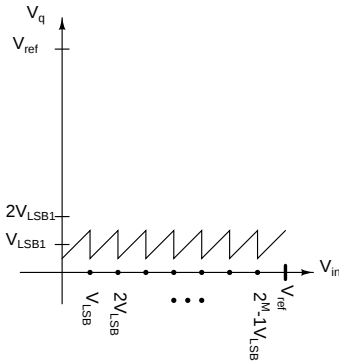
- A/D1 transitions in error by up to  $V_{ref}/2^{M+1}$
- Quantization error  $V_q$  limited to  $(-V_{ref}/2^{M+1}, 3V_{ref}/2^{M+1})$ —a range of  $V_{ref}/2^{M-1}$
- $2^M V_q$  overloads A/D2

# Two step A/D with digital error correction (I)



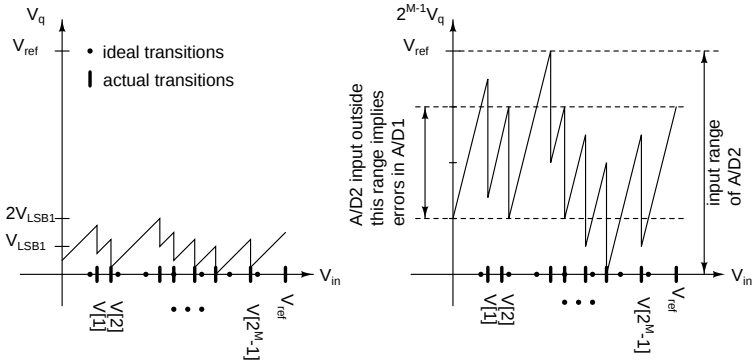
- Reduce interstage gain to  $2^{M-1}$
- Add  $V_{ref}/2^{M+1}$  (0.5 LSB1) offset to keep  $V_q$  positive
- Subtract  $2^{K-2}$  from digital output to compensate for the added offset
- Overall accuracy is  $N = M + K - 1$  bits; A/D1 contributes  $M - 1$  bits, A/D2 contributes  $K$  bits; 1 bit redundancy
- Output  $n = 2^{K-1}m + k - 2^{K-2}$

# Two step A/D with digital error correction (I)—Ideal A/D1



- $2^{M-1}V_q$  varies from  $V_{ref}/4$  to  $3V_{ref}/4$
- $2^{M-1}V_q$  outside this range implies errors in A/D1

# Two step A/D with digital error correction (I)—M bit accurate A/D1

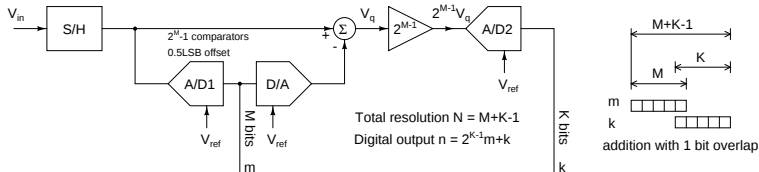


- $2^{M-1}V_q$  varies from 0 to  $V_{ref}$
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1

# Two step A/D with digital error correction (I)—M bit accurate A/D1

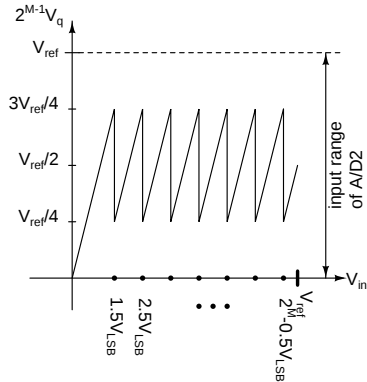
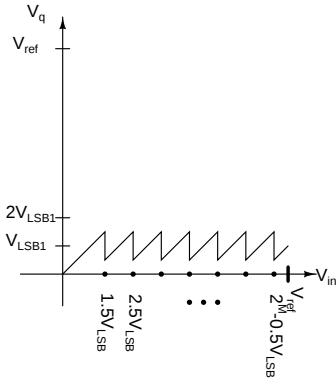
- A/D1 Transition shifted to the left
  - $m$  greater than its ideal value by 1
  - $k$  lesser than its ideal value by  $2^{K-1}$
  - A/D output  $n = 2^{K-1}m + k - 2^{K-2}$  doesn't change
- A/D1 Transition shifted to the right
  - $m$  lesser than its ideal value by 1
  - $k$  greater than its ideal value by  $2^{K-1}$
  - A/D output  $n = 2^{K-1}m + k - 2^{K-2}$  doesn't change
- 1 LSB error in  $m$  can be corrected

# Two step A/D with digital error correction (II)



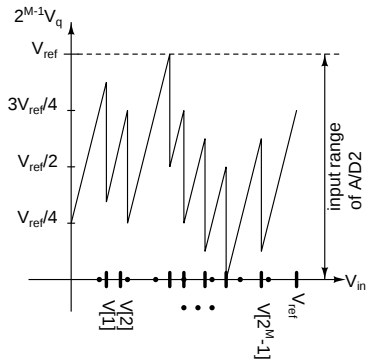
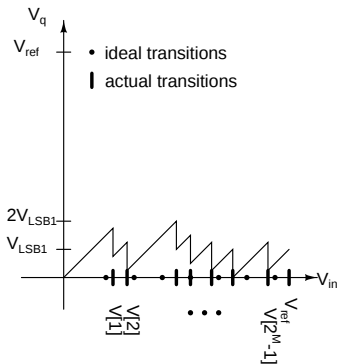
- Reduce interstage gain to  $2^{M-1}$
- Shift the transitions of A/D1 to the right by  $V_{ref}/2^{M+1}$  (0.5 LSB) to keep  $V_q$  positive
- Overall accuracy is  $N = M + K - 1$  bits; A/D1 contributes  $M - 1$  bits, A/D2 contributes  $K$  bits; 1 bit redundancy
- Output  $n = 2^{K-1}m + k$ , no digital subtraction required  
*Rightarrow* simpler digital logic

# Two step A/D with digital error correction (II)—Ideal A/D1



- $2^{M-1}V_q$  varies from 0 to  $3V_{ref}/4$ ;  $V_{ref}/4$  to  $3V_{ref}/4$  except the first segment
- $2^{M-1}V_q$  outside this range implies errors in A/D1

# Two step A/D with digital error correction (II)—M bit accurate A/D1



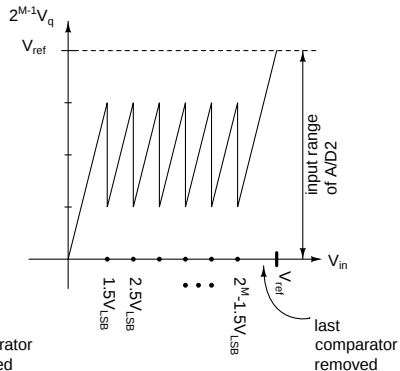
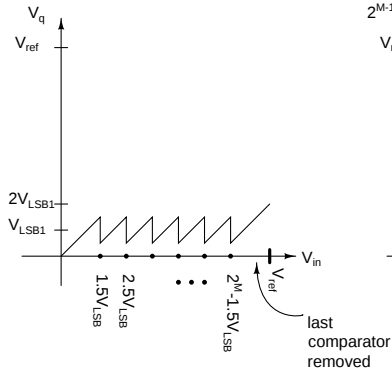
- $2^{M-1}V_q$  varies from 0 to  $V_{ref}$
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1

# Two step A/D with digital error correction (II)—M bit accurate A/D1

- A/D1 Transition shifted to the left
  - $m$  greater than its ideal value by 1
  - $k$  lesser than its ideal value by  $2^{K-1}$
  - A/D output  $n = 2^{K-1}m + k$  doesn't change
- A/D1 Transition shifted to the right
  - $m$  lesser than its ideal value by 1
  - $k$  greater than its ideal value by  $2^{K-1}$
  - A/D output  $n = 2^{K-1}m + k$  doesn't change
- 1 LSB error in  $m$  can be corrected

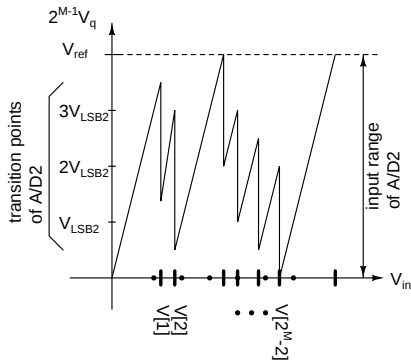
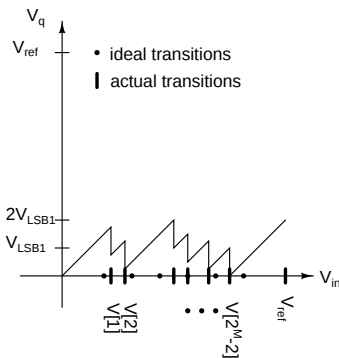


# Two step A/D with digital error correction (IIa)—Ideal A/D1



- $2^{M-1}V_q$  varies from 0 to  $V_{ref}$ ;  $V_{ref}/4$  to  $3V_{ref}/4$  except the first and last segments
- $2^{M-1}V_q$  outside this range implies errors in A/D1

# Two step A/D with digital error correction (IIa)—M bit accurate A/D1



- $2^{M-1}V_q$  varies from 0 to  $V_{ref}$
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1

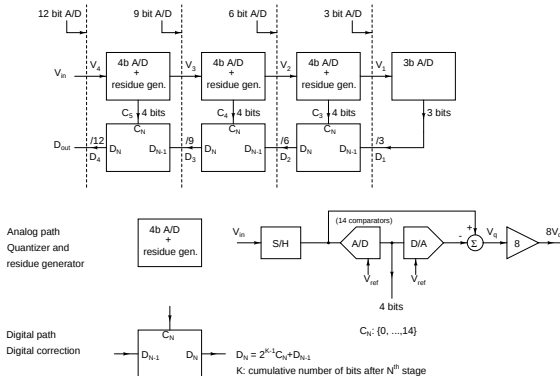
# Two step A/D with digital error correction (IIa)—M bit accurate A/D1

- A/D1 Transition shifted to the left
  - $m$  greater than its ideal value by 1
  - $k$  lesser than its ideal value by  $2^{K-1}$
  - A/D output  $n = 2^{K-1}m + k$  doesn't change
- A/D1 Transition shifted to the right
  - $m$  lesser than its ideal value by 1
  - $k$  greater than its ideal value by  $2^{K-1}$
  - A/D output  $n = 2^{K-1}m + k$  doesn't change
- 1 LSB error in  $m$  can be corrected

# Multi step converters

- Two step architecture can be extended to multiple steps
- All stages except the last have their outputs digitally corrected from the following A/D output
- Number of effective bits in each stage is one less than the stage A/D resolution
- Accuracy of components in each stage depends on the accuracy of the A/D converter following it.
- Accuracy requirements less stringent down the pipeline, but optimizing every stage separately increases design effort
- Pipelined operation to obtain high sampling rates
- Last stage is not digitally corrected

# Multi step A/D converter



- 4,4,4,3 bits for an effective resolution of 12 bits
- 3 effective bits per stage
- Digital outputs appropriately delayed before addition

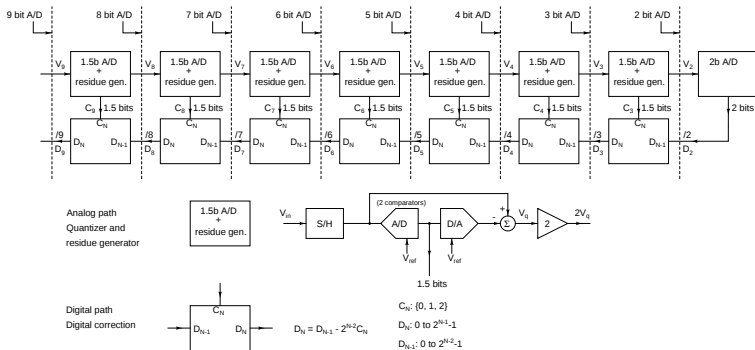
# Multi step converter-tradeoffs

- Large number of stages, fewer bits per stage
  - Fewer comparators, low accuracy-lower power consumption
  - Larger number of amplifiers-power consumption increases
  - Larger latency
- Fewer stages, more bits per stage
  - More comparators, higher accuracy designs
  - Smaller number of amplifiers-lower power consumption
  - Smaller latency
- Typically 3-4 bits per stage easy to design

# 1.5b/stage pipelined A/D converter

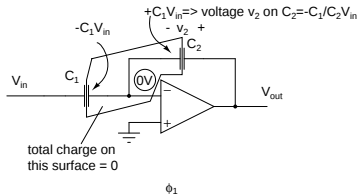
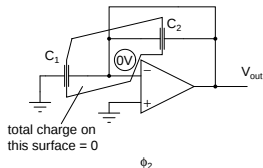
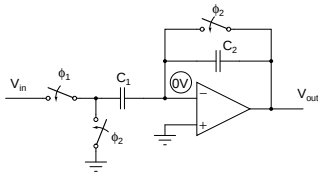
- To resolve 1 effective bit per stage, you need  $2^2 - 2$ , i.e. two comparators per stage
- Two comparators result in a 1.5 bit conversion (3 levels)
- Using two comparators instead of three (required for a 2 bit converter in each stage) results in significant savings

# 1.5b/stage pipelined A/D converter



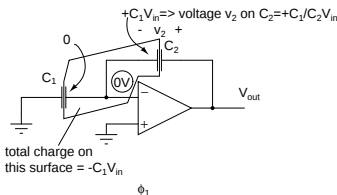
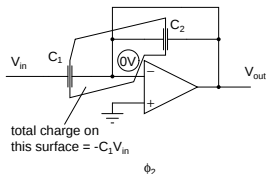
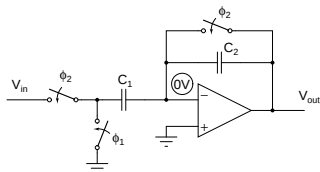
- Digital outputs appropriately delayed before addition

# Switched capacitor (SC) amplifier



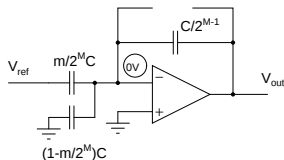
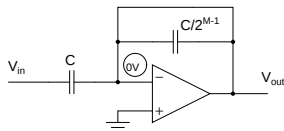
- $\phi_2$ :  $C_1$  connected to ground;  $C_2$  reset; reset switch provides dc negative feedback around the opamp
- $\phi_1$ : Input sampled on  $C_1$ ;  $C_2$  in feedback
- $\phi_2 \rightarrow \phi_1$ : Charge at virtual ground node is conserved  
 $\Rightarrow V_{out} = -C_1/C_2 V_{in}$

# Non inverting SC amplifier



- Change the phase of input sampling to invert the gain

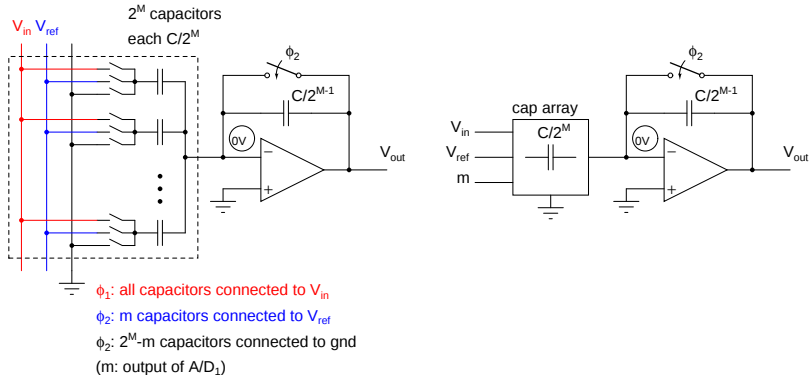
# SC realization of DAC and amplifier



m: output of A/D1

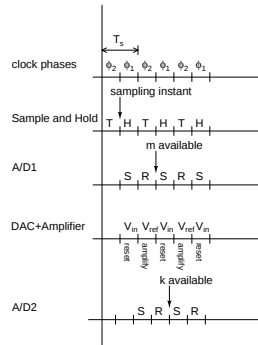
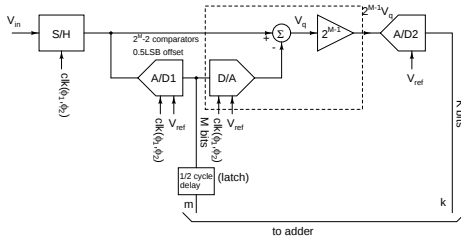
- Pipelined A/D needs DAC, subtractor, and amplifier
  - $V_{in}$  sampled on  $C$  in  $\phi_2$  (positive gain)
  - $V_{ref}$  sampled on  $m/2^M C$  in  $\phi_1$  (negative gain).
  - At the end of  $\phi_1$ ,  $V_{out} = 2^{M-1} (V_{in} - m/2^M V_{ref})$

# SC realization of DAC and amplifier



- $m/2^M C$  realized using a switched capacitor array controlled by  $A/D_1$  output

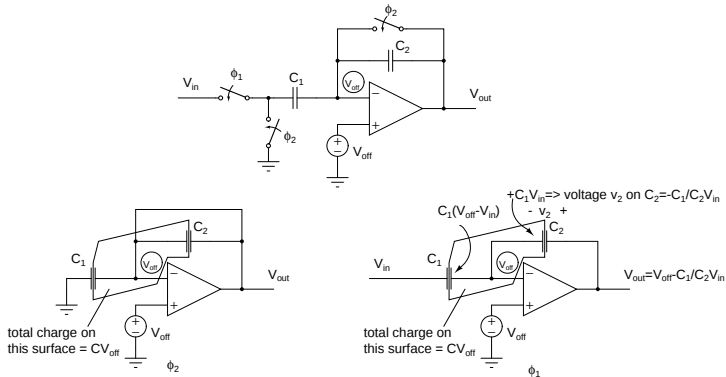
# Two stage converter timing and pipelining



# Two stage converter timing and pipelining

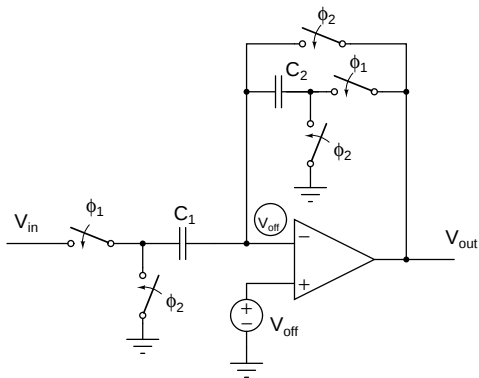
- $\phi_1$ 
  - S/H holds the input  $V_i[n]$  from the end of previous  $\phi_2$
  - A/D1 samples the output of S/H
  - Amplifier samples the output of S/H on C
  - Opamp is reset
- $\phi_2$ 
  - S/H tracks the input
  - A/D1 regenerates the digital value  $m$
  - Amplifier samples  $V_{ref}$  of S/H on  $m/2^M C$
  - Opamp output settles to the amplified residue
  - A/D2 samples the amplified residue
- $\phi_2$ 
  - A/D2 regenerates the digital value  $k$ .  $m$ , delayed by  $1/2$  clock cycle, can be added to this to obtain the final output
  - S/H, A/D1, Amplifier function as before, but on the next sample  $V_i[n+1]$
- In a multistep A/D, the phase of the second stage is reversed when compared to the first, phase of the third stage is the same as the first, and so on

# Effect of opamp offset



- $\phi_2$ :  $C_1$  is charged to  $V_{in} - V_{off}$  instead of  $V_{in} \Rightarrow$  input offset cancellation; no offset in voltage across  $C_2$
- $\phi_2$ :  $V_{out} = -C_1/C_2 V_{in} + V_{off}$ ; Unity gain for offset instead of  $1 + C_1/C_2$  (as in a continuous time amplifier)

# Correction of offset on $C_2$

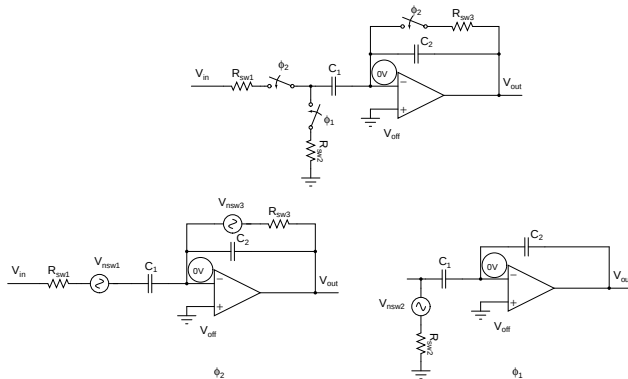


- $\phi_2$ : Charge  $C_2$  to the offset voltage instead of 0V
- $\phi_1$ :  $V_{out} = -C_1/C_2 V_{in}$ ; Offset completely cancelled

# Nonidealities

- Random mismatch: Capacitors must be large enough (relative matching  $\propto 1/\sqrt{WL}$ ) to maintain DAC, amplifier accuracy
- Thermal noise: Capacitors must be large enough to limit noise well below 1 LSB. Opamp's input referred noise should be small enough.
- Opamp dc gain: Should be large enough to reduce amplifier's output error to  $V_{ref}/2^{K+1}$ .
- Opamp bandwidth: Should be large enough for amplifier's output settling error to be less than  $V_{ref}/2^{K+1}$ .

# Thermal noise in SC amplifiers

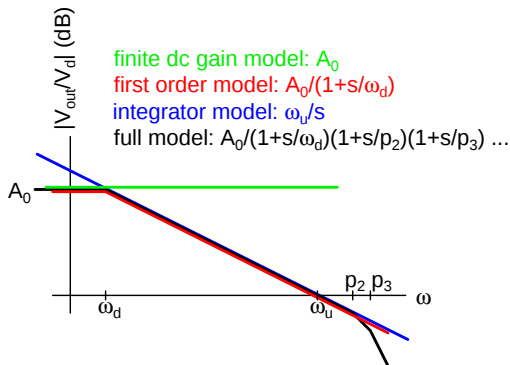


- Noise from switch resistances
- Noise from the amplifier-ignored

# Thermal noise in SC amplifiers

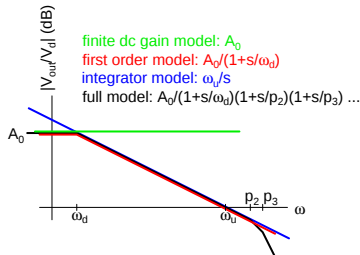
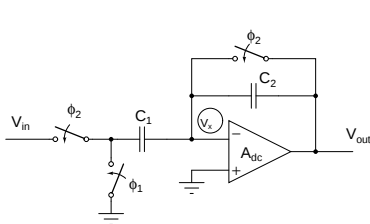
- $\phi_2$ :
  - $R_{SW1}$ :  $C_1$  has a voltage noise of variance  $kT/C_1$
  - $R_{SW2}$ :  $C_2$  has a voltage noise of variance  $kT/C_2$ .
- $\phi_1$ :
  - $R_{SW1}$ : Its contribution in  $\phi_2$  ( $kT/C_1$ ) will be amplified to  $kT/C_1(C_1/C_2)^2$
  - $R_{SW2}$ : Its contribution in  $\phi_2$  ( $kT/C_1$ ) will be held
  - $R_{SW3}$ : Results in a noise  $kT/C_1$  on  $C_1$  and  $kT/C_1(C_1/C_2)^2$  at the output
- Total output noise:  $kT/C_2(2C_1/C_2 + 1) \approx 2kT/C_1(C_1/C_2)^2$
- Input referred noise:  $kT/C_1(2 + C_2/C_1) \approx 2kT/C_1$
- $C_1$  must be large enough to minimize the effects of thermal noise

# Op amp models



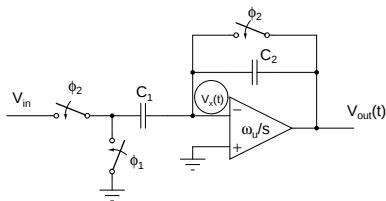
- Opamp has finite dc gain, predominantly first order rolloff, and many high frequency poles
- High frequency poles should be beyond the unity gain frequency of the feedback loop gain (not necessarily the opamp's open loop gain) for stability.
- Effect of dc gain and first order rolloff modeled separately for simplicity

# Effect of opamp dc gain

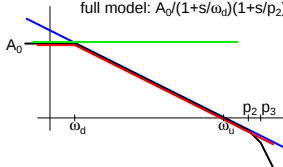


- $\phi_2$ :  $V_{out} = V_x = 0$
- $\phi_1$ :  $V_{out} = C_1/C_2 \times 1/[1 + (1 + C_1/C_2)/A_0]V_{in}$ ;
- Reduced dc gain in the amplifier
- Error should be smaller than  $V_{ref}/2^{K+1} \Rightarrow$   
 $A_0 > 2^{M+K} + 2^{K+1} - 2^{M-1} - 1$
- Approximately,  $A_0 > 2^{M+K}$ , 2/LSB of the overall converter

# Effect of finite unity gain frequency of the opamp

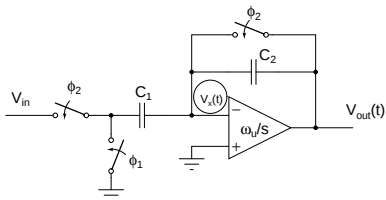


finite dc gain model:  $A_0$   
 first order model:  $A_0/(1+s/\omega_u)$   
 integrator model:  $\omega_u/s$   
 full model:  $A_0/(1+s/\omega_u)(1+s/p_2)(1+s/p_3) \dots$

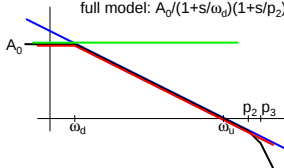


- $\phi_2$ :  $V_{out}(t) = V_x(t) = V_{out}(0) \exp(-\omega_u t)$
- Incomplete reset
- Worst case:  $V_{out}(0) = V_{ref}$ ; Error smaller than  $V_{ref}/2^{K+1}$  at the  $t = T_s/2$
- $\omega_u \geq 2 \ln(2)(K + 1)f_s$
- $p_{2,3,\dots} > \omega_u$

# Effect of finite unity gain frequency of the opamp



finite dc gain model:  $A_0$   
 first order model:  $A_0/(1+s/\omega_u)$   
 integrator model:  $\omega_u/s$   
 full model:  $A_0/(1+s/\omega_u)(1+s/p_2)(1+s/p_3) \dots$

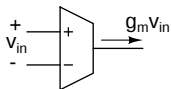


- $\phi_1$ :  $V_{out}(t) = C_1/C_2 V_{in} \left( 1 - \exp(-\omega_u \frac{C_2}{C_1+C_2} t) \right) + V_{out}(0) \exp(-\omega_u \frac{C_2}{C_1+C_2} t)$
- Incomplete settling of amplified residue  $V_q$
- Worst case:  $C_1/C_2 V_{in} = V_{ref}$ ; Error smaller than  $V_{ref}/2^{K+1}$  at the  $t = T_s/2$ ;  $V_{out}(0) = 0$  after reset.
- $\omega_u/(1 + 2^{M-1}) \geq 2 \ln(2)(K + 1)f_s$  ( $\omega_u$  in rad/s,  $f_s$  in Hz)
- $\omega_u/(1 + 2^{M-1})$  is the unity loop gain frequency assuming no parasitics
- $p_{2,3,\dots} > \omega_u/(1 + 2^{M-1})$

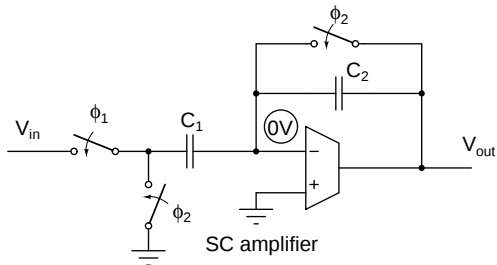
# Effect of finite unity gain frequency of the opamp

- Depending on amplifier topology, reset and amplifying phases pose different constraints
- In our example, amplifying phase constraint is more stringent (loop gain in amplifying and reset phases are very different-better to have them close to each other)
- $\omega_u$  itself can depend on capacitive load(different for  $\phi_1, \phi_2$ )
- Higher order poles  $p_2, p_3, \dots$  need to be placed above the unity loop gain frequency, not necessarily  $\omega_u$

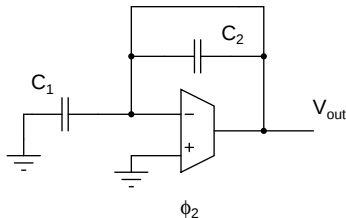
# Single stage opamp-transconductor



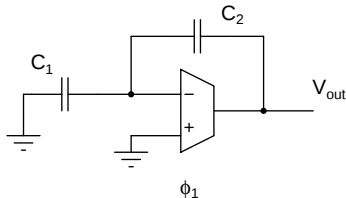
Model of a single stage opamp



SC amplifier



$\phi_2$

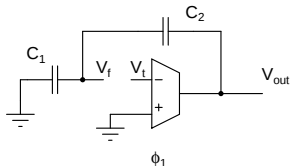
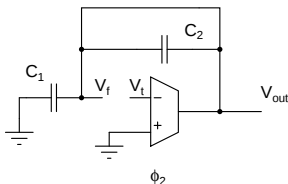


$\phi_1$

- $\phi_2$ : Capacitive load =  $C_1$
- $\phi_1$ : Capacitive load =  $C_1 C_2 / (C_1 + C_2)$

# Single stage opamp-transconductor

Loop opened at  
opamp input



- Loop broken at the opamp input to evaluate loop gain

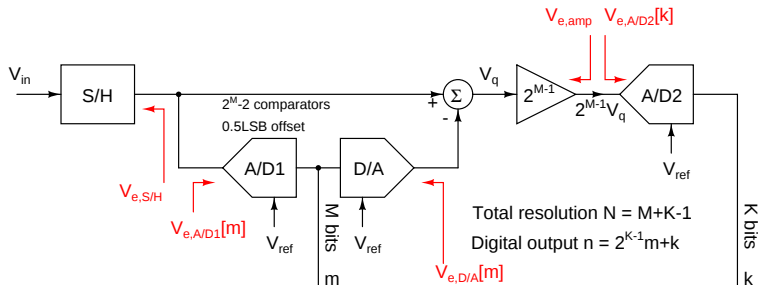
- $\phi_2$

- $V_{out}(s)/V_t(s) = g_m/sC_1$
- Opamp unity gain frequency  $\omega_u = g_m/C_1$
- $V_f(s)/V_t(s) = g_m/sC_1$
- Unity loop gain frequency  $\omega_{u,loop} = g_m/C_1$

- $\phi_1$

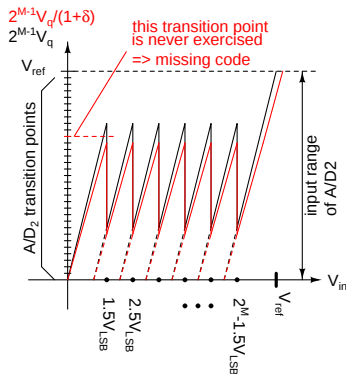
- $V_{out}(s)/V_t(s) = g_m/s(C_1C_2/C_1 + C_2)$
- Opamp unity gain frequency  $\omega_u = g_m/(C_1C_2/C_1 + C_2)$
- $V_f(s)/V_t(s) = g_m/sC_1$
- Unity loop gain frequency  $\omega_{u,loop} = g_m/C_1$

# Two step A/D: errors



- Model each error as an error voltage
- Determine  $V_{in}[m]$  for which A/D1 changes from  $m - 1$  to  $m$
- Determine  $V_{in}[m, k]$  for which A/D1 output is  $m$  and A/D2 changes from  $k - 1$  to  $k$
- Compare  $V_{in}[m, k]$  to corresponding ideal values to find the error

# Two step A/D: Residue amplifier gain error



- Amplified residue doesn't exercise all combinations of  $m, k$
- Results in missing codes

# Two step A/D: Residue amplifier gain error

Ideally

$$\frac{V_{in}[m, k]}{V_{ref}} = \frac{m2^{K-1} + k}{2^{M+K-1}}$$

With gain error

$$V_{in}[m, k] = \frac{mV_{ref}}{2^M} + \frac{kV_{ref}}{2^{M+K-1}}(1 + \delta)$$
$$\frac{V_{in}[m, k]}{V_{ref}} = \frac{2^{K-1}m + k(1 + \delta)}{2^{M+K-1}}$$

- Digital representation of  $V_{in}[m, k]$  corresponds to an output of  $2^{K-1}m + k(1 + \delta)$
- $k$  must be digitally multiplied by  $1 + \delta$  before addition

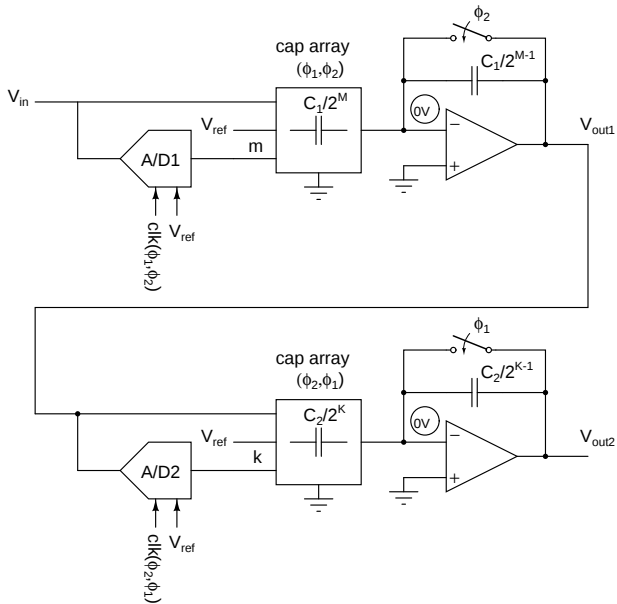
# Two step A/D: Correction for gain error

- $k$  must be digitally multiplied by  $1 + \delta$  before adding it to  $2^{K-1}m$
- $(1 + \delta)$  of the form  $1.00000xxx_2 \Rightarrow$  Wider multipliers necessary at each stage
- Although  $D_{out} = 2^{K-1}m + (1 + \delta)k$  versus  $V_{in}[m, k]$  is linear, some combinations of  $[m, k]$  are missing  $\Rightarrow$  reduced effective resolution
- Effective resolution is smaller than  $M + K - 1$  and  $K$  needs to be increased to preserve resolution
- If amplifier gain error varies from  $\delta_1$  to  $\delta_2$ , calibrate for  $(\delta_1 + \delta_2)/2$

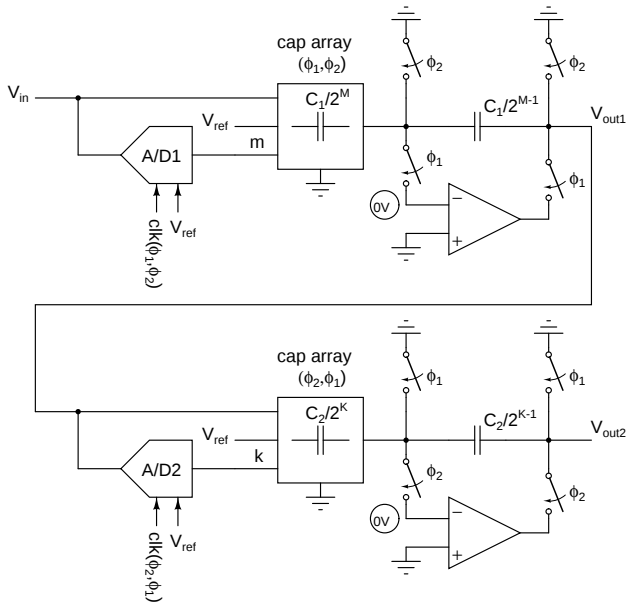
# Multi step converter-opamp power consumption

- Opamp power consumption a large fraction of the converter power consumption
- Amplification only in one phase
- Successive stages operate in alternate phases
- Share the amplifiers between successive stages ([1])

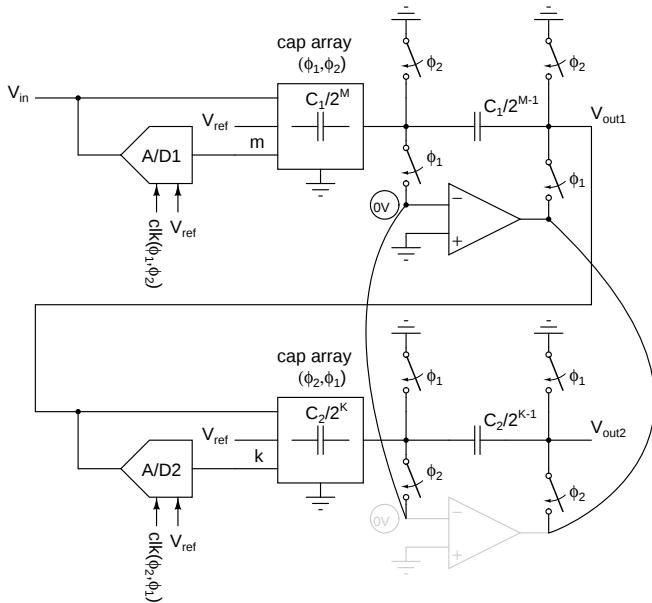
# Multi step converter-with offset cancellation



# Multi step converter-no offset cancellation



# Multi step converter-Amplifier sharing



# Multi step converter

- First stage uses the opamp only in  $\phi_1$
- Second stage uses the opamp only in  $\phi_2$
- Use a single opamp
  - Switch it to first stage in  $\phi_1$
  - Switch it to second stage in  $\phi_2$
- Reduces power consumption
- Cannot correct for opamp offsets
- Memory effect because of charge storage at negative input of the opamp

# Multi step converter-Further optimization ([2])

- Alternate stages with more and fewer bits e.g. 3-1-3-1
- Optimized loading
- Use a two stage opamp for stage 1 (High gain)
- Use a single stage opamp for stage 2 (Low gain)

# Multi step converter-Further optimization ([2])

- Use a single two stage opamp
  - Use both stages for stage 1 of the A/D
  - Use only the second stage for stage 2 of the A/D
  - Feedback capacitor in stage 2 of the A/D appears across the second stage of the opamp—Miller compensation capacitor
- Further Reduces power consumption
- Optimized realization in [2] achieves 12 bit resolution at 21 MS/s using 35 mW in 0.6  $\mu\text{m}$  CMOS

# References



K. Nagaraj et al., "A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers", *IEEE Journal of Solid-State Circuits*, pp. 312-320, vol. 32, no. 3, March 1997.



S. Kulhalli et al., "A 30mW 12b 21MSample/s pipelined CMOS ADC", *2002 IEEE International Solid State Conference*, pp. 18.4, vol. I, pp. 248-249, vol. II.