Loop Stability Analysis

Differential Opamp Simulation

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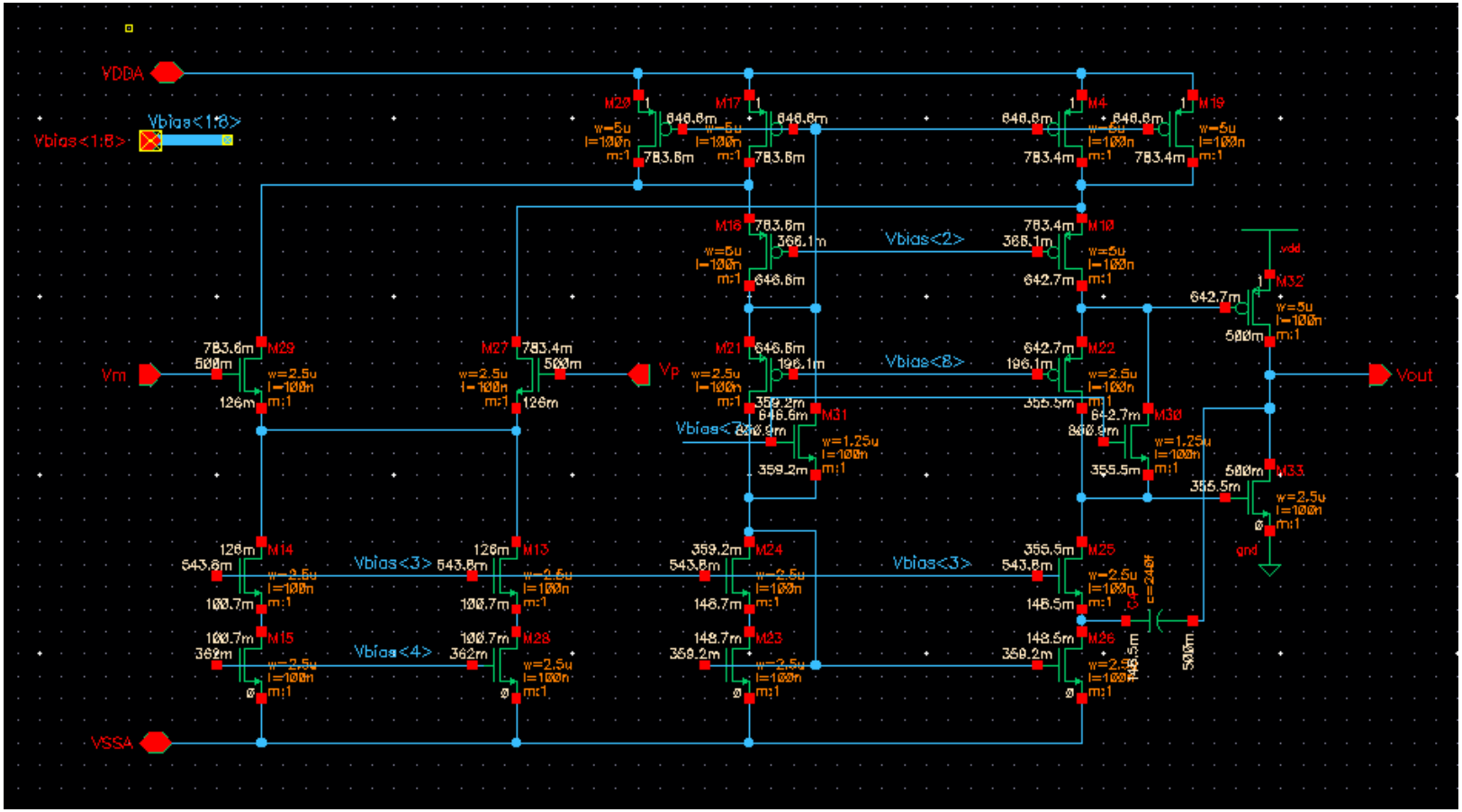
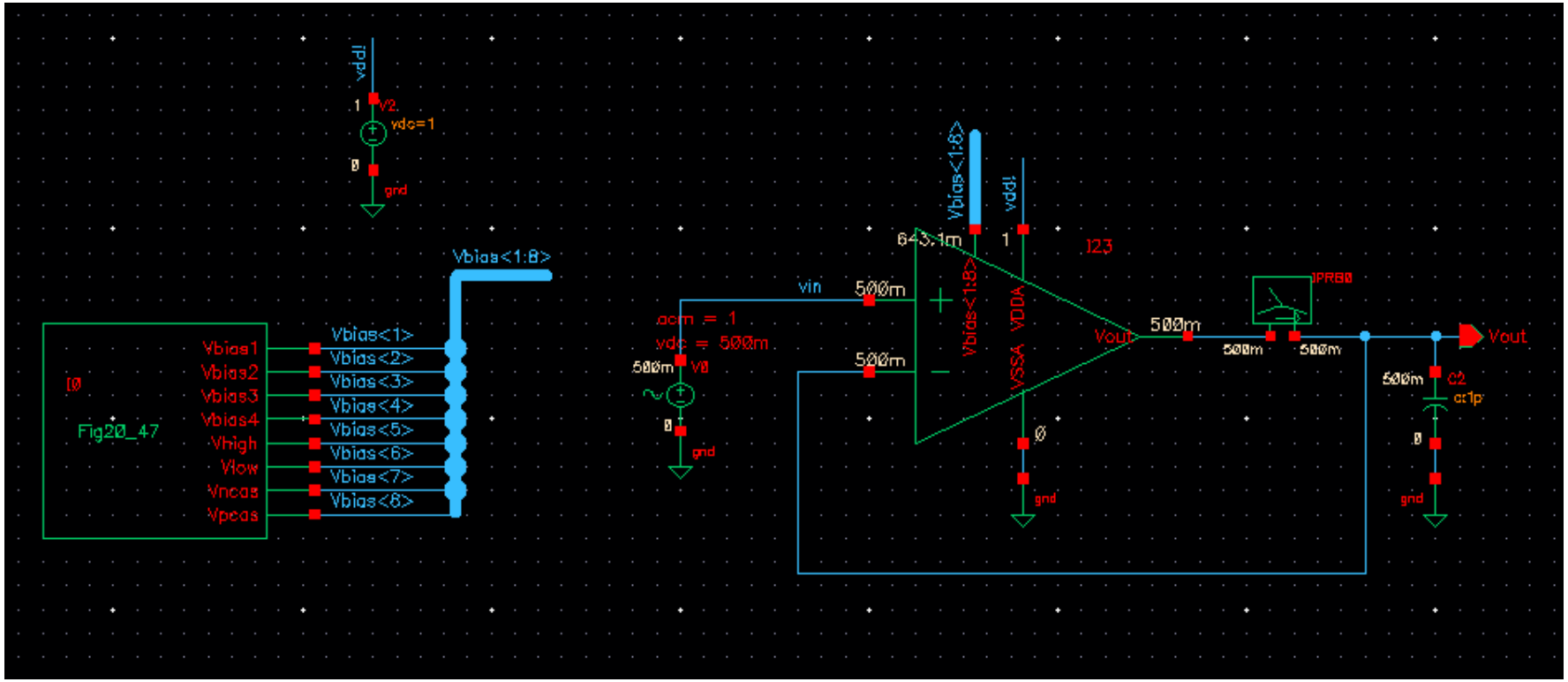
Spectre STB Analysis

- The STB analysis linearizes the circuit about the DC operating point and computes the loop-gain, gain and phase margins (if the sweep variable is frequency), for a feedback loop or a gain device [1].
- Refer to the Spectre Simulation Refrence [1] and [2] for details.
- Uses return ratio analysis method to calculate loop-gain and phase margin ([3, 4]).

Example Single-ended Opamp Schematic

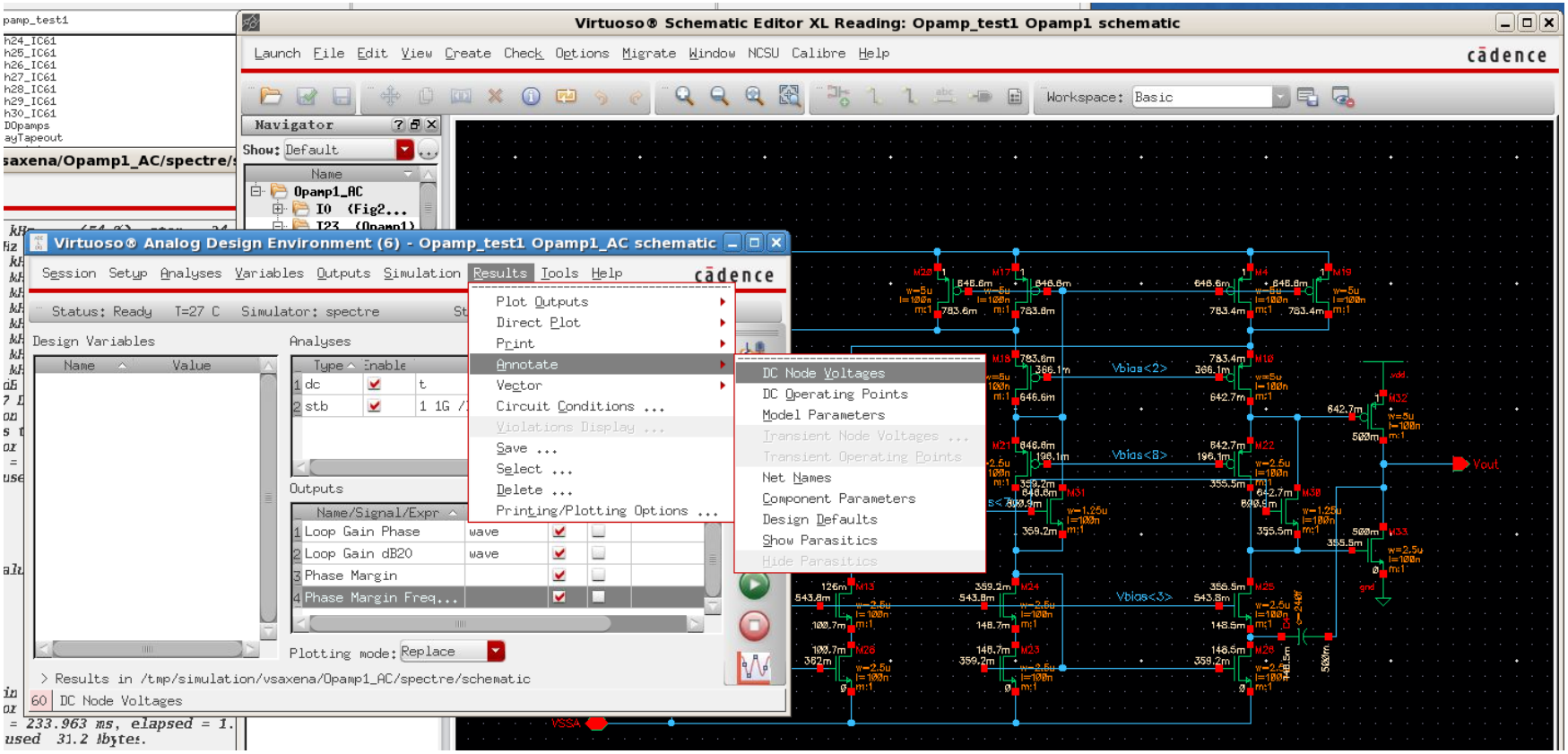


STB Analysis Test Bench



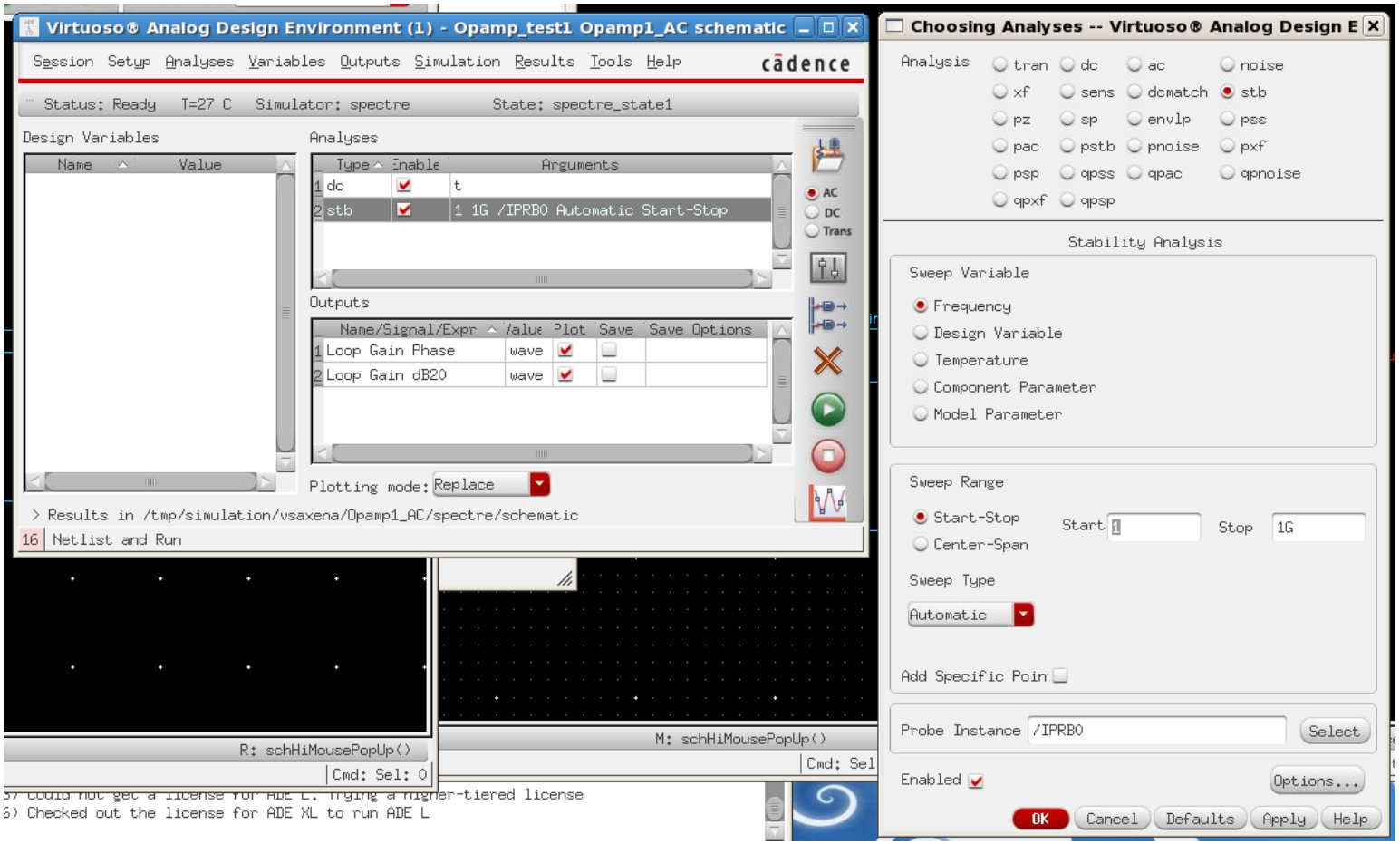
- Pay attention to the **iprobe** component (from analogLib)
  - Acts as a short for DC, but breaks the loop in stb analysis
- Place the probe at a point where it **completely breaks (all) the loops.**

DC Annotation



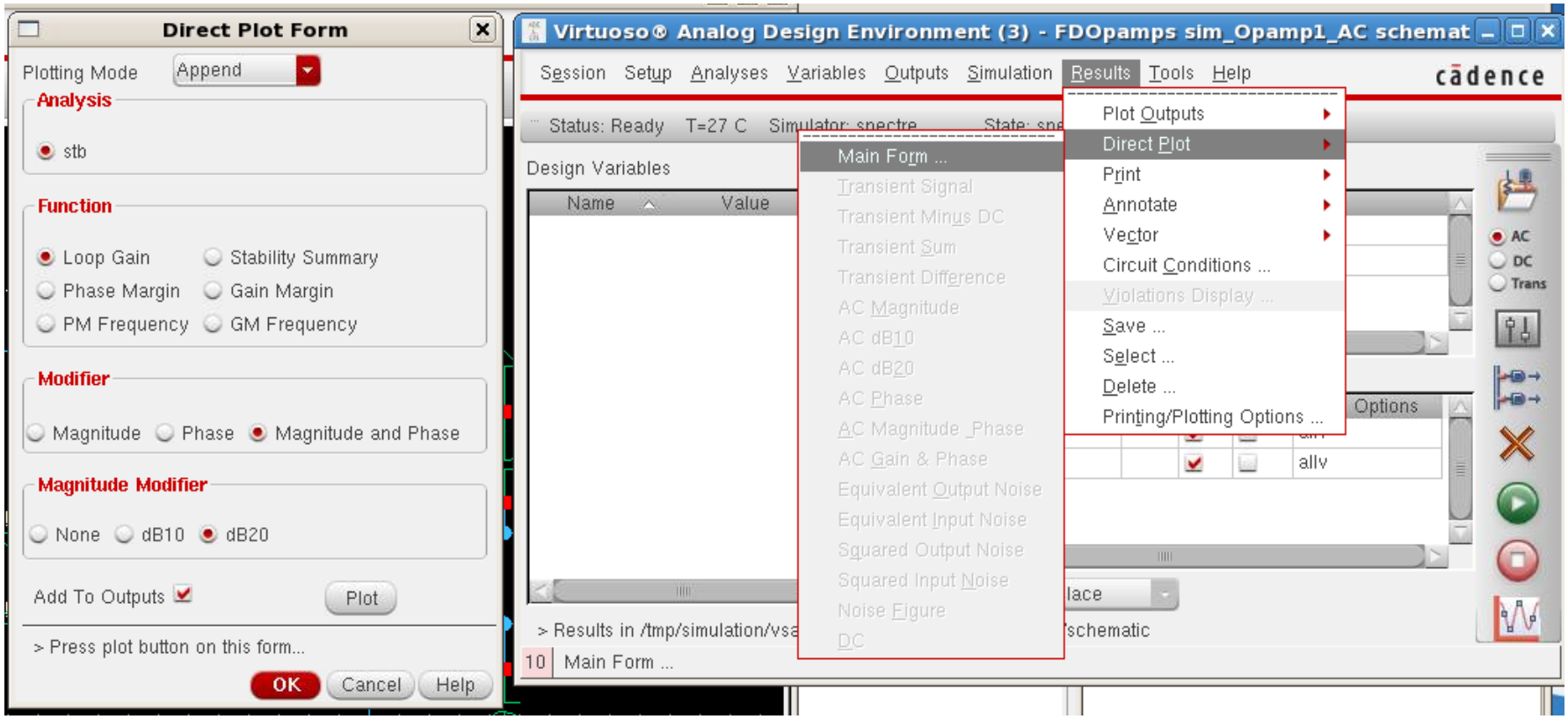
- Annotating the node voltages and DC operating points of the devices helps debug the design
  - Check device gds to see if its in triode or saturation regions

Simulation Setup



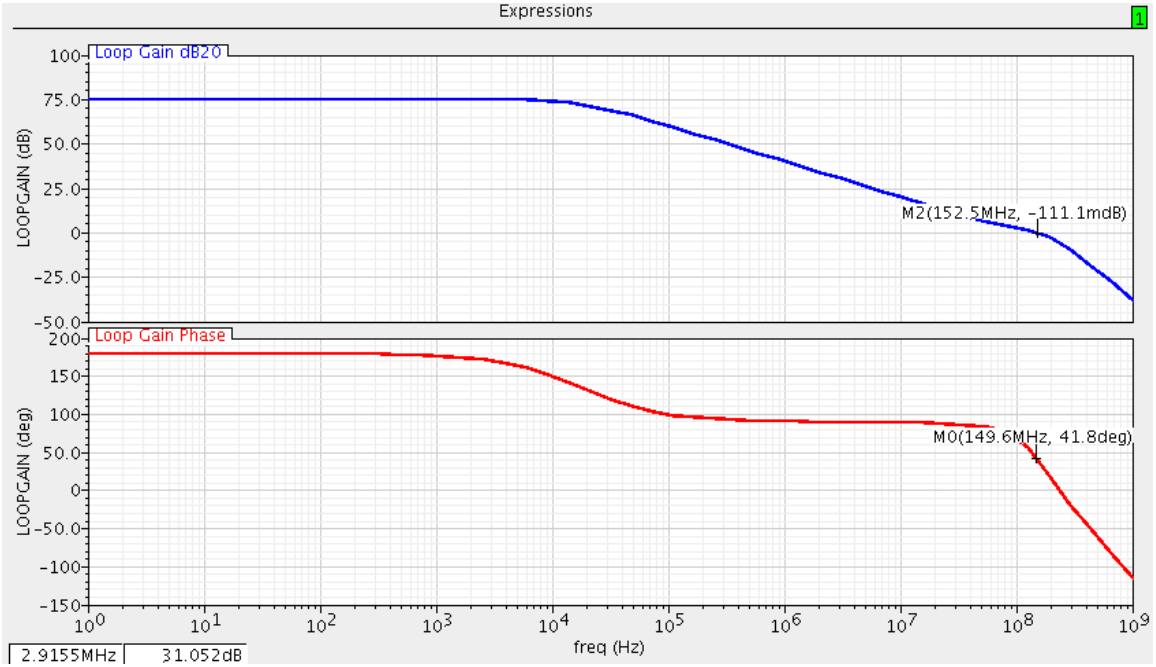
- Always have dc analysis on for debugging purpose

Bode Plot Setup



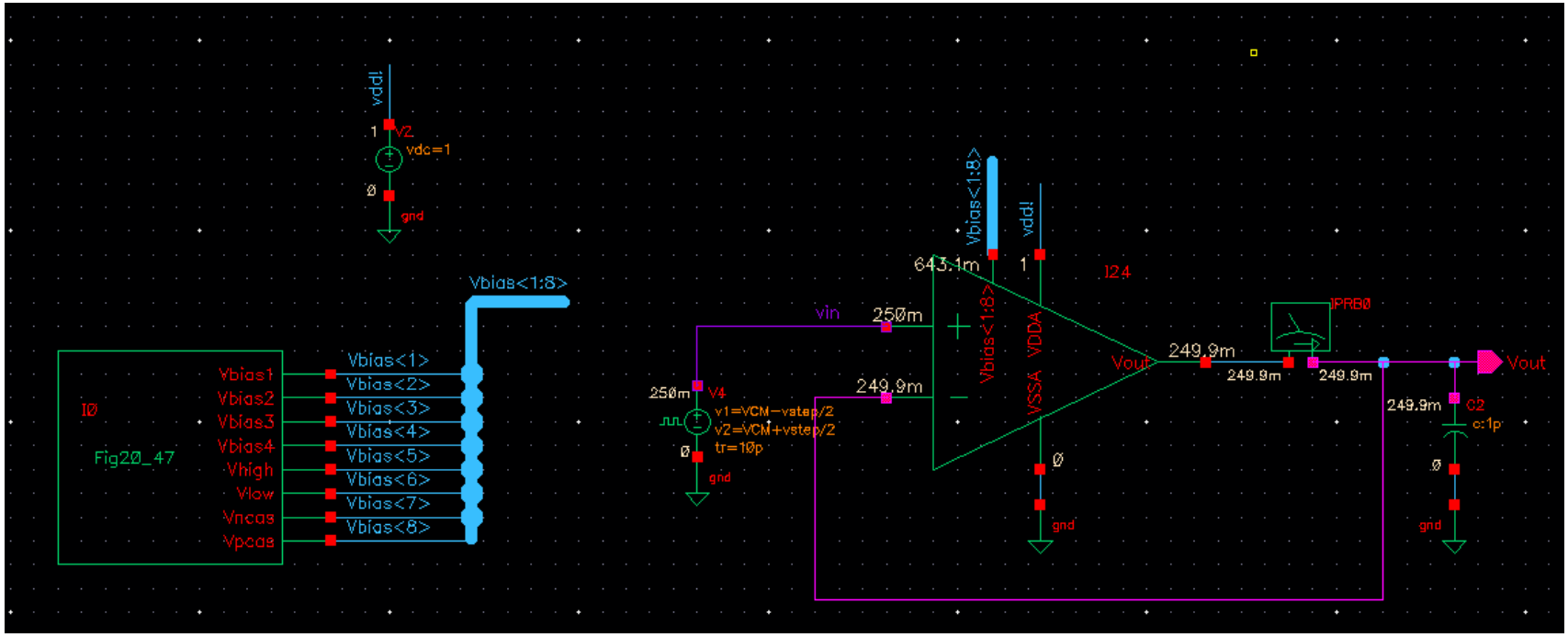
- Results →Direct Plot →Main Form

Loop Response Bode Plots



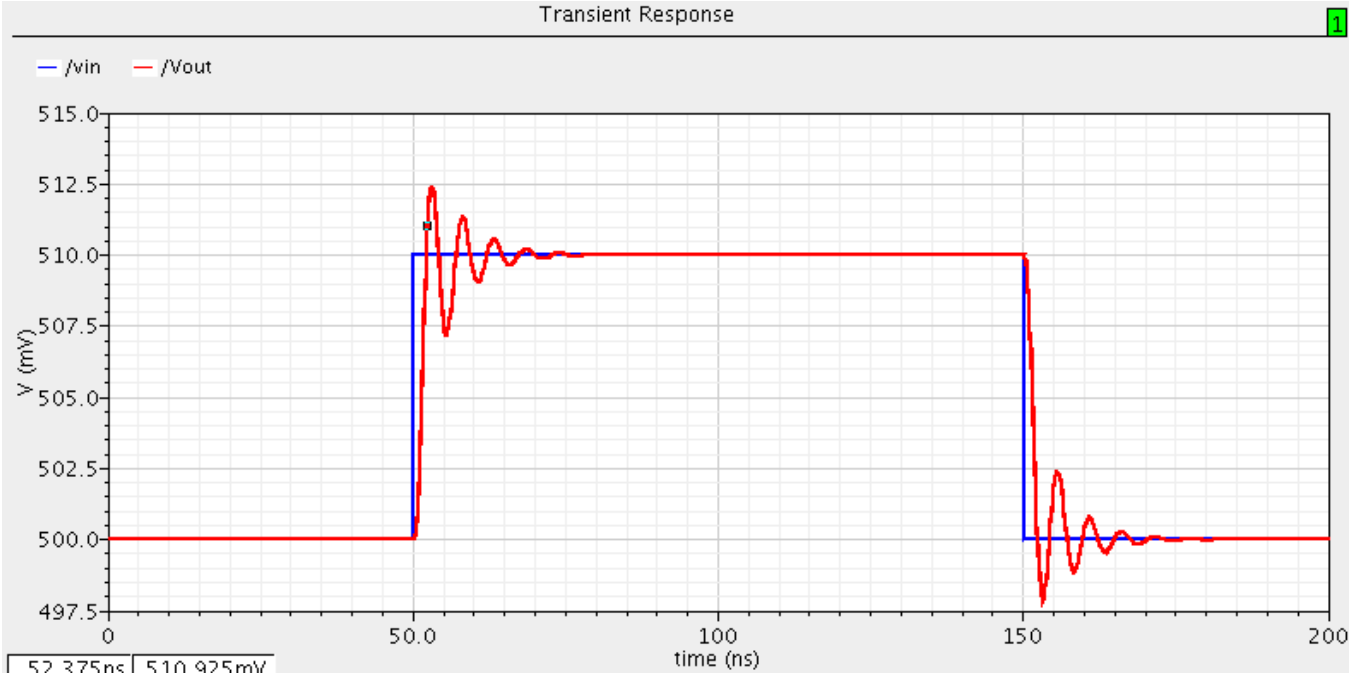
- Here, f_{un}=152.5 MHz, PM=41.8º
- Try to use the stb analysis while the circuit is in the desired feedback configuration
  - Break the loop with realistic DC operating points

Transient Step Response Test Bench



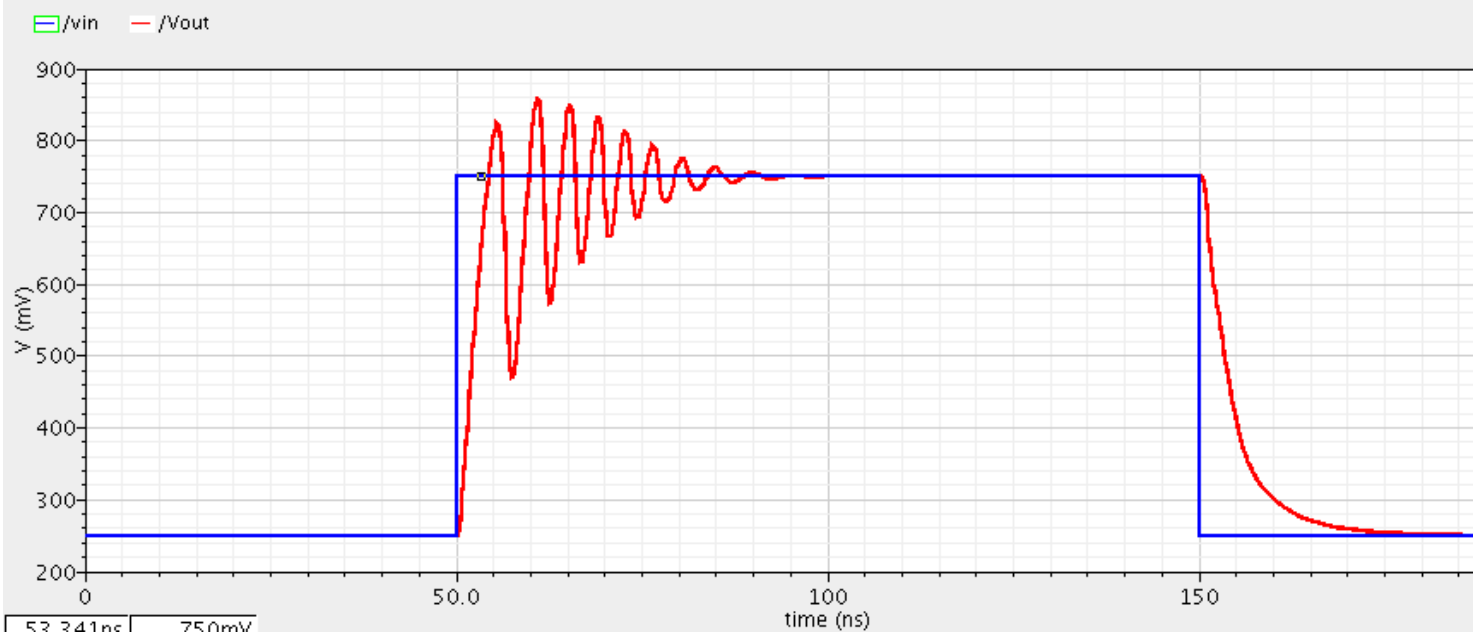
- Transient step-response verifies the closed-loop stability
- Use small as wells as large steps for characterization
- iprobe acts as a short (can remove it from transient sims)

Small Step Response



- Observe the ringing (PM was 41º)
  - Compensate more!
  - Correlate small-step response with the open-loop frequency response for your understanding.

Large Step Response

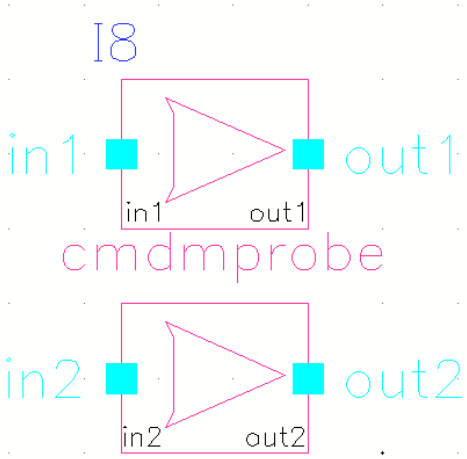


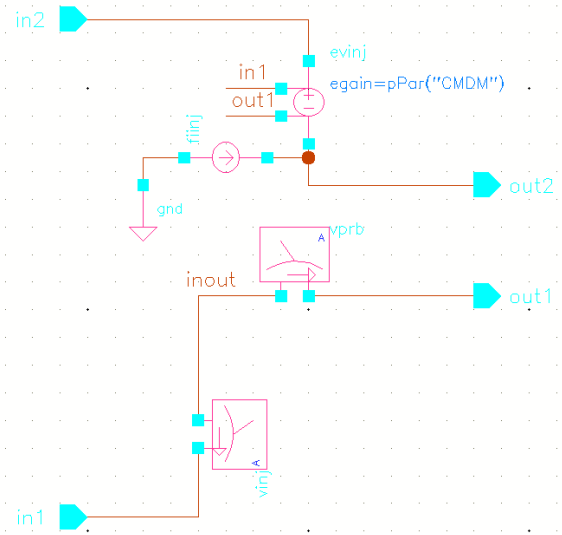
- Use large steps for large signal response
  - Not captured by the small-signal analysis
  - Note the slewing in the output here

Fully-Differential Opamp Simulation

Continuous-time CMFB

CMDM Probe

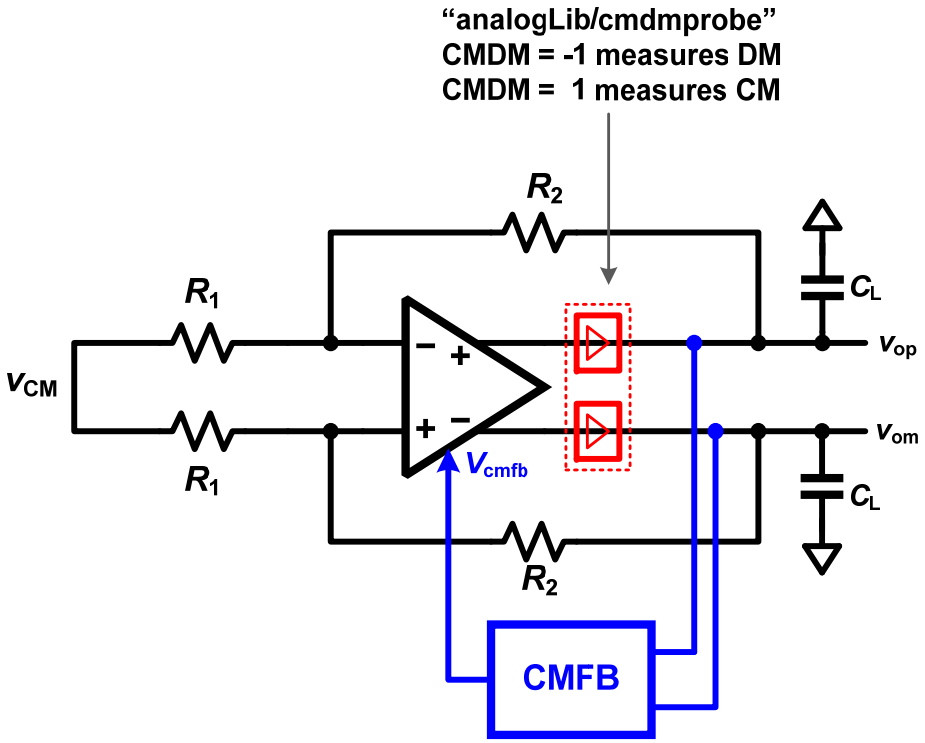




- Located in library: AnalogLib→cmdmprobe
- Variable CMDM =
  - -1 measures differential mode response
  - +1 measures common mode response
- In IC615, diffstbprobe is available which handles unbalanced differential circuits better than the cmdmprobe.
- More information on the differential probes and the STB analysis algorithm can be found in [4].

Fully Differential Circuit Analysis

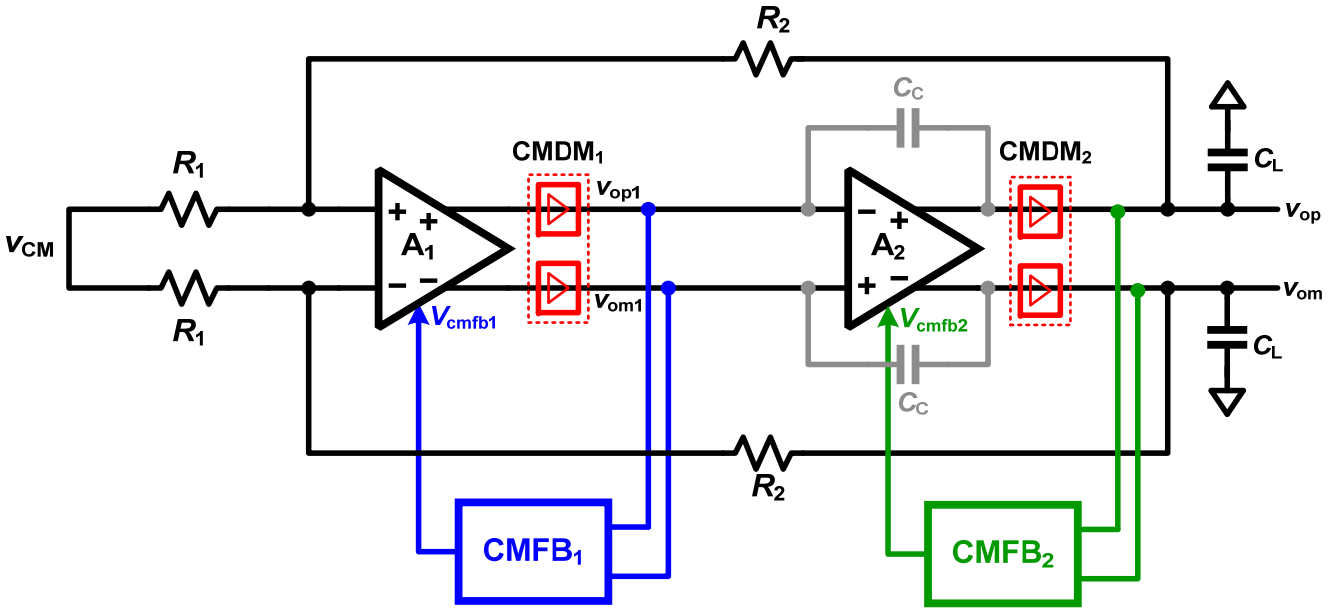
- Use CMDM probe for differential analysis [1, 3]
- Placement of the CMDM probe should break the differential as well the common-mode loops.



Fully Differential Circuit Analysis Method1

- For internal loops, isolate those loops individually and perform STB analysis
  - Ensure overall DC feedback for accurate biasing and that all loops are compensated
  - $CMDM_1$ measures only the first-stage CM response
  - $CMDM_2$ measures overall DM response and second-stage CM response

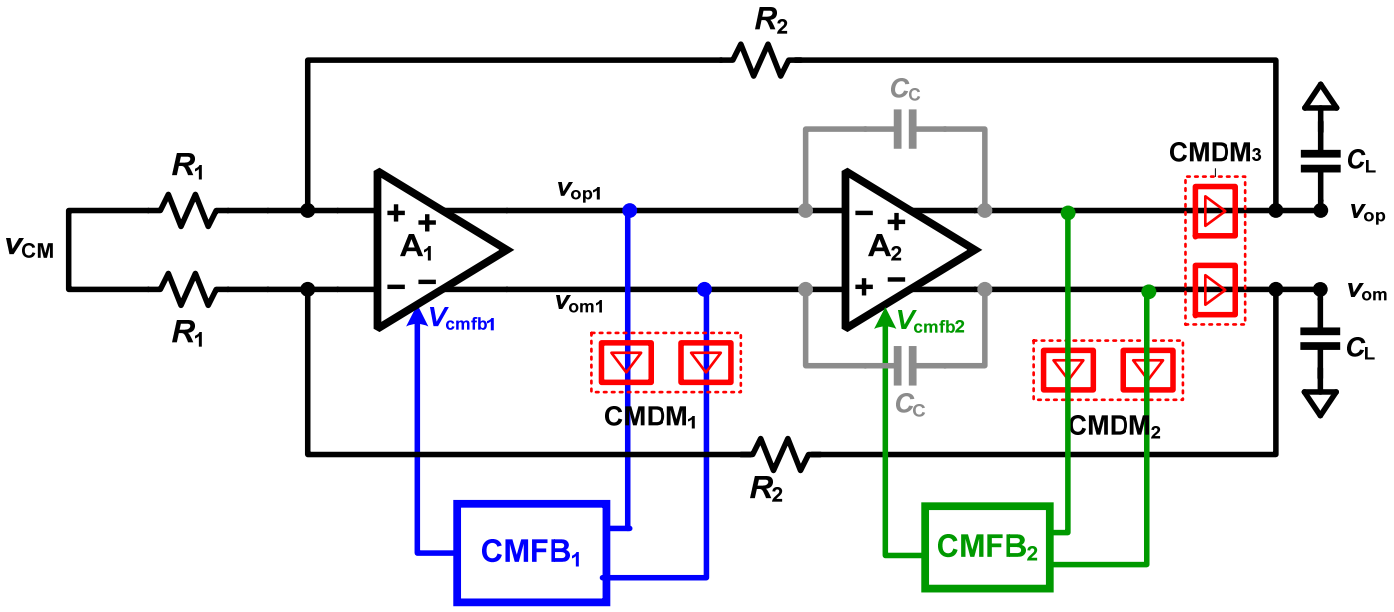
Two-stage Opamp STB Analysis



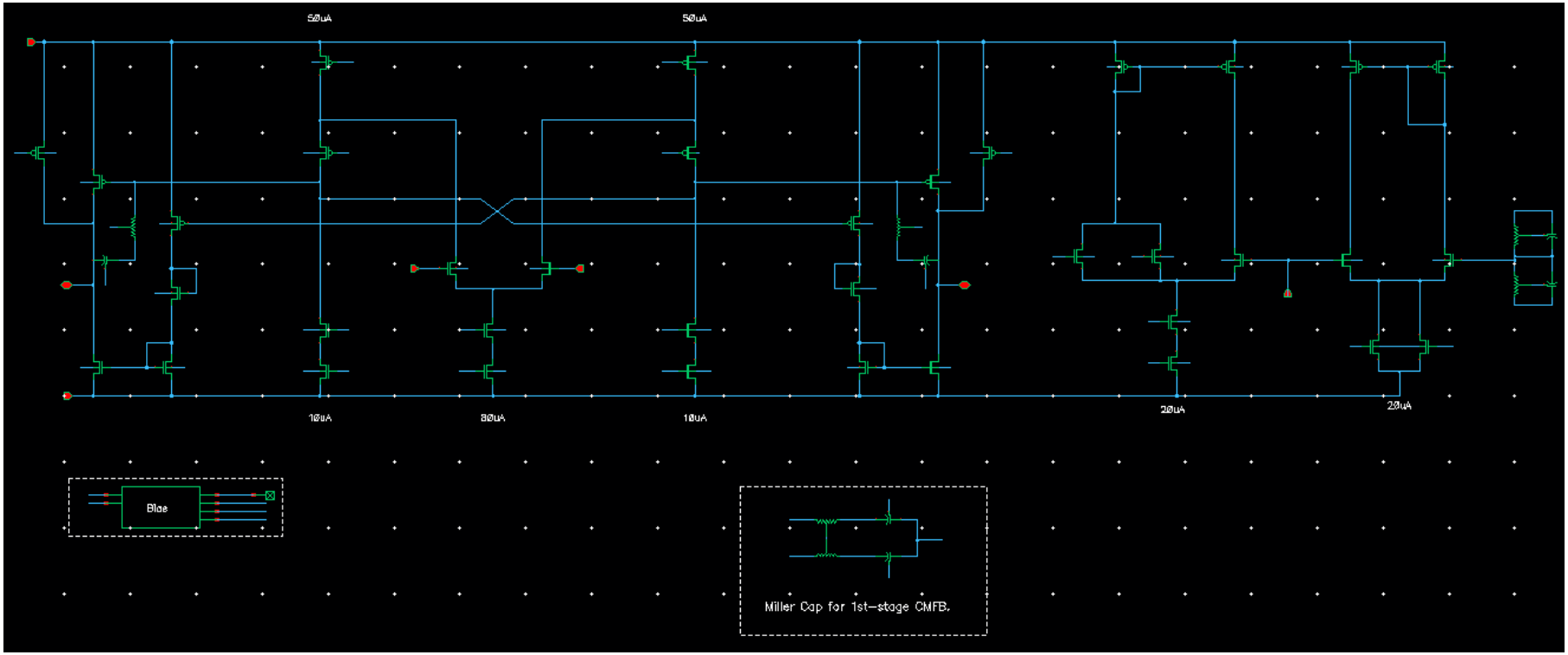
Fully Differential Circuit Analysis Method2

- cmdmprobes placed outside DM loop, only in CMFB loops
  - $CMDM_1$ measures only the first-stage CM response
  - $CMDM_2$ measures only the second-stage CM response
  - But need another CMDM probe to measure DM loop stability
  - Results match with iprobe results very well.

Two-stage Opamp STB Analysis

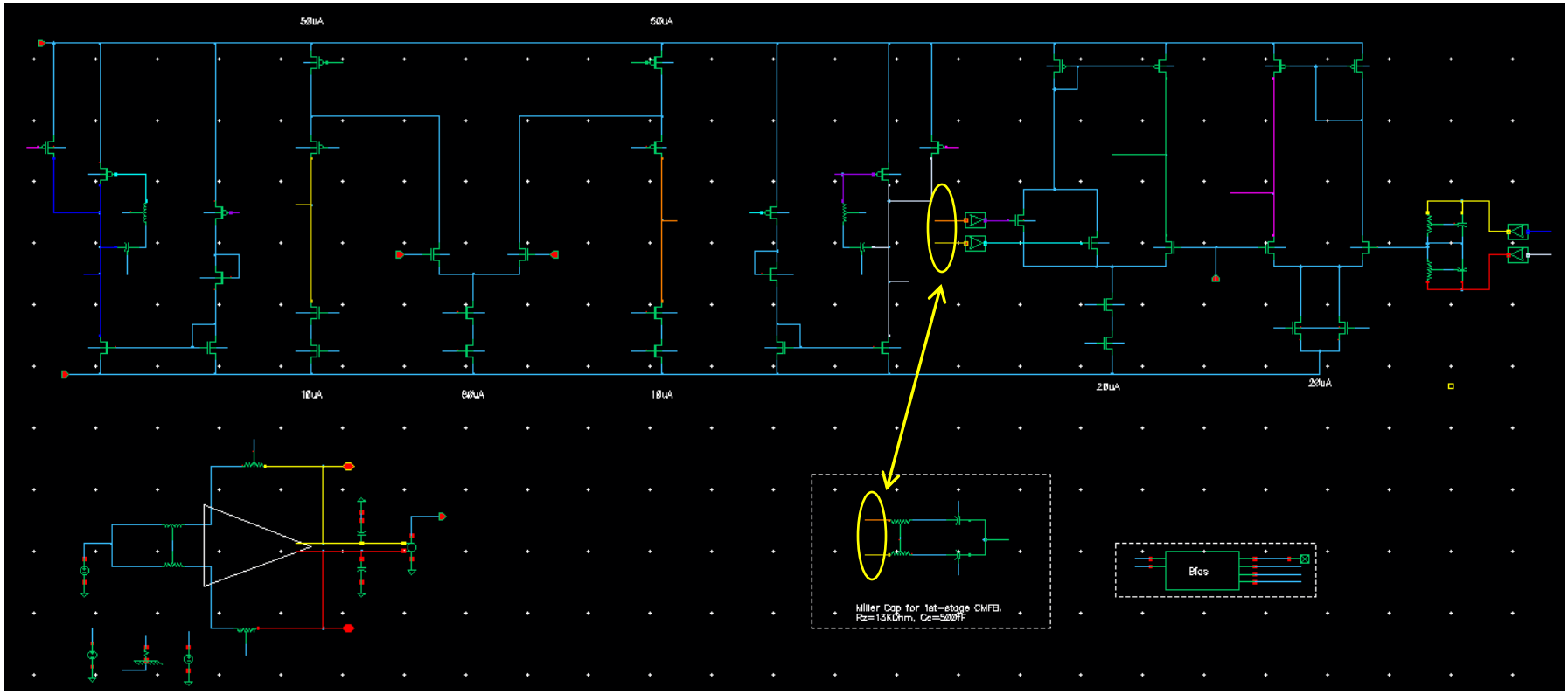


Fully Differential Opamp Schematic



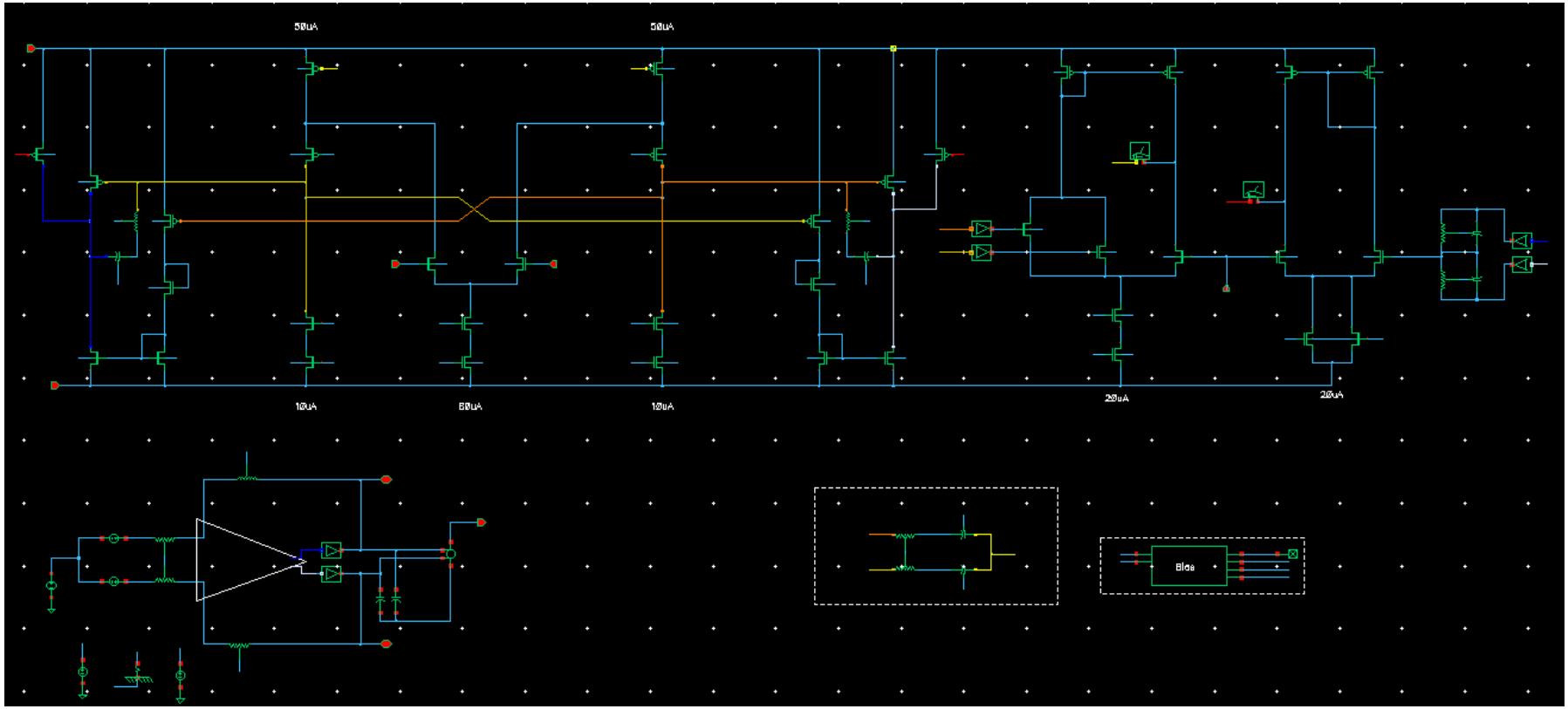
- Two-stage fully differential opamp
- Class AB output stage for large voltage swing
- With individual CMFB.
- 1st stage CMFB compensated

STB Analysis Using Method 1



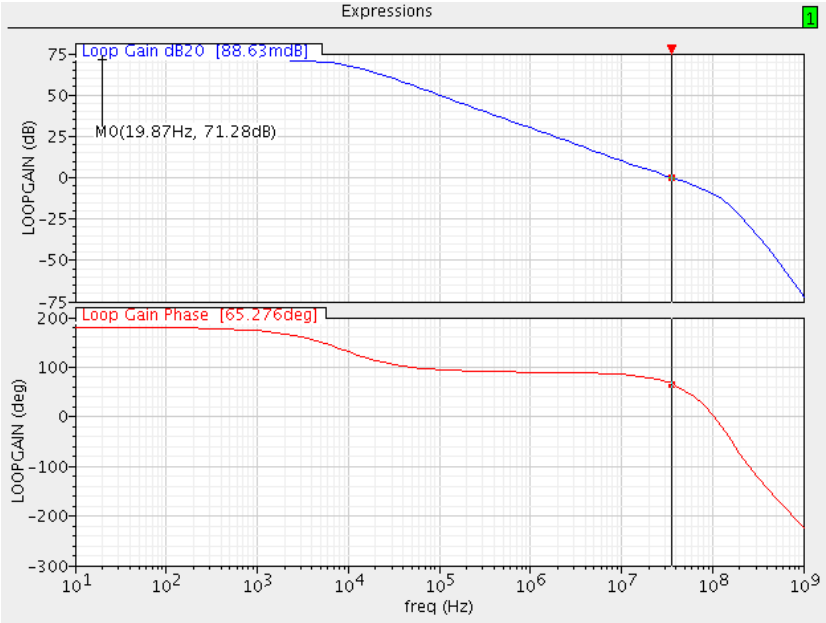
- Be noted that the nulling resistors should be connected before the inputs of cmdmprobe in the 1st CMFB loop, or it will generate incorrect results.

STB Analysis Using Method 2



- Need one extra cmdmprobe to measure DM loop comparing to method 1.

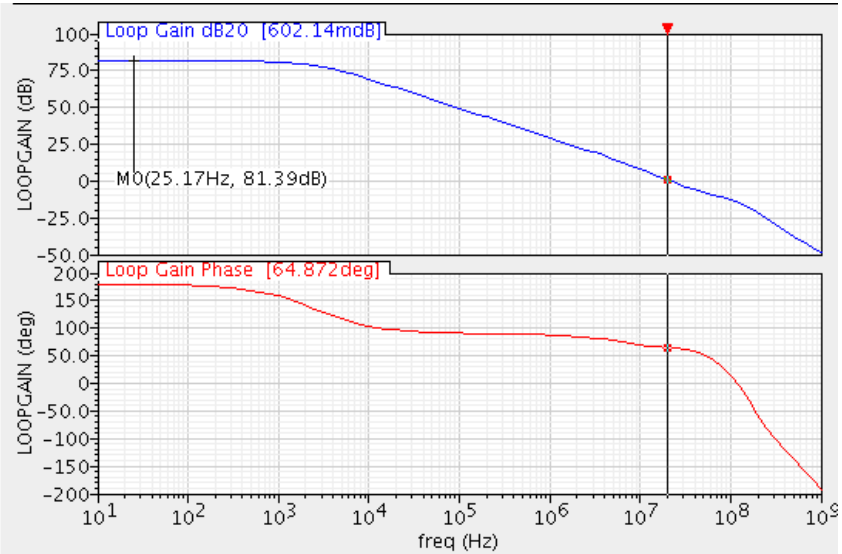
DM Loop Bode Plots M1&M2




```
Phase margin = 65.1422 Deg at frequency = 36.1282 MHz.
```

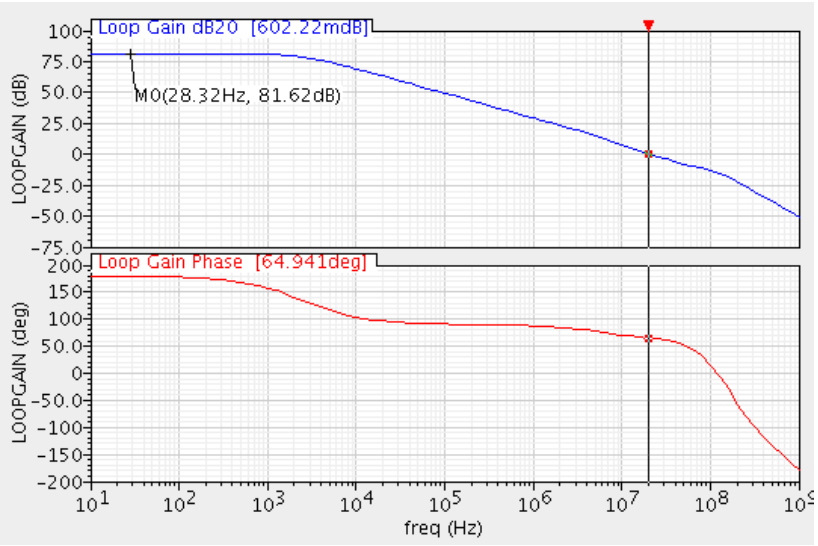
- Differential Mode loop gain and phase margin plots
- Same results obtained by using Method 1 and Method 2

1st Stage CMFB Loop Bode Plots



Phase margin = 64.5059 Deg at frequency = 21.2729 MHz.

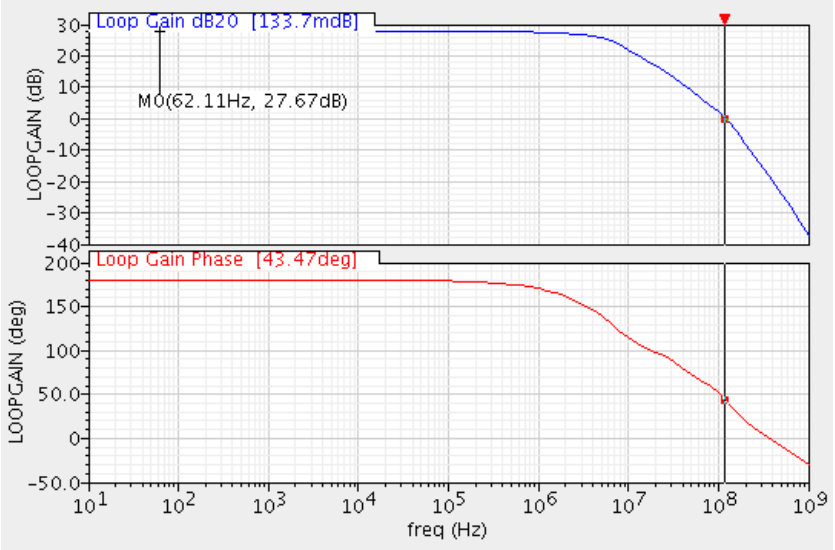
Method 1



Phase margin = 64.5788 Deg at frequency = 21.2722 MHz.

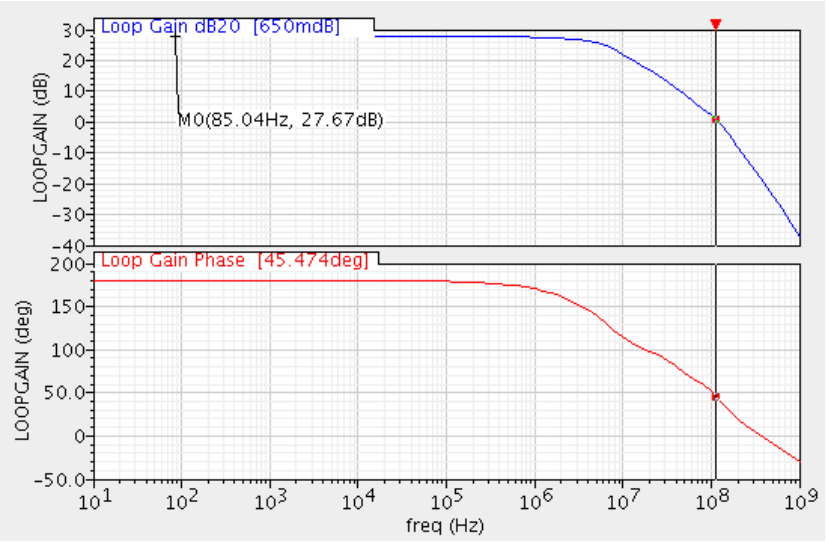
Method 2

2nd Stage CMFB Loop Bode Plots




```
Phase margin = 42.6336 Deg at frequency = 119.604 MHz.
```

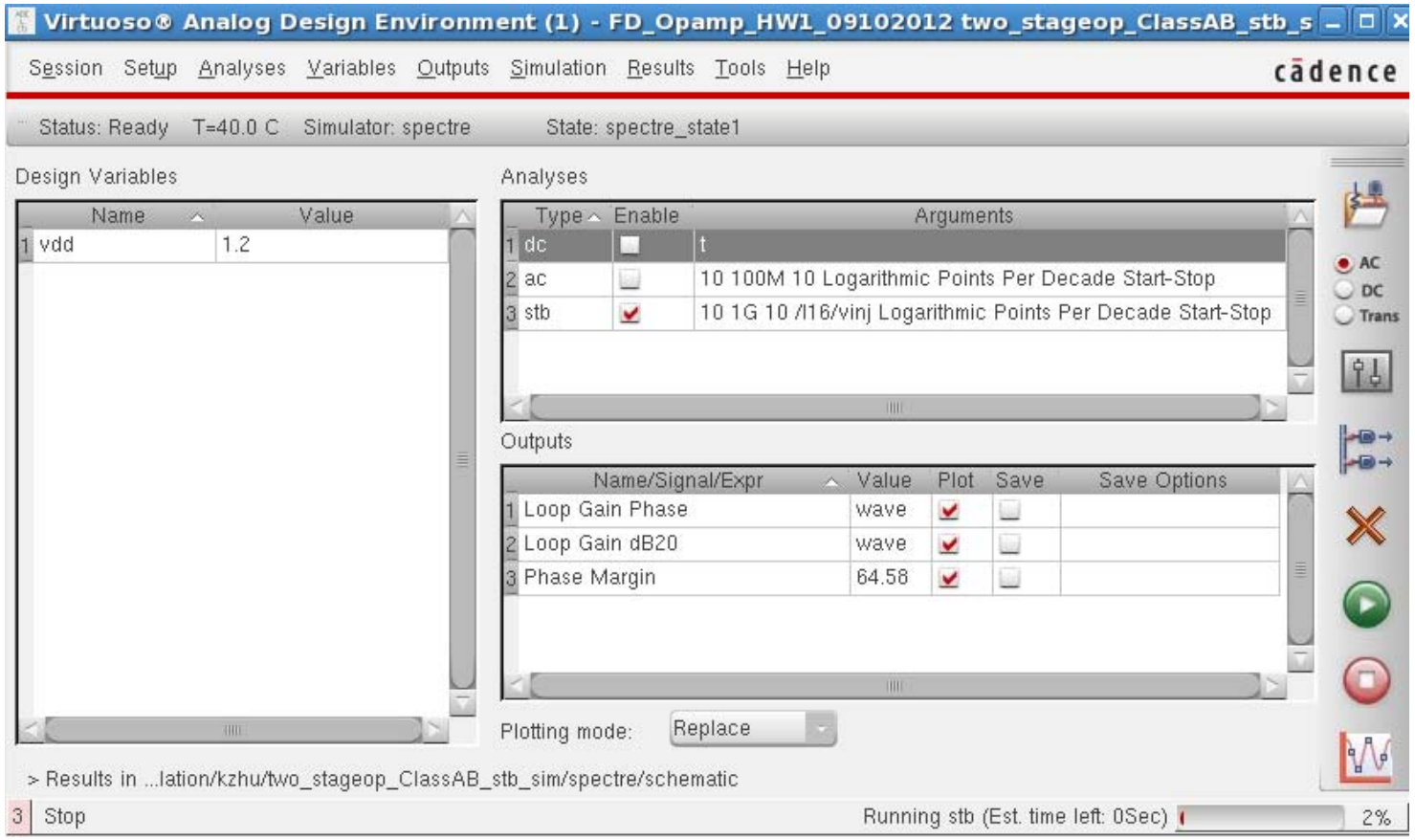
Method 1




```
Phase margin = 42.376 Deg at frequency = 119.867 MHz.
```

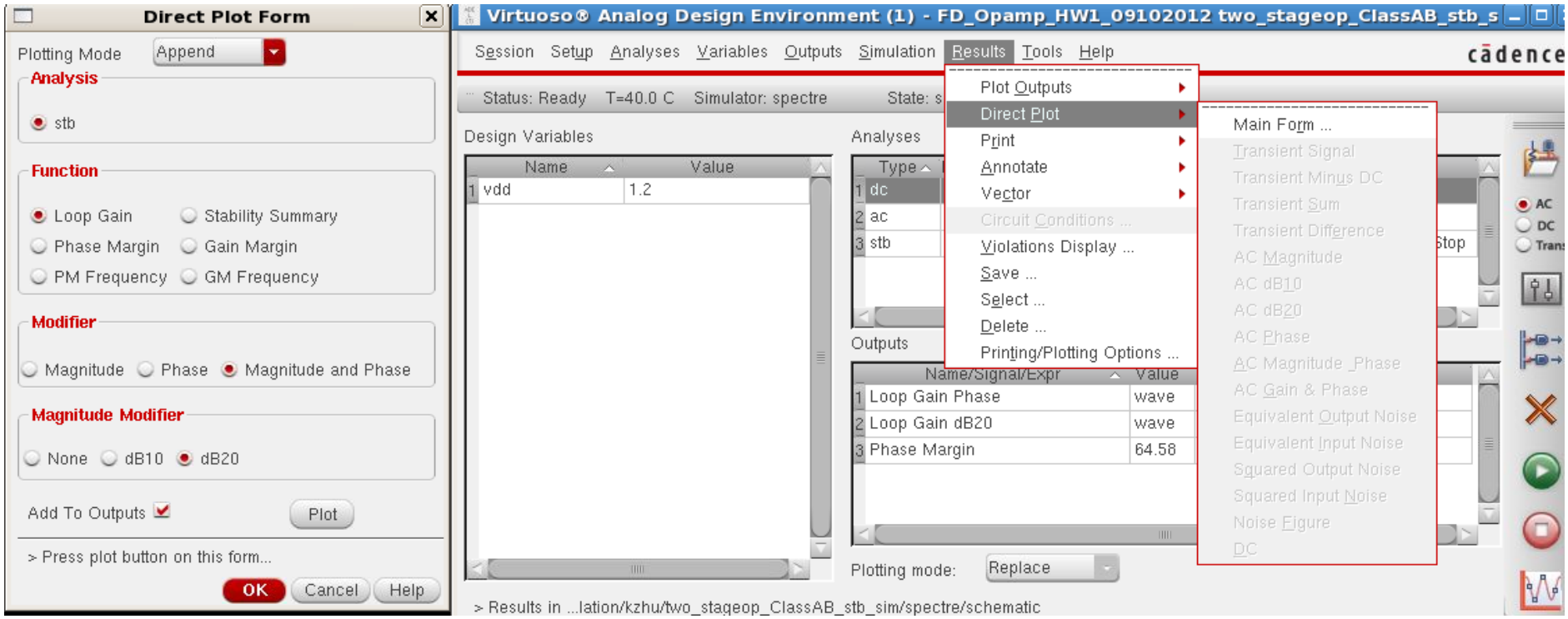
Method 2

Simulation Setup



- Use previous oppt (operating point) in the stb analysis

Bode Plot Setup

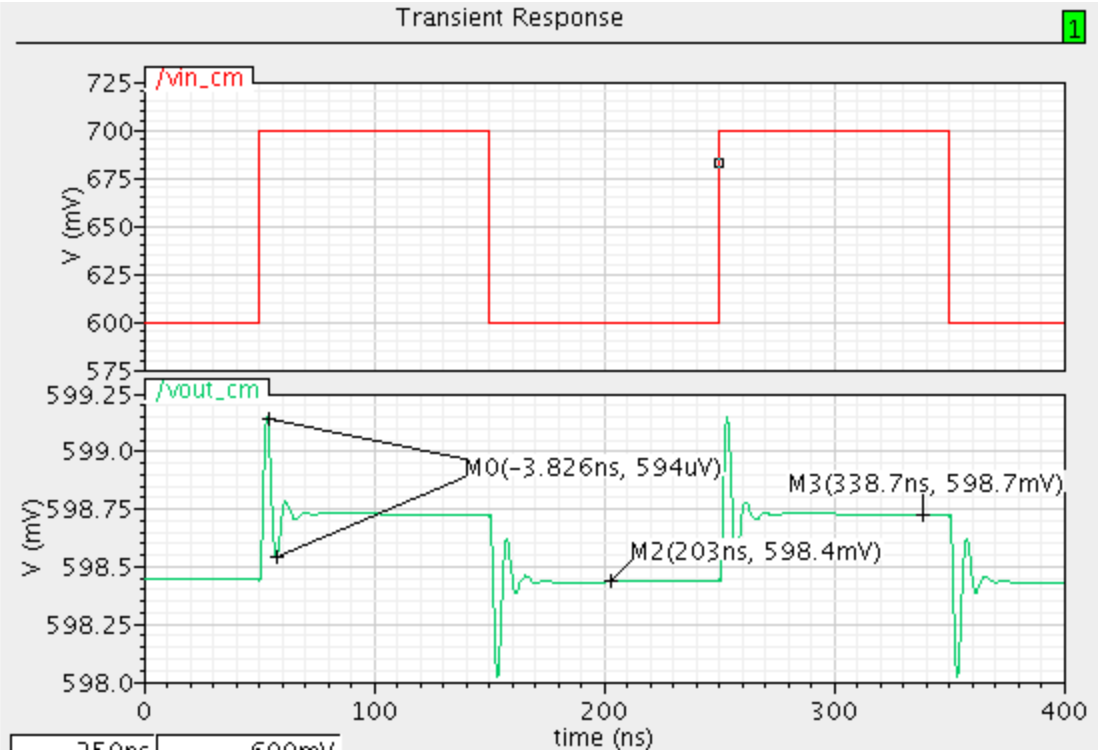


- Results → Direct Plot → Main Form

DM Transient

- Unity- gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse with=100ns)

CM Transient

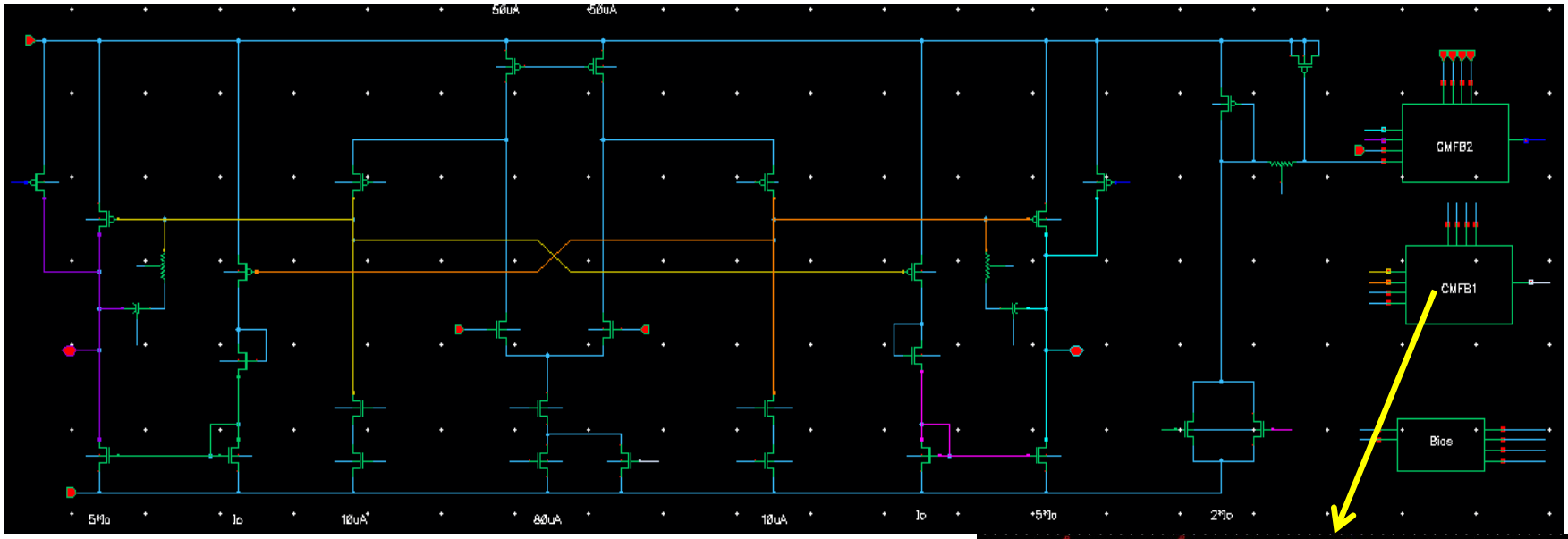


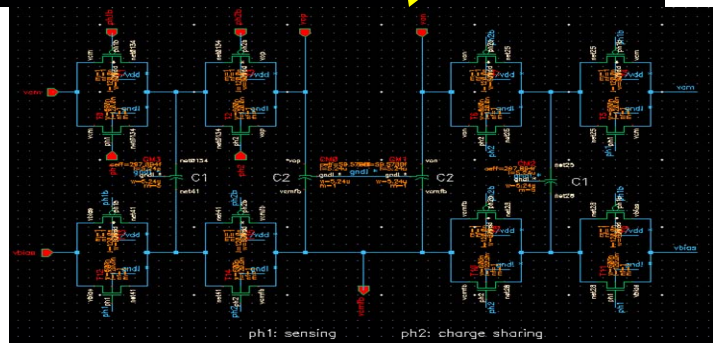
- Unity- gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse with=100ns)

Fully-Differential Opamp Simulation

Switched-capacitor CMFB

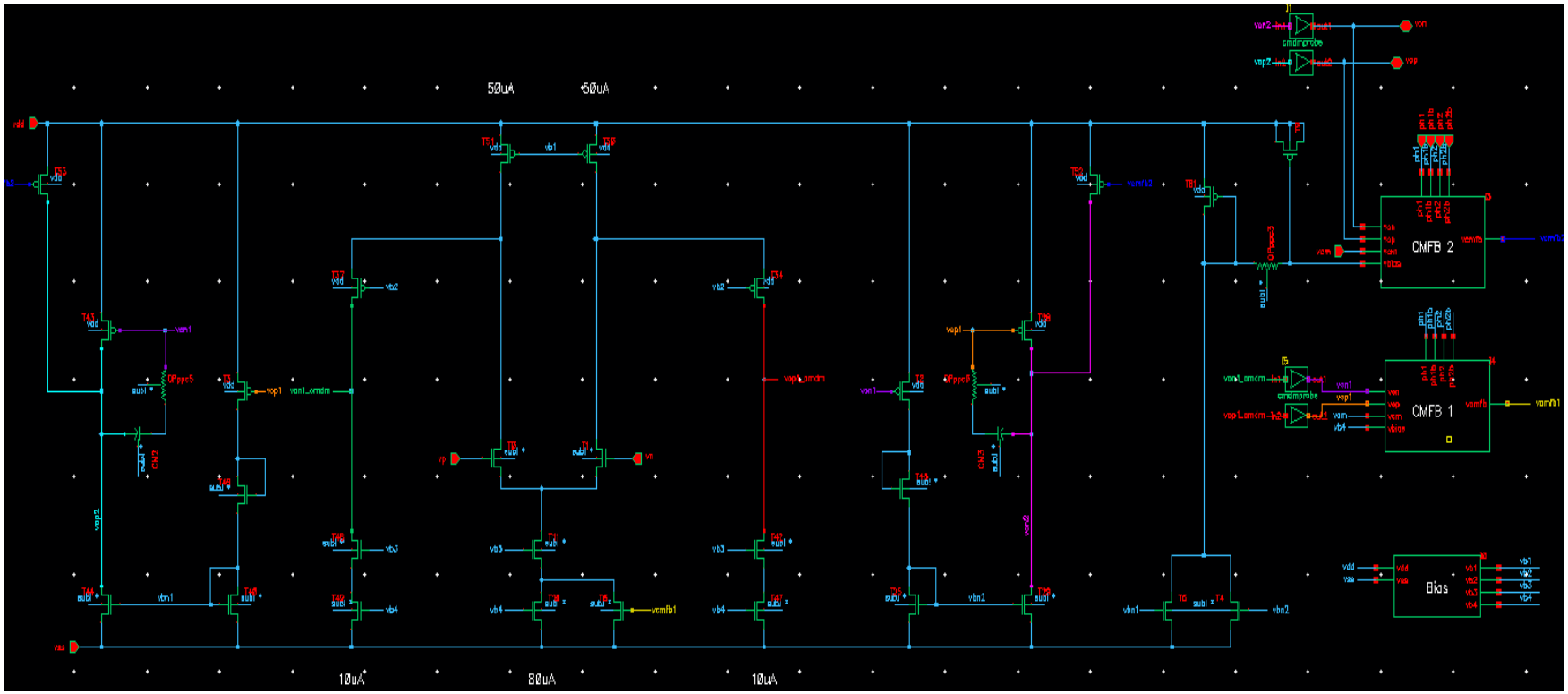
Switched Capacitor CMFB Simulation





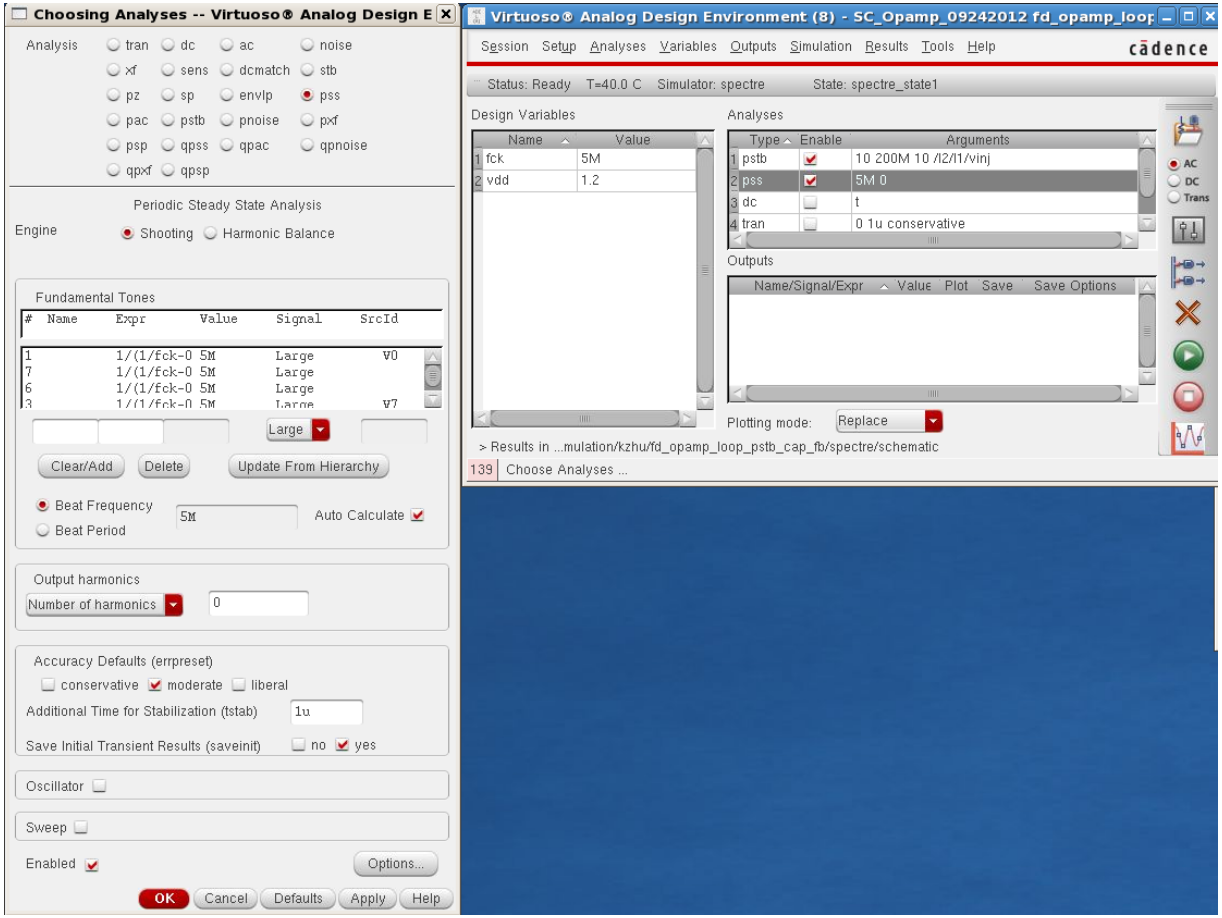
- 2-stage Class AB output Opamp
- Individual SC-CMFB

PSTB Analysis Using Method 1



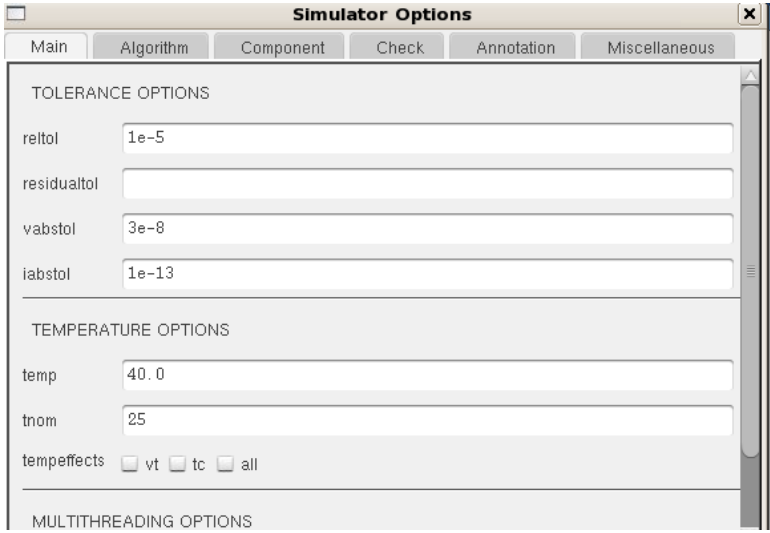
- PSTB analysis is essential for sampled circuit

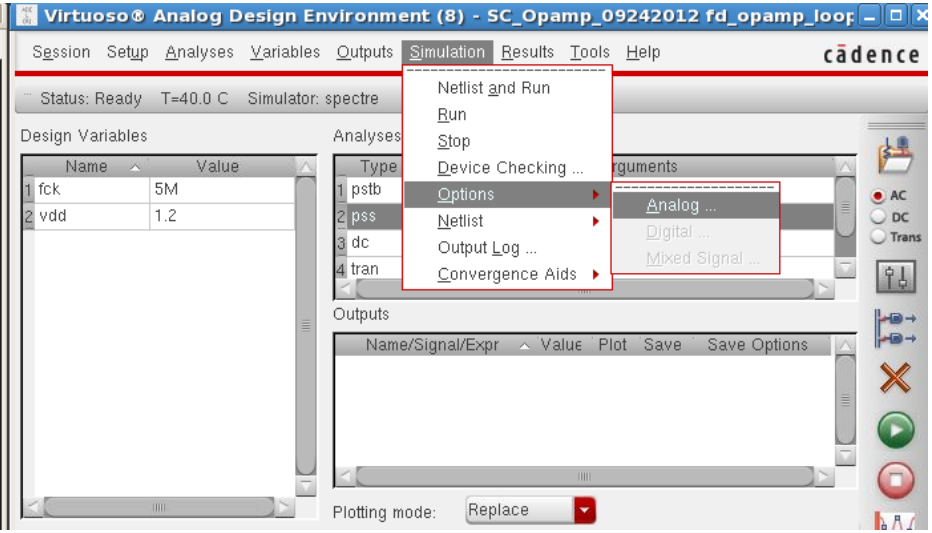
Simulation Setup---PSS



- We can only set the number of harmonics to 0 by choosing Shooting method
- tstab parameter can be obtained by tran analysis first

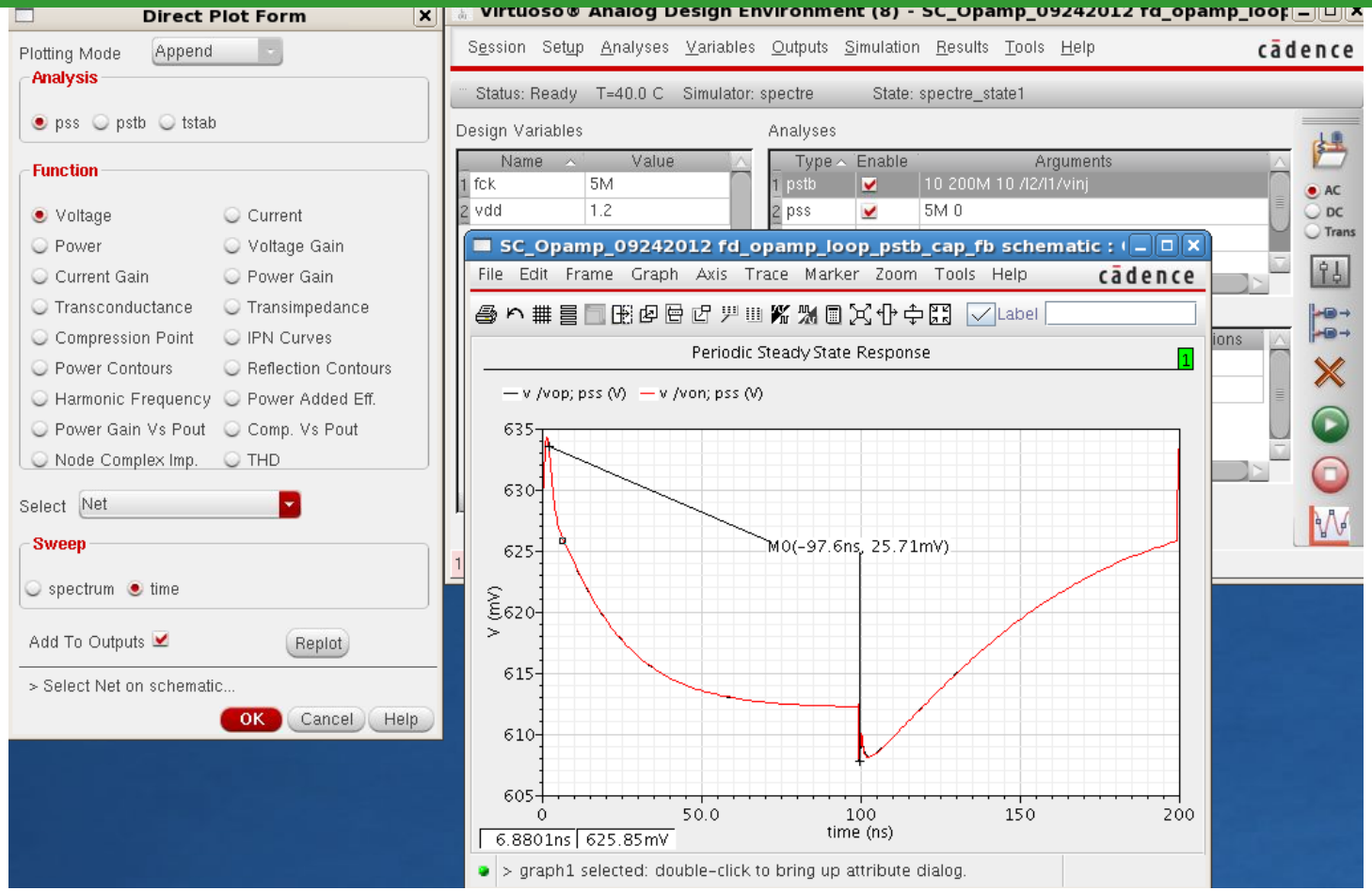
PSS Accuracy suggestions





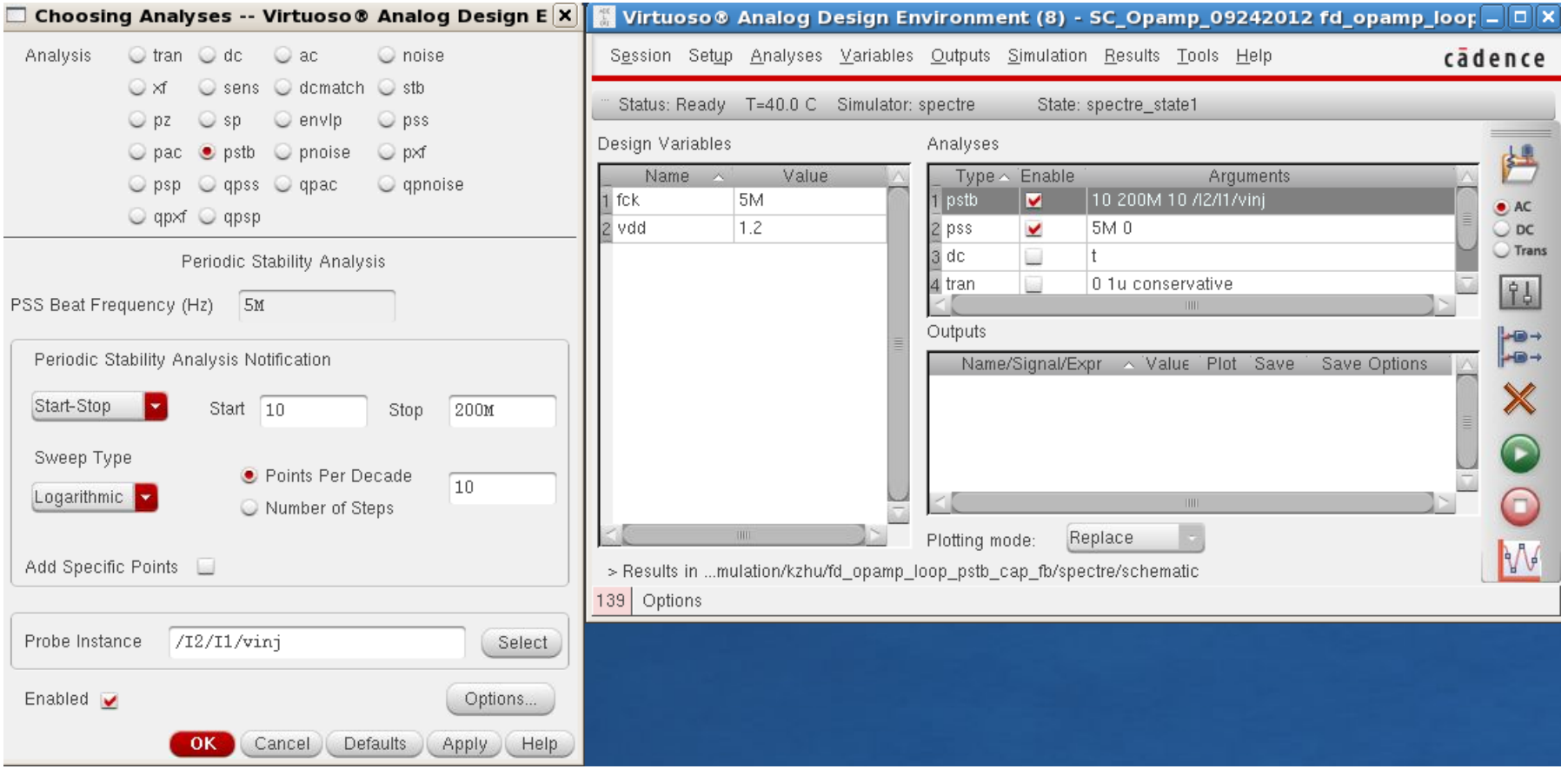
- Go to Simulation →Options→ Analog →Main in the ADE window to setup tolerance options accordingly. If the frequency of periodic small signal analyses followed by PSS is high (e.g. 1G), the *maxacfreq* parameter (options→accuracy) of the PSS can be used to specify the highest frequency, otherwise, the frequency analysis in PAC maybe truncated.

PSS Time Plot



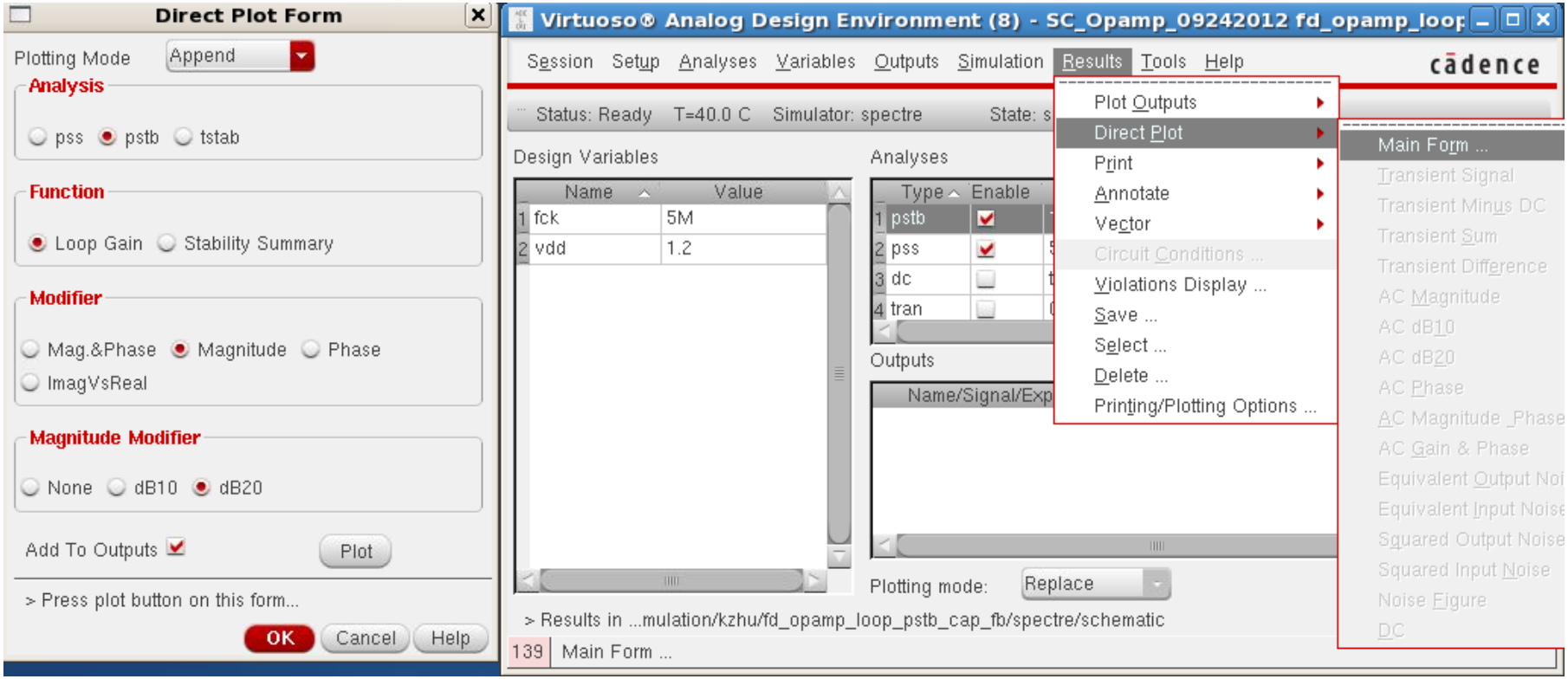
- Results ⟶ Direct Plot ⟶ Main Form
- X-axis scale range is 1/sampling clock frequency

PSTB Setup



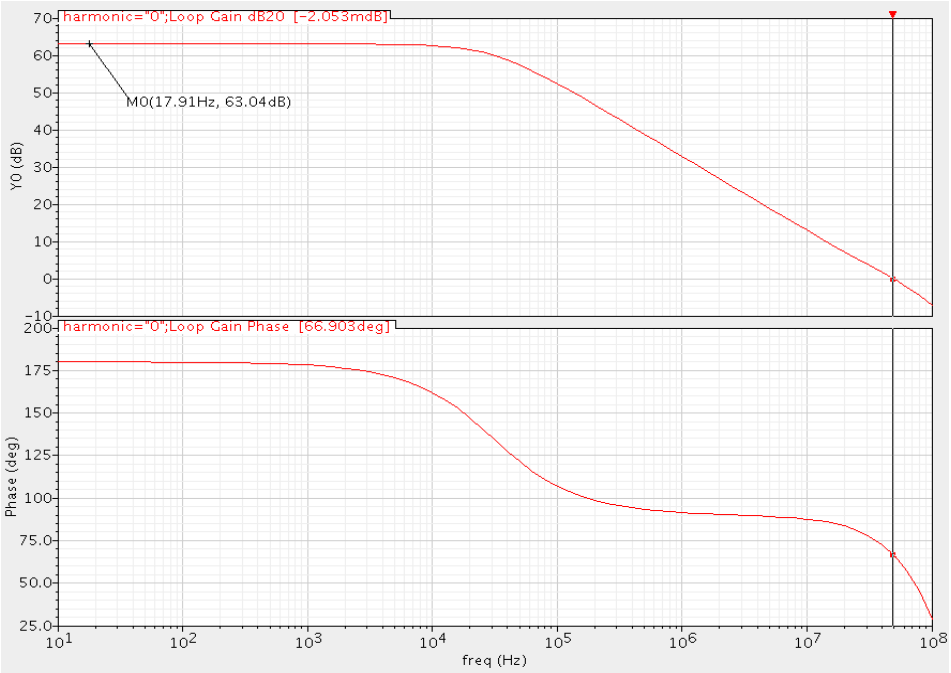
- PSTB is always followed by PSS

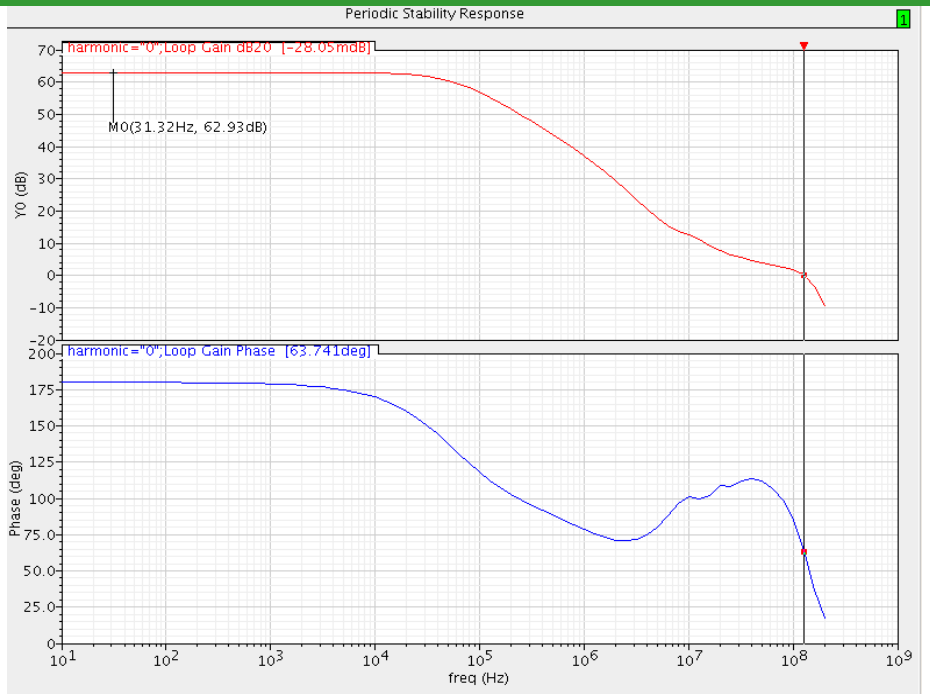
PSTB Plot



- Results → Direct Plot → Main Form

DM Loop Bode Plots






```
Phase margin = 67.0107 Deg at frequency = 48.633 MHz.
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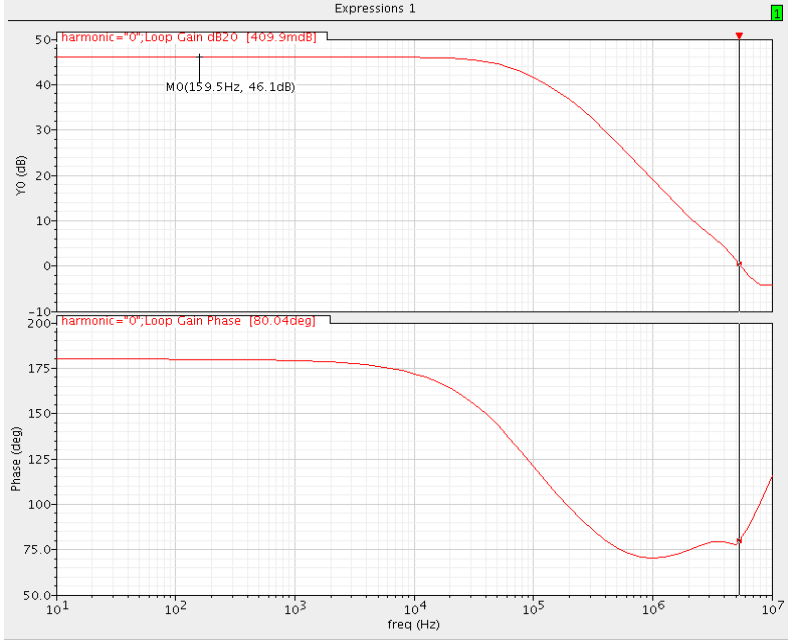
```
Phase margin = 64.0631 Deg at frequency = 125.724 MHz.
```

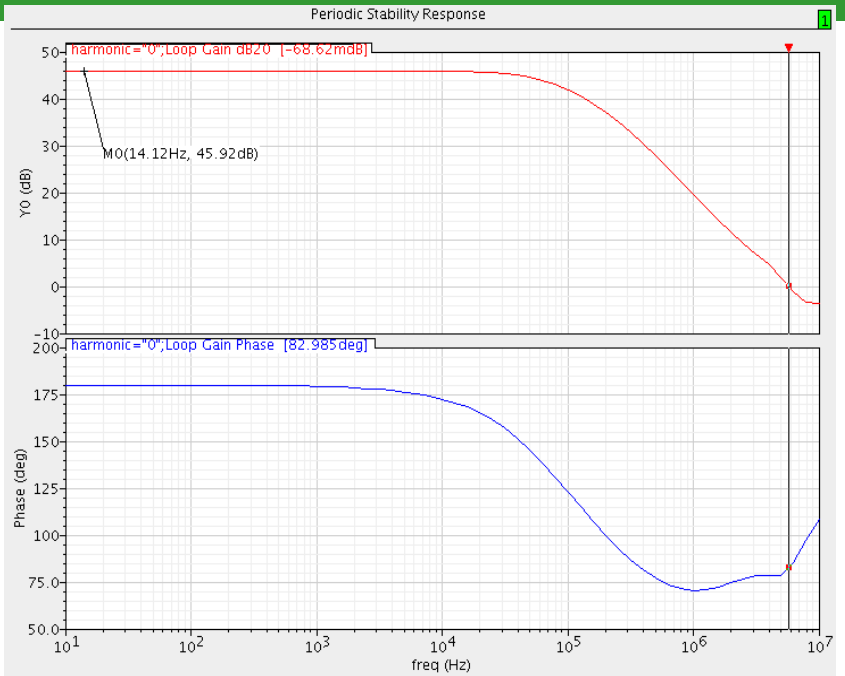
Resistive feedback

Capacitive feedback

1st Stage CMFB Loop Bode Plots



Phase margin = 79.0094 Deg at frequency = 5.36771 MHz.

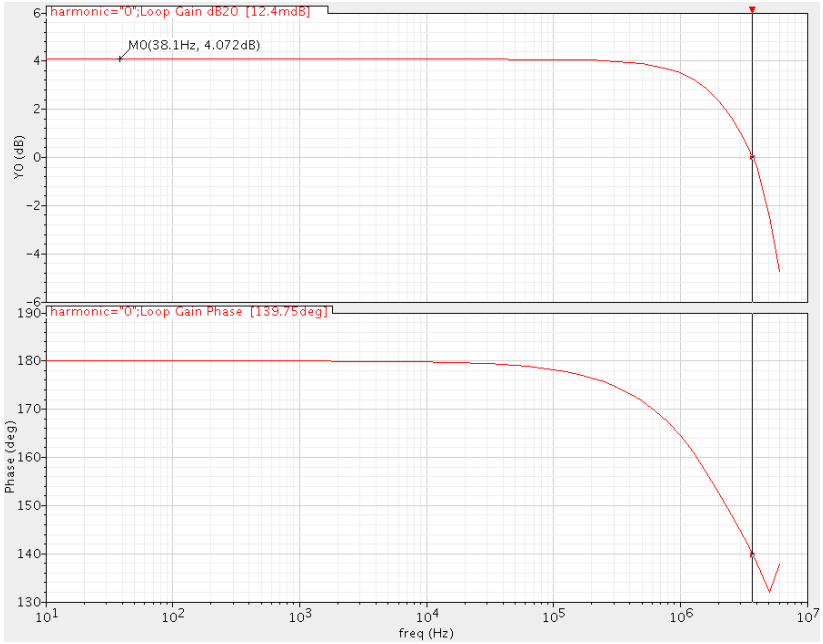


Phase margin = 84.622 Deg at frequency = 6.17596 MHz.

Resistive feedback

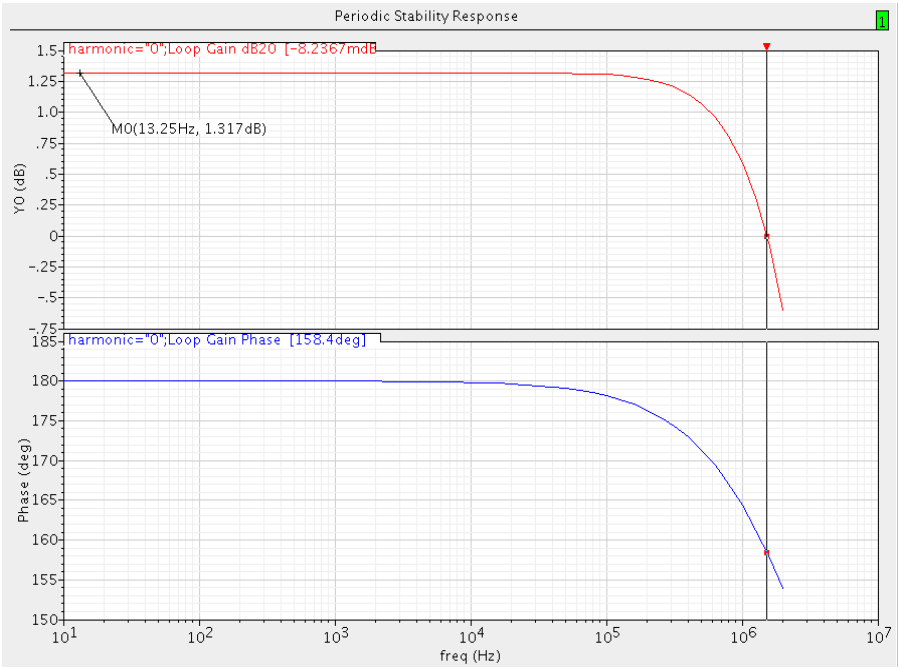
Capacitive feedback

2nd Stage CMFB Loop Bode Plots



Phase margin = 139.738 Deg at frequency = 3.73402 MHz.

Resistive feedback



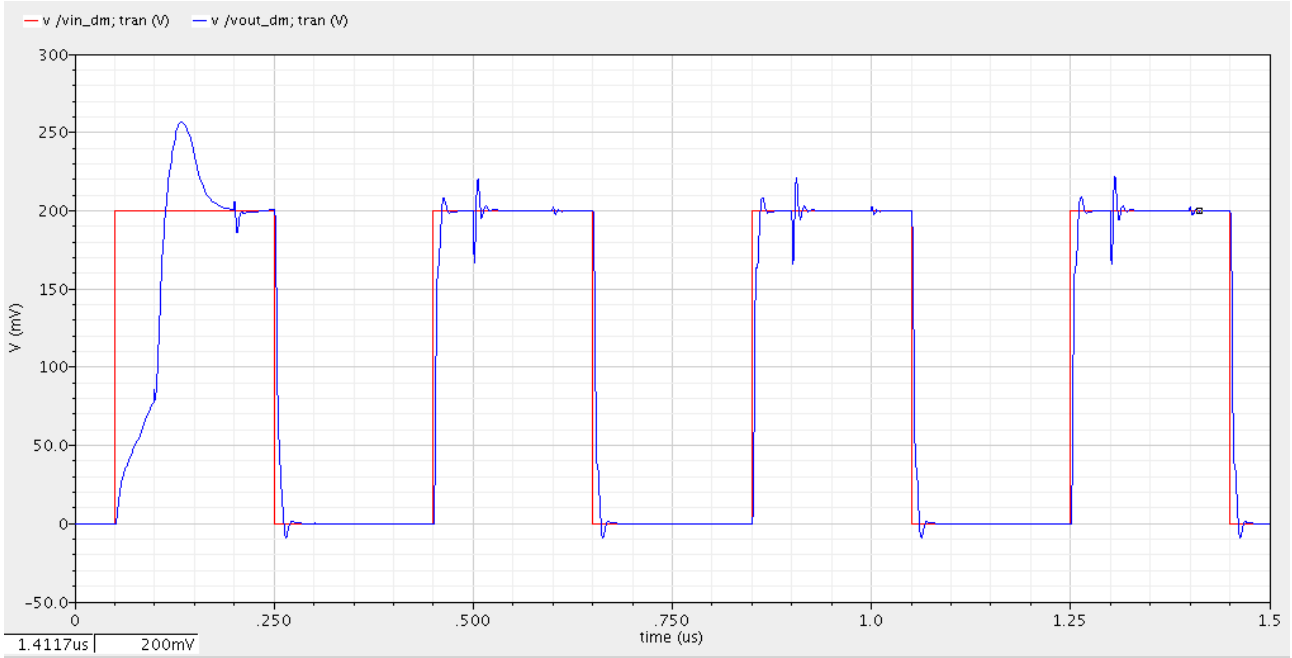
Phase margin = 158.414 Deg at frequency = 1.51941 MHz.

Capacitive feedback

Summary of pstb analysis

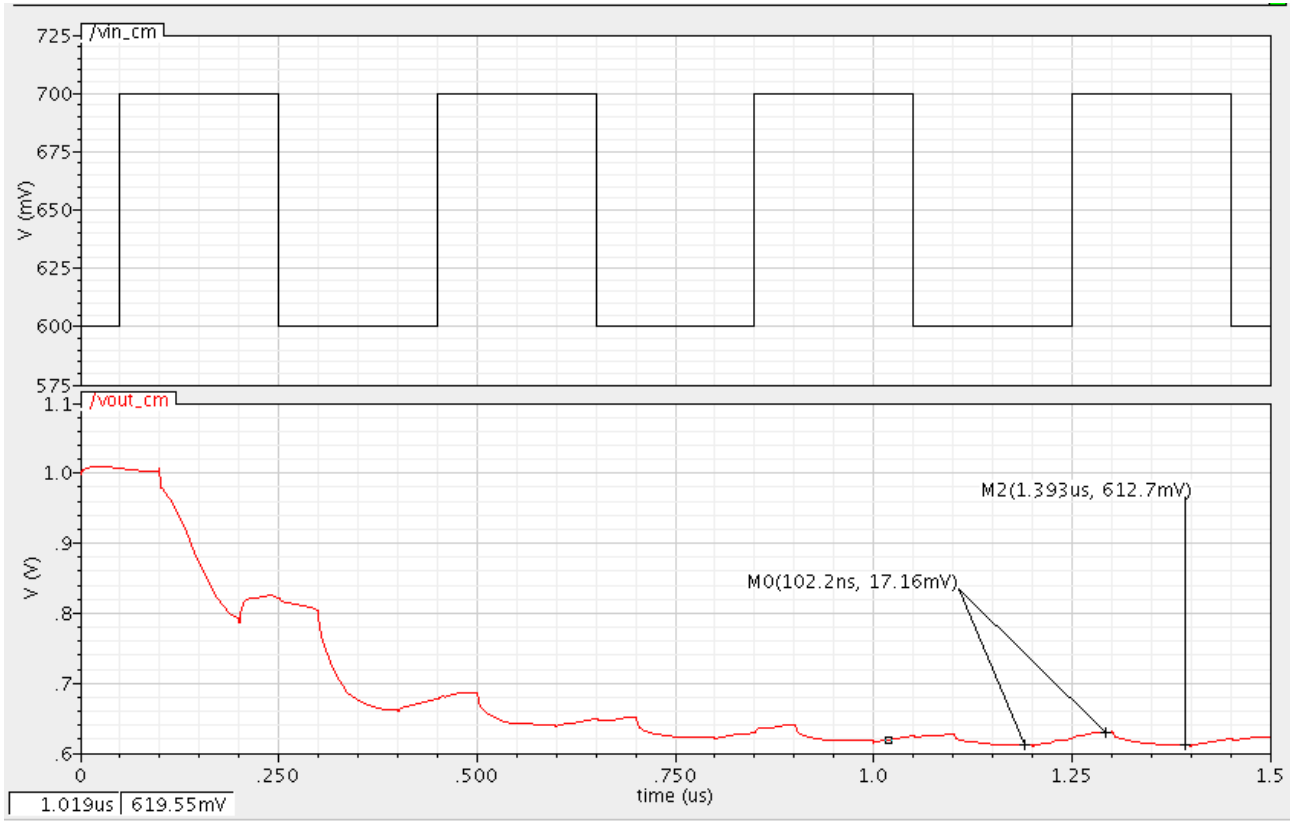
Application	Items	DC Gain (dB)	PM (°)	GBW (MHz)
Sample hold	1st stage CMFB	45.9	84.6	6.1
	2nd stage CMFB	1.31	158.4	1.5
	DM loop	62.9	64.1	125
Resistive feedback	1st stage CMFB	46.1	79	5.3
	2nd stage CMFB	4.1	139.7	3.7
	DM loop	63	67	48.6

Resistive Feedback DM Transient



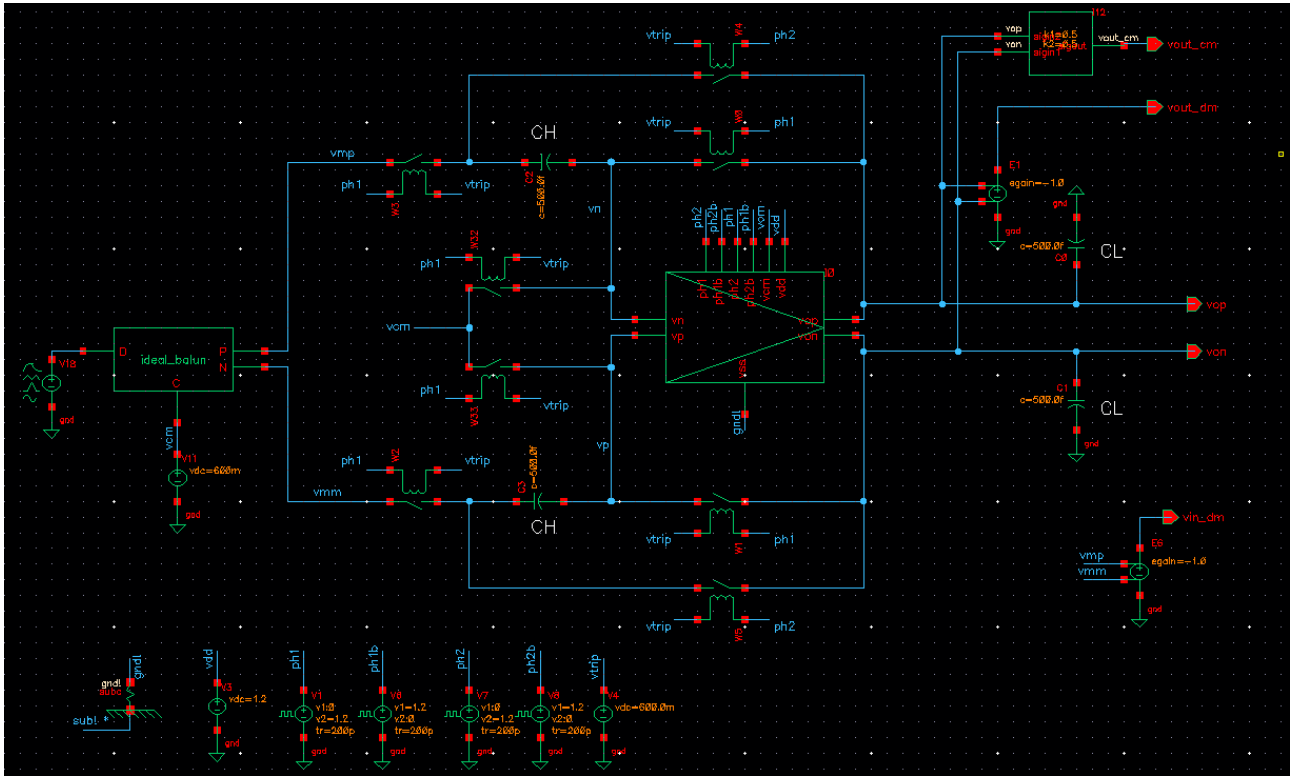
- Unity- gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse with=200ns)

Resistive Feedback CM Transient



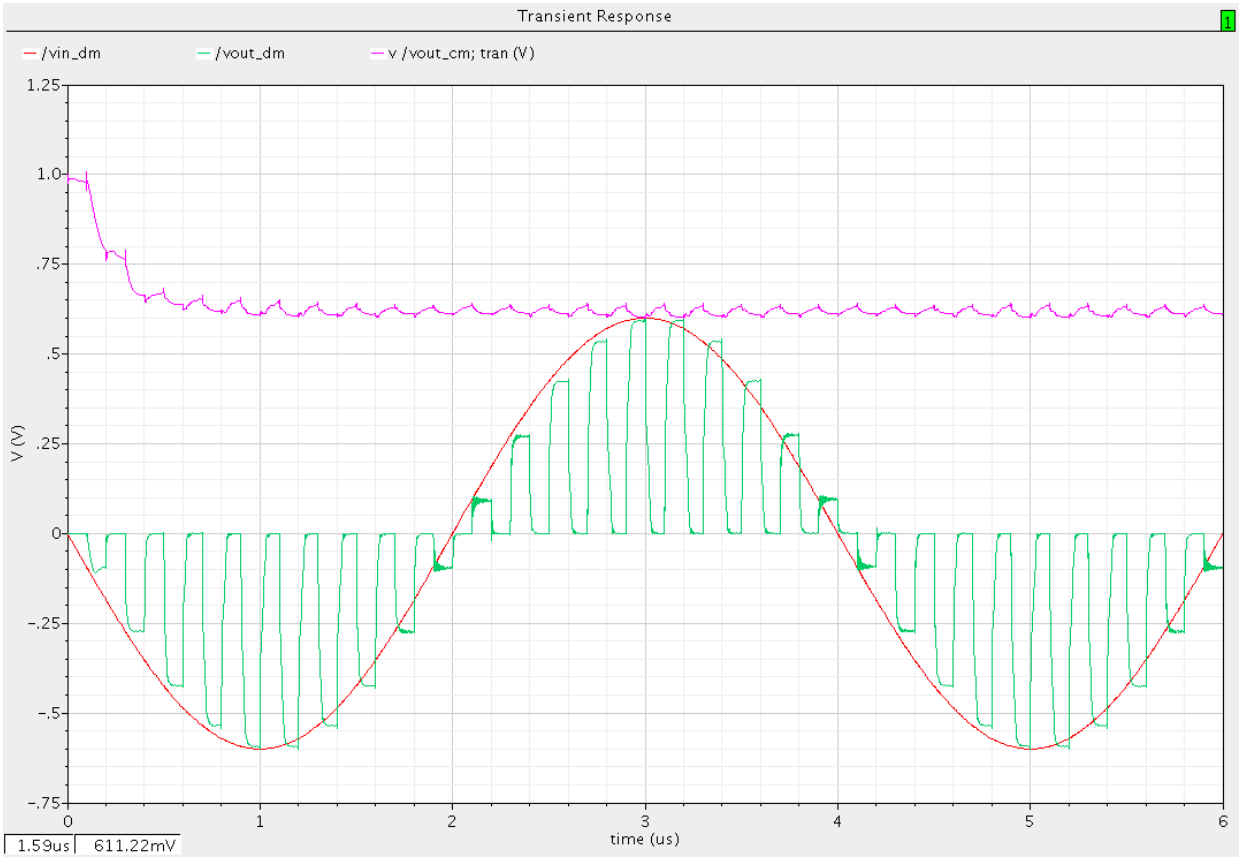
- Unity- gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse with=200ns)

Sample-Hold Configuration



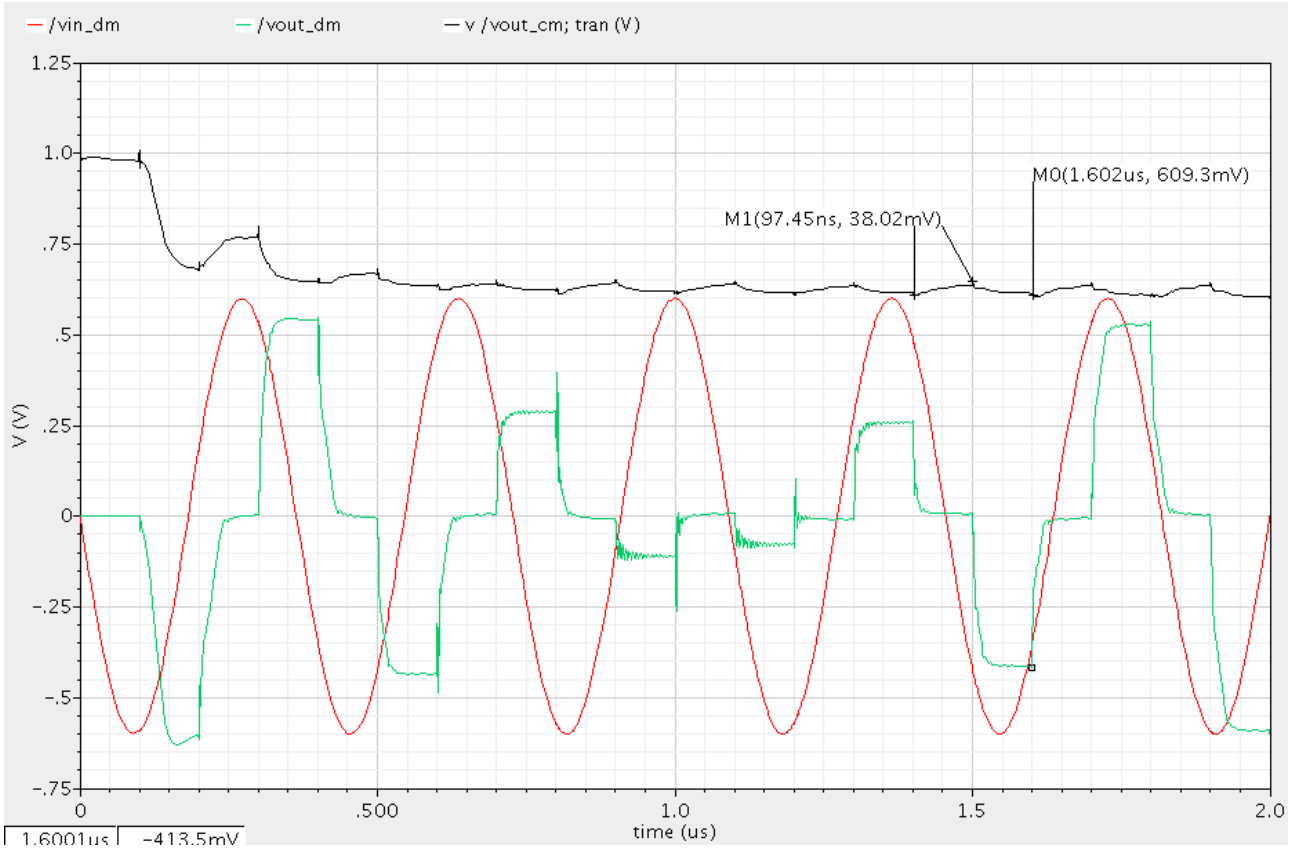
- Ideal switches with on resistance of 1kΩ

Sample-Hold Transient Response



- **DM and CM outputs waveforms when fin=1/4 MHz, fs=5MHz**

Sample-Hold Transient Response



- **DM and CM outputs waveforms when fin=11/4 MHz, fs=5MHz**

References

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[3] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, “Analog and Design of Analog Integrated Circuits,” 4th Ed., Wiley, 2010.

[4] F. Wiedmann, “Loop gain simulation,” Online: https://sites.google.com/site/frankwiedmann/loopgain