# Flash ADCs

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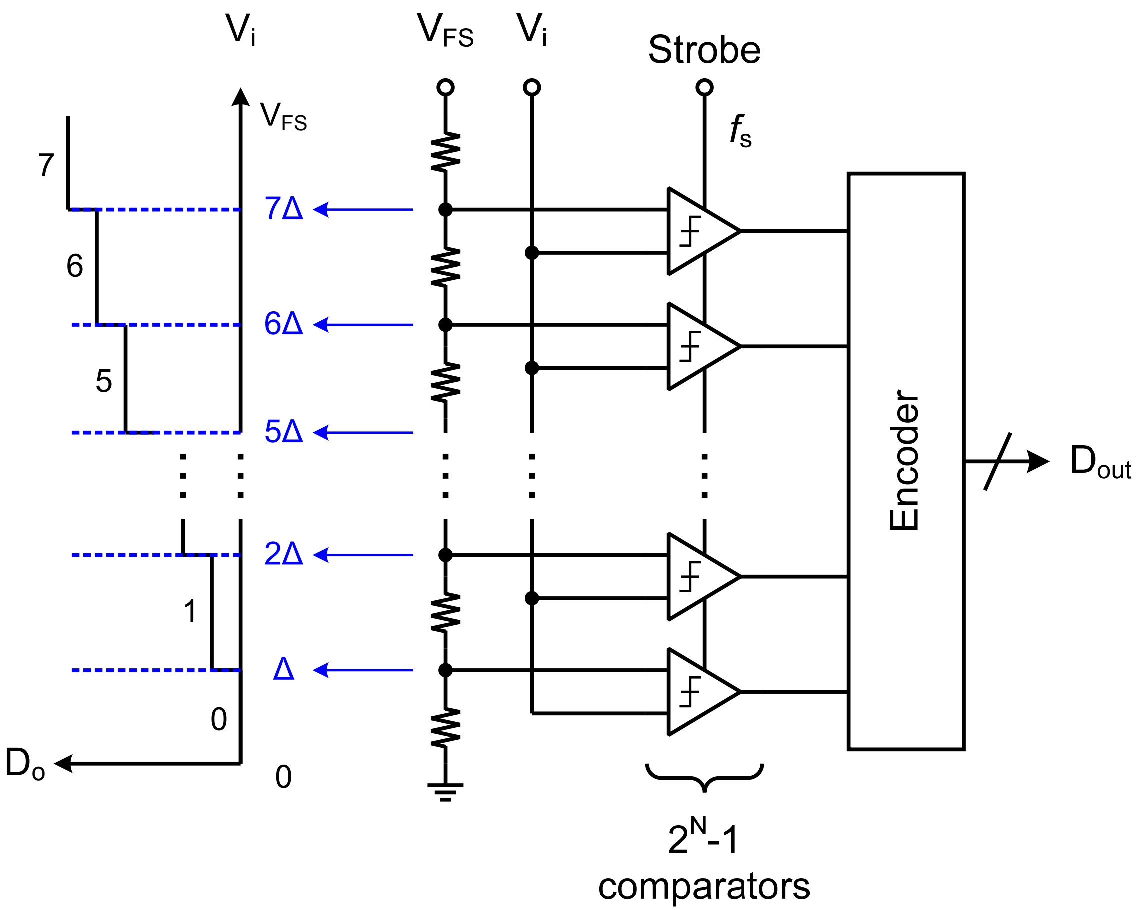
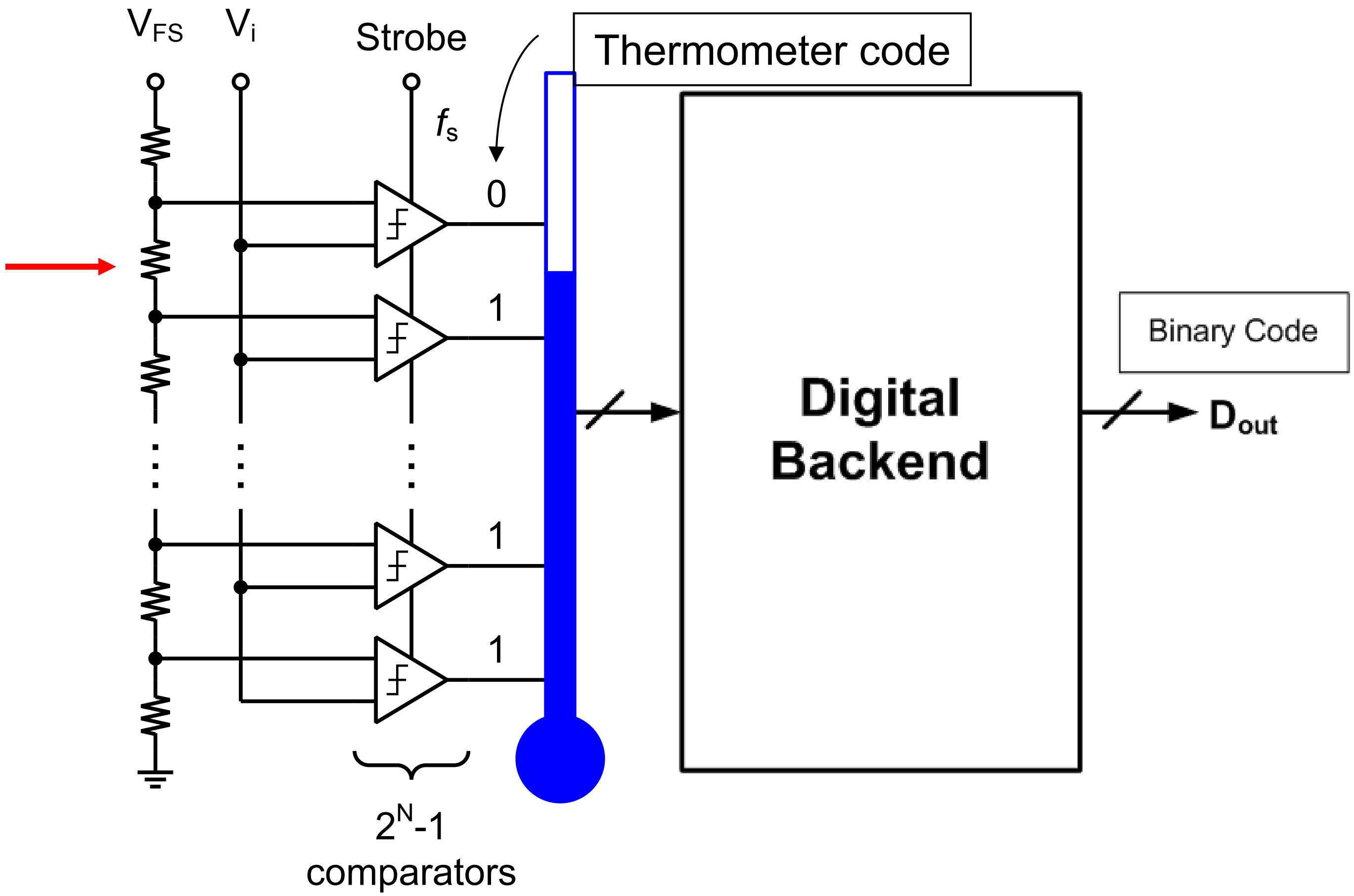
# Flash ADC Architecture

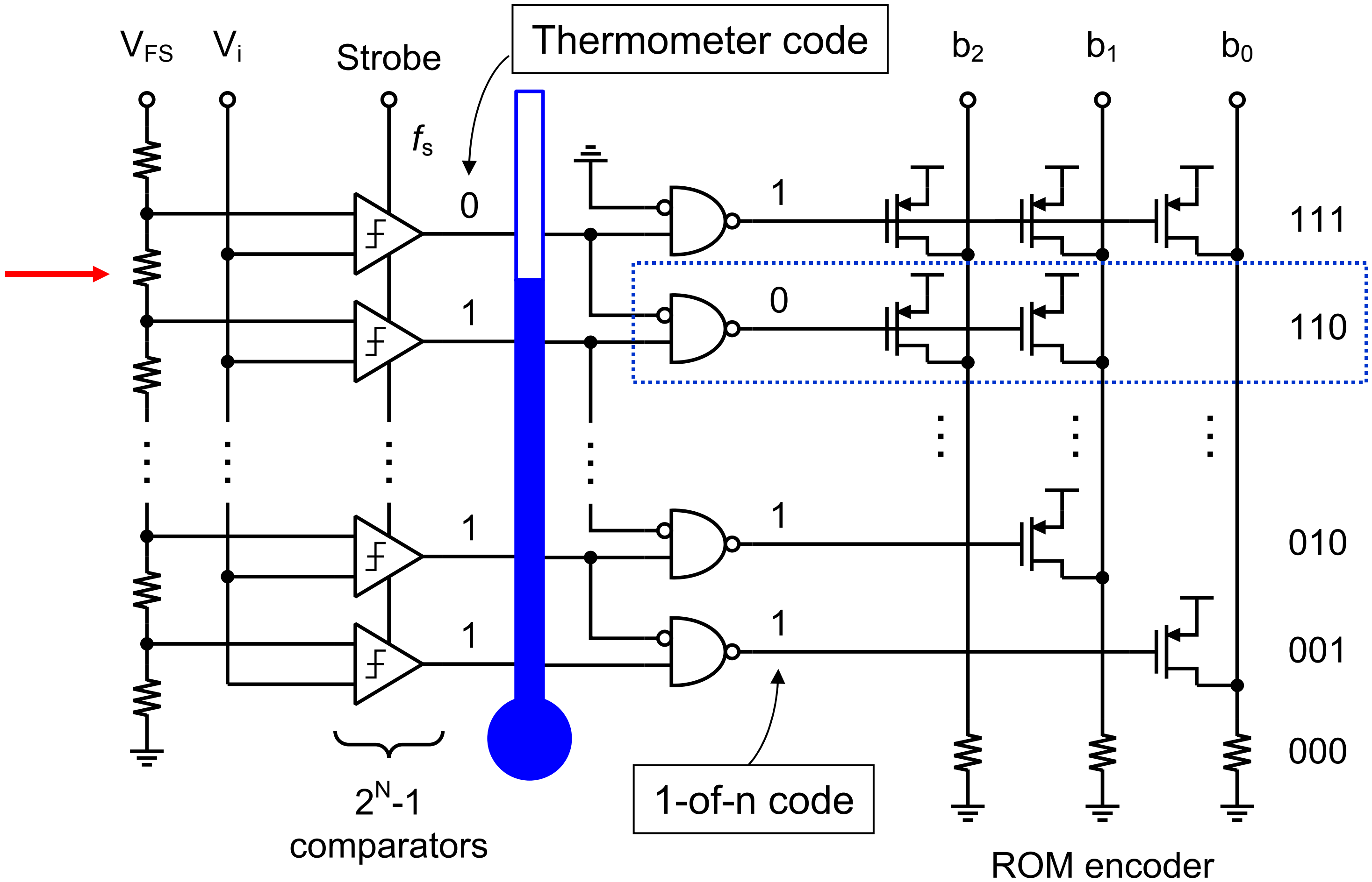



- Reference ladder consists of $2^N$ equal size resistors
- Input is compared to $2^N$-1 reference voltages
- Massive parallelism
- Very fast ADC architecture
- Latency = 1 $T_s$ = $1/f_s$
- Throughput = $f_s$
- Complexity = $2^N$

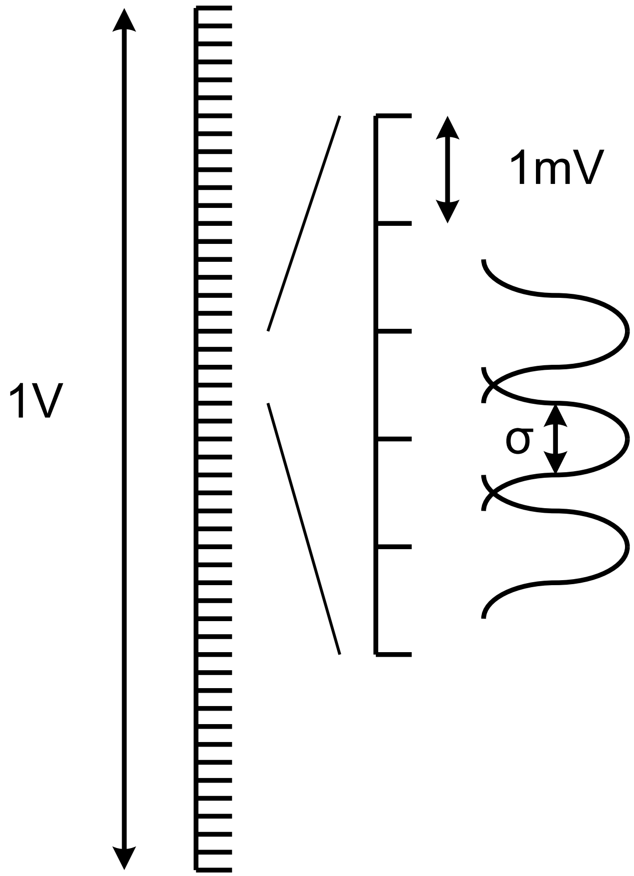
# Thermometer Code



# Thermometer Code



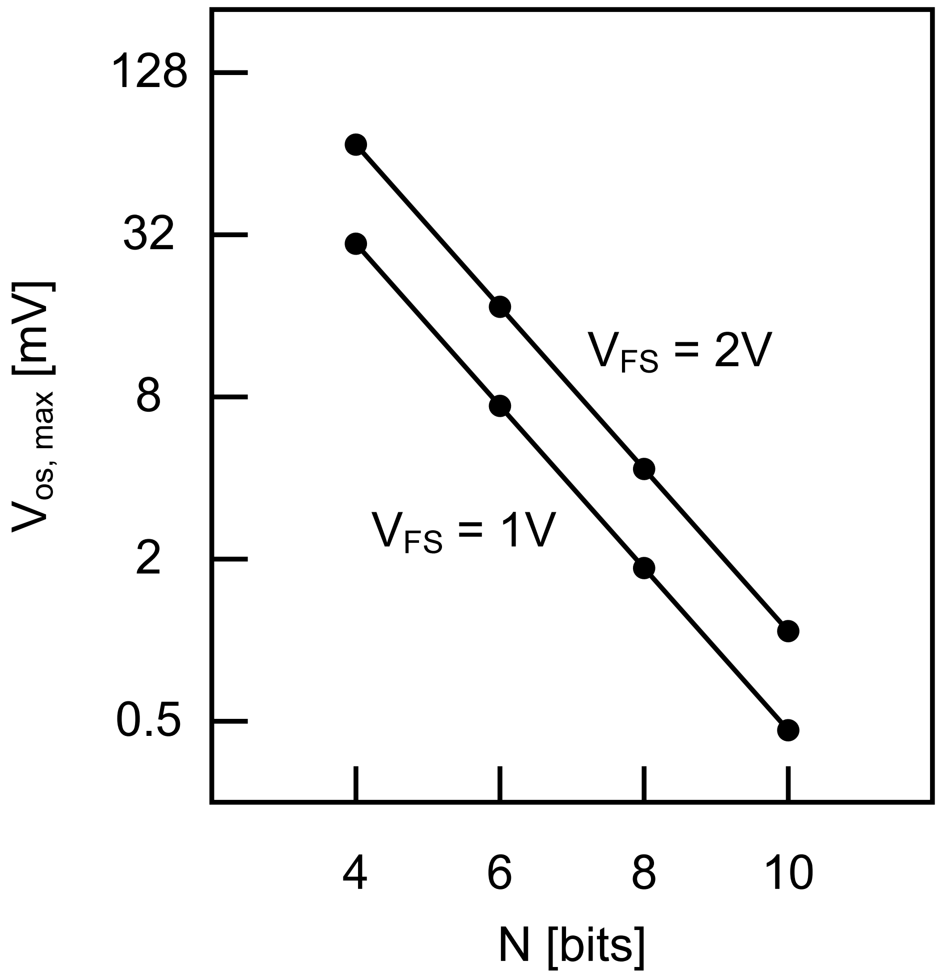
# Flash ADC Challenges




- $V_{DD}$ = 1.8 V
- 10-bit → 1023 comparators
- $V_{FS}$ = 1 V → 1 LSB = 1 mV
- DNL < 0.5 LSB → $V_{os}$ < 0.5 LSB
- 0.5 mV = 3-5 σ → σ = 0.1-0.2 mV

- $2^N$-1 very large comparators
- Large area, large power consumption
- Very sensitive design
- Limited to resolutions of 4-8 bits

# Flash ADC Challenges




- DNL < 0.5 LSB
- Large $V_{FS}$ relaxes offset tolerance
- Small $V_{FS}$ benefits conversion speed (settling, linearity of building blocks)

# ADC Input Capacitance

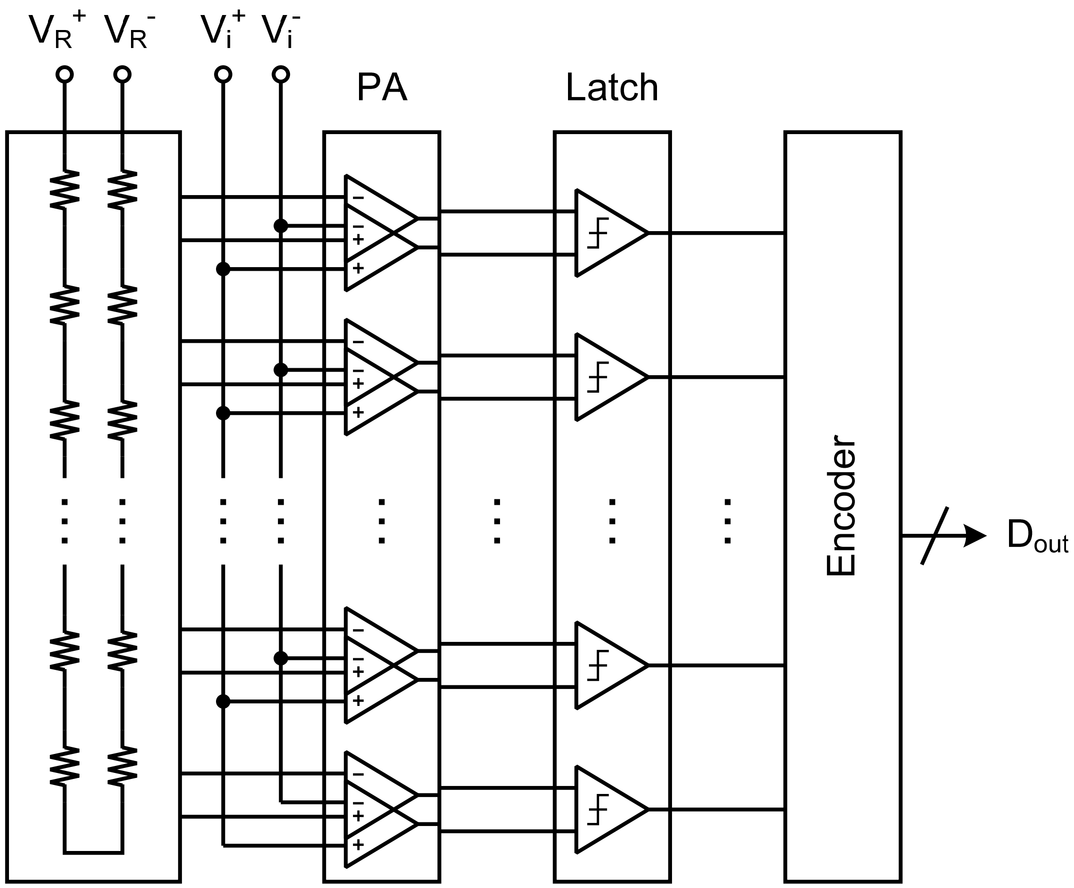
$$\sigma^2(V_{th}) = \frac{A_{Vth}^{\ 2}}{WL} \qquad C_g = 10\ \text{fF}/\mu\text{m}^2$$

- N = 6 bits → 63 comparators
- $V_{FS}$ = 1 V → 1 LSB = 16 mV
- σ = LSB/4 → σ = 4 mV
- $A_{VT0}$ = 10 mV·µm → L = 0.24 µm, W = 26 µm

| N (bits) | # of comp. | $C_{in}$ (pF) |
|---|---|---|
| 6 | 63 | 3.9 |
| 8 | 255 | 250 |
| 10 | 1023 | ??! |

- Small $V_{os}$ leads to large device sizes, hence large area and power
- Large comparator leads to large input capacitance, difficult to drive and difficult to maintain tracking bandwidth

# Fully-Differential Architecture

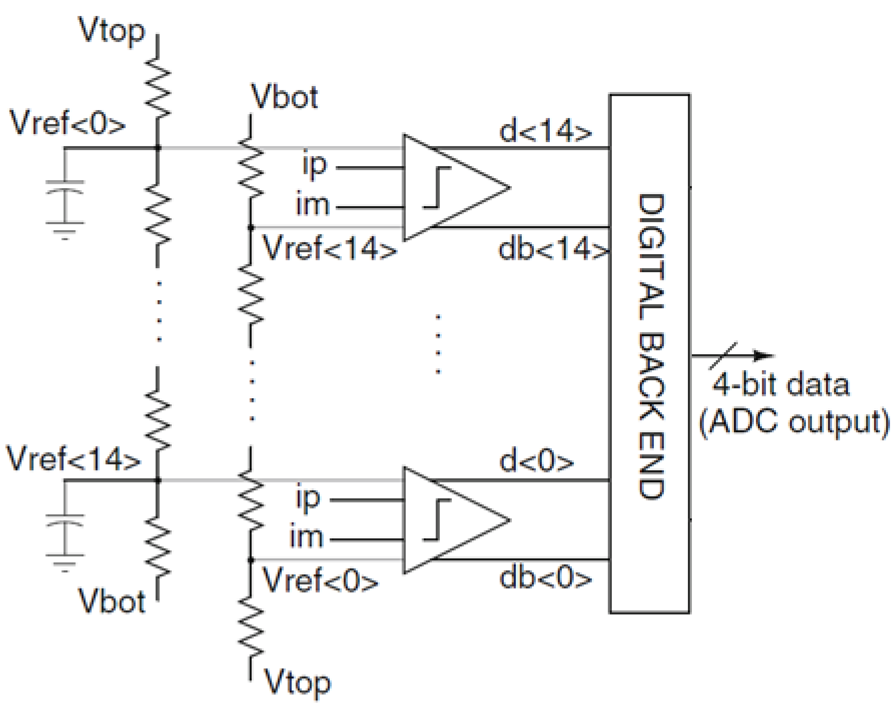



- $V_{FS}$ doubled
- 3-dB gain in SNR
- Better CMRR
- Noise immunity
- Input feedthrough cancelled
- $C_{in}$ nonlinearity partially removed
- Effect of $V_{cmi}$ diff. mitigated

# Flash ADC Design Considerations

- Use a dedicated S/H (or T/H) for better dynamic performance
  - Can be avoided when using the A/D inside a $\Delta\Sigma$ loop
- Large input range for the quantizer has several benefits
  - Increased step-size ($V_{LSB}$) relaxes offset requirements on the comparators
  - Reduced matching requirements result in small input cap to the S/H, easier to drive
  - Reduced input cap results in smaller clock routing parasitics – power savings in clock drivers
- Comparator Design
  - See comparator design slides

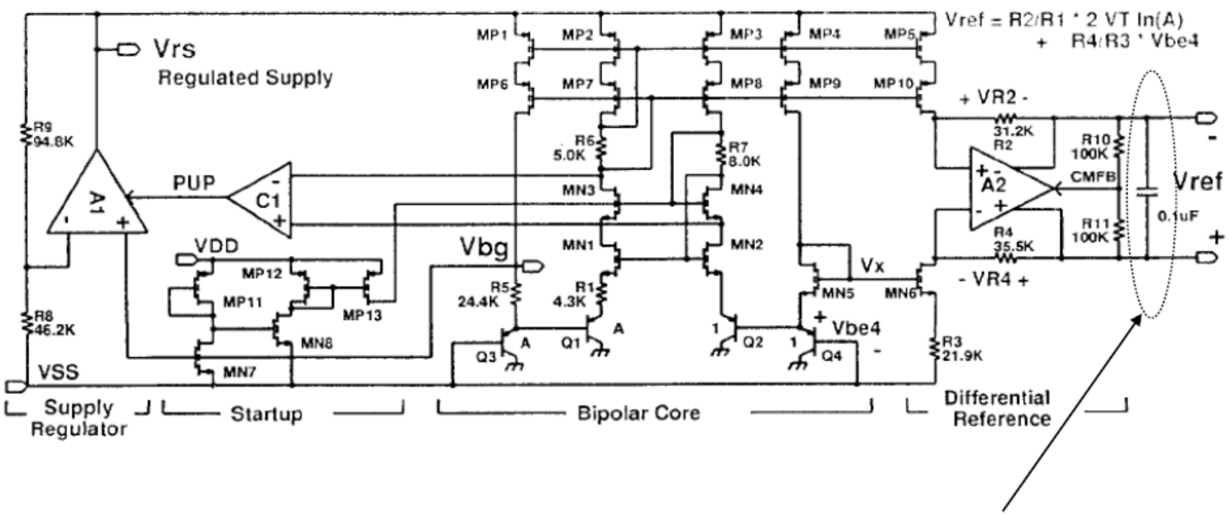
# Flash ADC: Reference Ladder



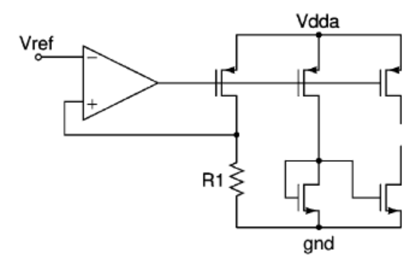

- Differential reference ladder
- Decaps on the reference taps
  - large *RC* time-constant will not allow reference restoration after kickback noise
  - Small *R* will lead to power dissipation
  - Optimize *RC*
- Subtract references from the input in a differential manner
  - Several topologies
- Several architectures for the digital backend
  - May need to pipeline digital logic at high sampling rates >500 MS/s

# Reference Generator (for $V_{refp}$ and $V_{refm}$)

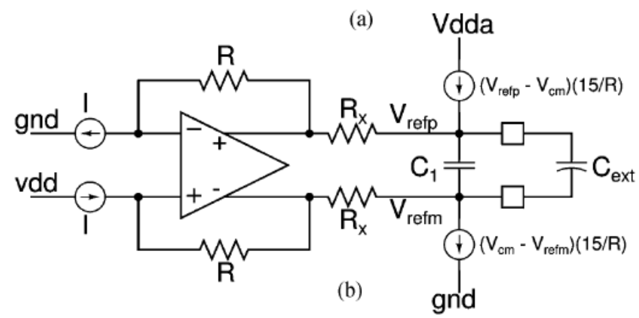
[Brooks 1994]




External decoupling caps provide dynamic currents
⇒ Low power reference buffer



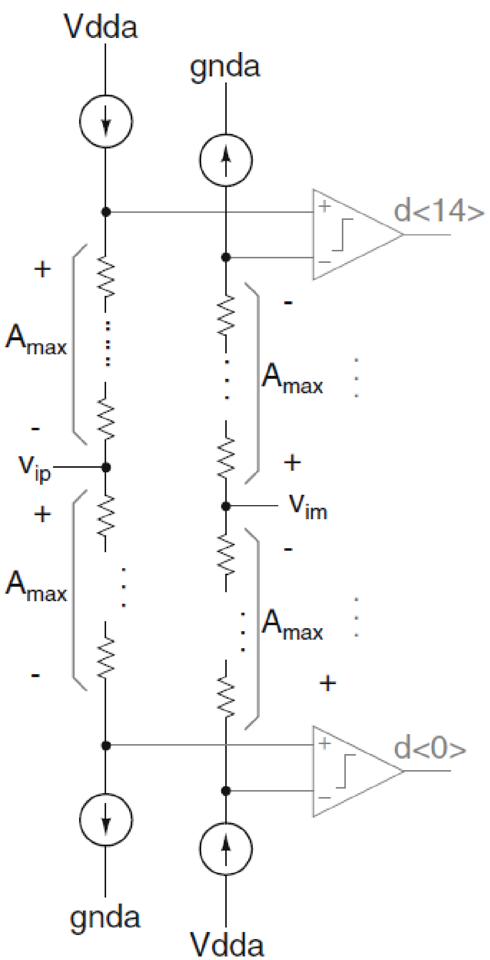
(a)



(b)

# Flash ADC: Reference Subtraction

# Reference Subtraction: Scheme I

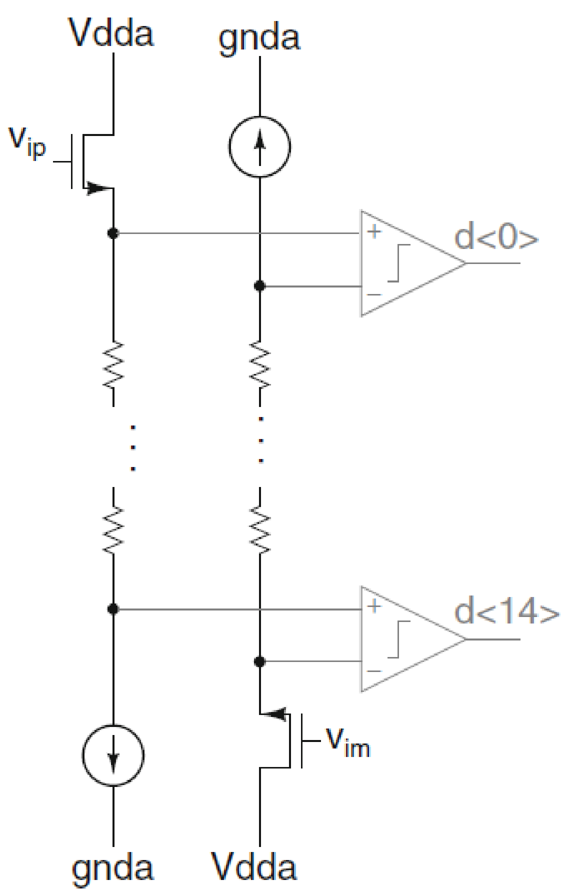



- Employ reference ladder for subtraction
- Choose current (*I*) such that differential voltage drop across R = 1 $V_{LSB}$
- Ladder is part of the signal path
  - Comparator input cap load the resistor taps
  - Excess delay

$$A_{max} = \frac{0.5V_{dd} - \Delta V}{2}$$


Paton, S., Di Giandomenico, A., Hernandez, L., Wiesbauer, A., Potscher, T., & Clara, M. (2004). A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 bits of resolution. *IEEE Journal of Solid State Circuits, 39*(7), 1056–1063.

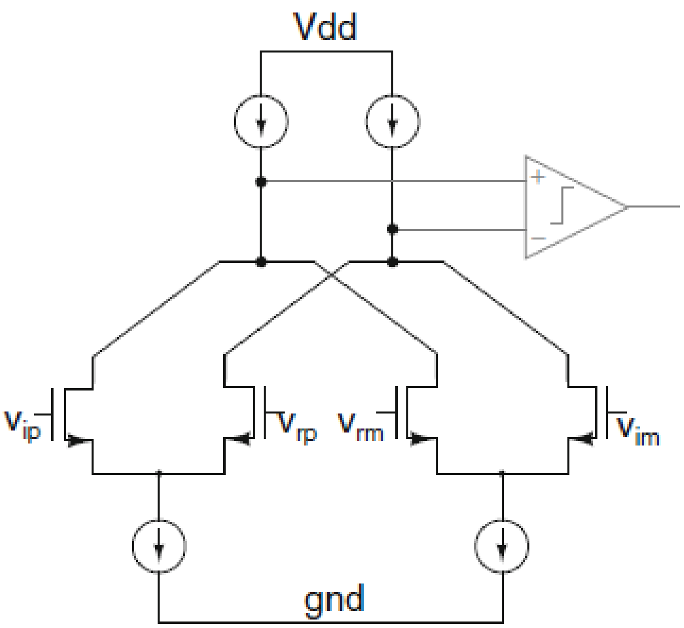
# Reference Subtraction: Scheme II




- Source followers to buffer $v_{in}$
  - reduced swing, varies with PVT
- Ladder is part of the signal path
  - Comparator input cap load the resistor taps
  - Excess delay


Arias, J., Kiss, P., Prodanov, V., Boccuzzi, V., Banu, M., Bisbal, D., et al. (2006). A 32-mW 320-MHz continuous-time complex ΣΔ ADC for multi-mode wireless-LAN receivers. *IEEE Journal of Solid State Circuits, 41*(2), 339–351.

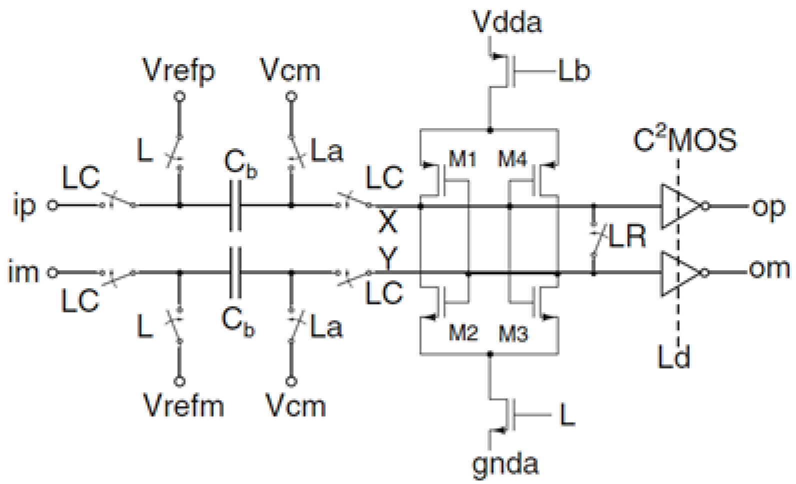
# Reference Subtraction: Scheme III

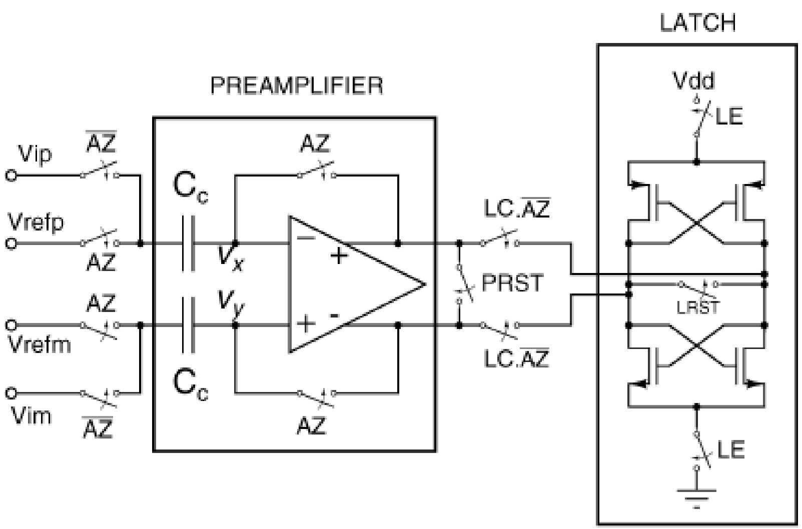



- Differential difference amplifier for subtracting the reference
  - followed by a zero crossing detector
- Relaxes the impedance requirements on the ladder
- Mismatch in differential pairs and tail current sources results in comparator offset
  - current trimming (see the reference below)
- Finite BW of the amplifier causes excess delay


Mitteregger, G., Ebner, C., Mechnig, S., Blon, T., Holuigue, C., & Romani, E. (2006). A 20-mW 640-MHz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. *IEEE Journal of Solid State Circuits, 41*(12), 2641–2649.

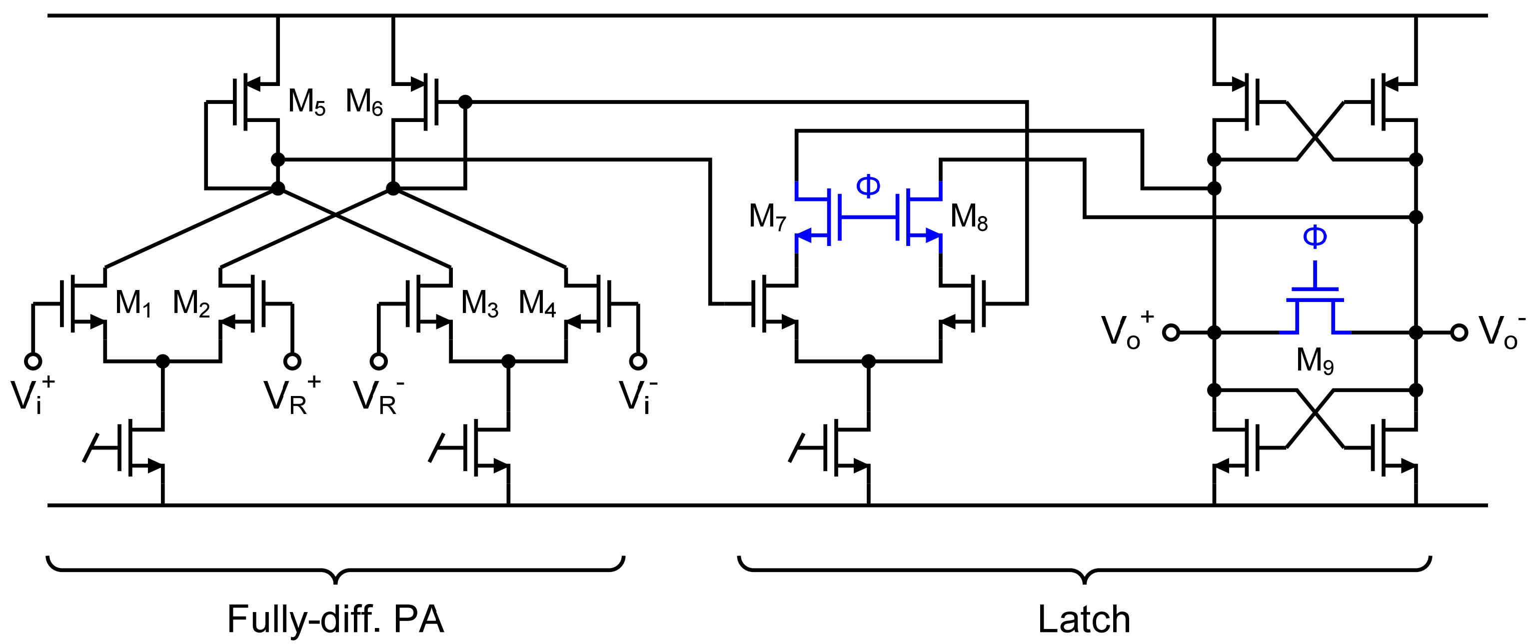
# Reference Subtraction: Scheme IV




- Switched-capacitor reference subtraction
  - Pay attention to charge injection
- ADC can handle large input swing
- Slow when auto-zeroing preamp is used
  - Large settling time constant
  - Reference subtraction in background

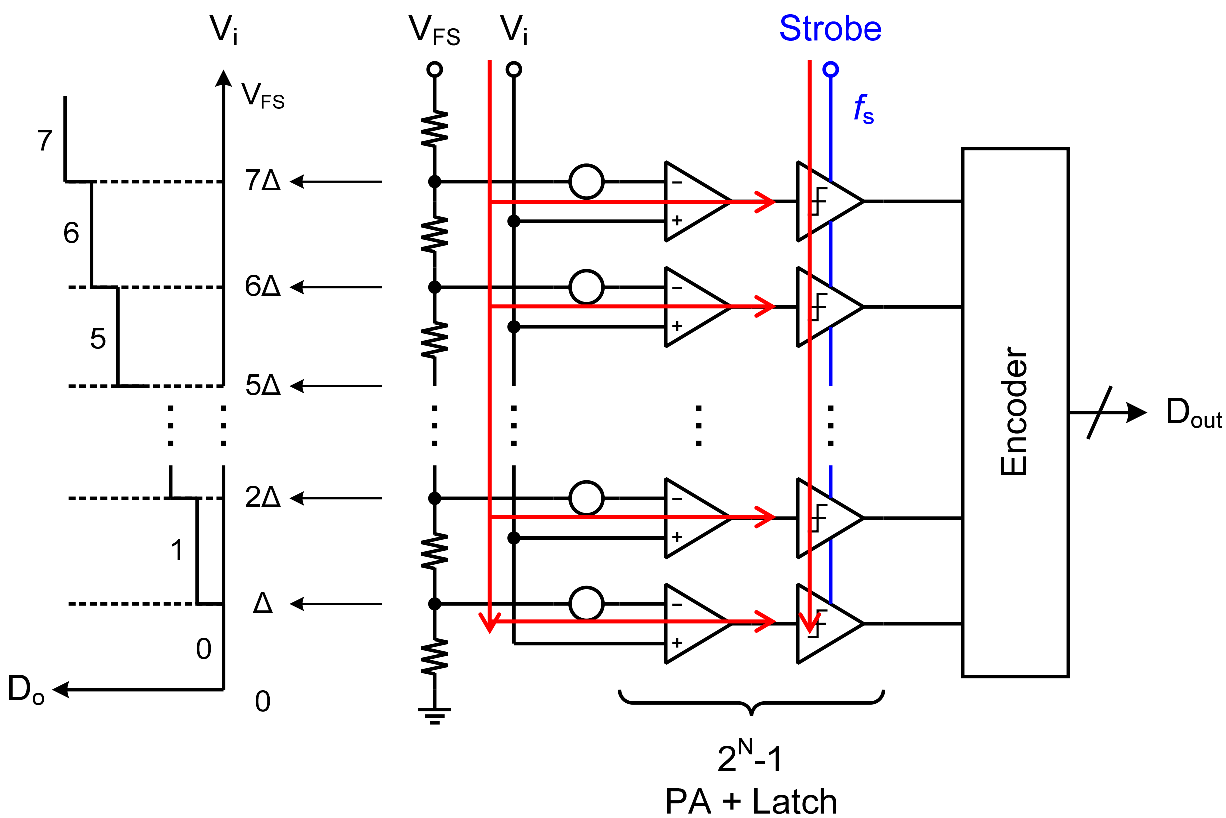
# Example: Fully-Differential Comparator




- Double-balanced, fully-differential preamp
- Switches ($M_7$, $M_8$) added to stop input propagation during regeneration
- Active pull-up PMOS added to the latch

# Flash ADC: Errors

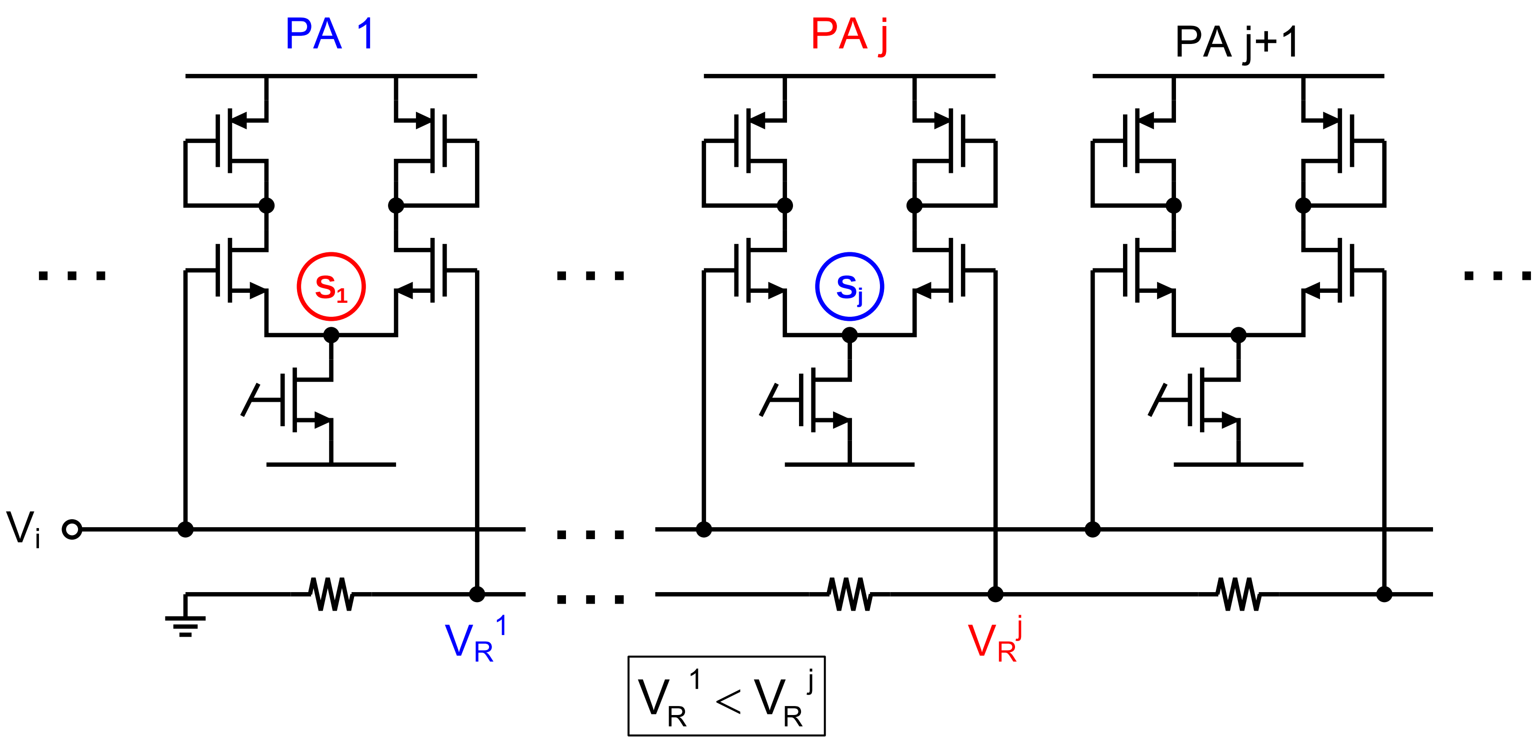
# Flash ADC Errors



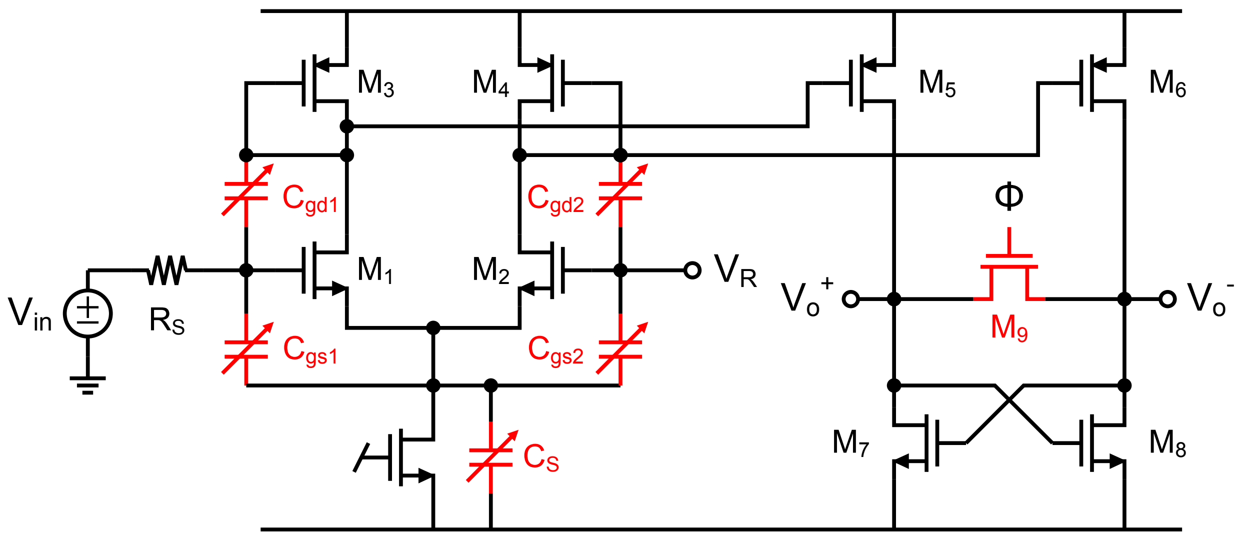

- SHA-less
- Signal and clock propagation delay
- $2^N$-1 PAs + latches must be matched
- Synchronized strobe signal is critical

Going parallel is fast, but also gives rise to inherent problems…

# Preamp Input Common Mode



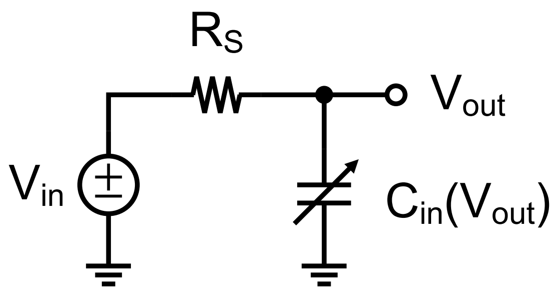

Input CM difference creates systematic mismatch (offset, gain, $C_{in}$, tracking BW, and CMRR) among preamps

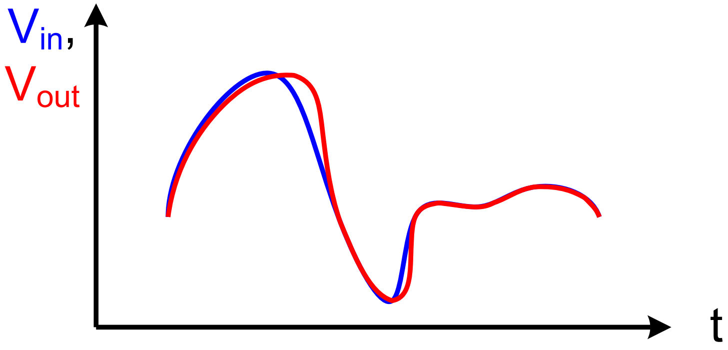



| Φ | Mode |
|---|---|
| "high" | Track |
| "low" | Regen |

- Preamp delay and $V_{th}$ of sampling switch ($M_9$) are both signal-dependent → signal-dependent sampling point (aperture error)
- A major challenge of distributing clock signals across $2^N$-1 comparators in flash ADC with minimum clock skew (routing, $V_{th}$ mismatch of $M_9$, etc.)

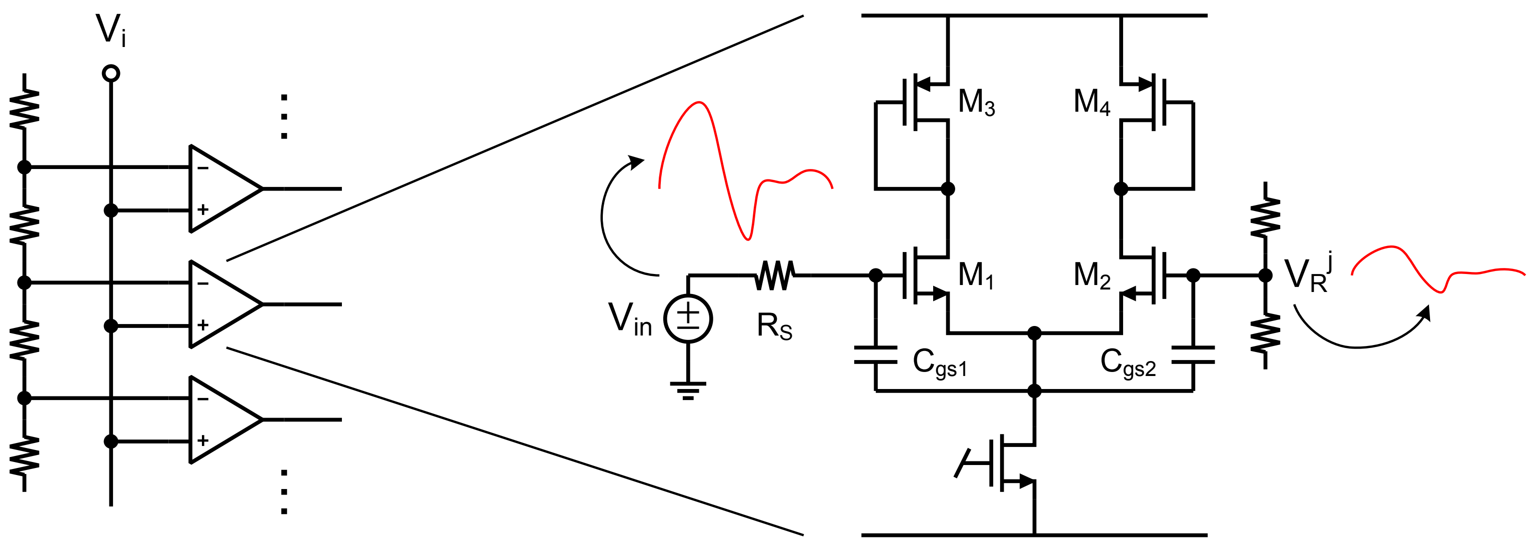
# Nonlinear Input Capacitance



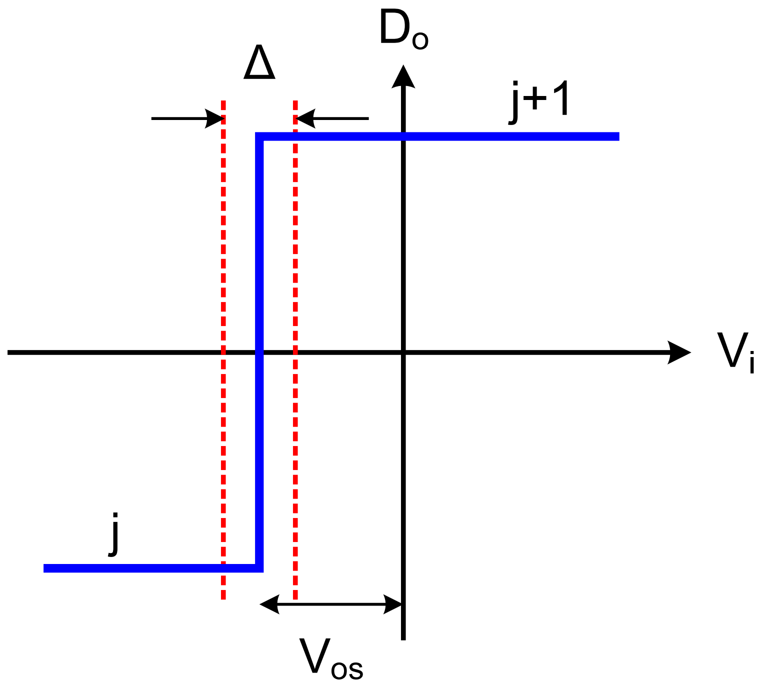

Signal-dependent input bandwidth ($1/R_S C_{in}$) introduces distortion

# Input Signal Feedthrough




Feedthrough of $V_{in}$ to the reference ladder through the serial connection of $C_{gs1}$ and $C_{gs2}$ disturbs the reference voltages

# Comparator Metastability



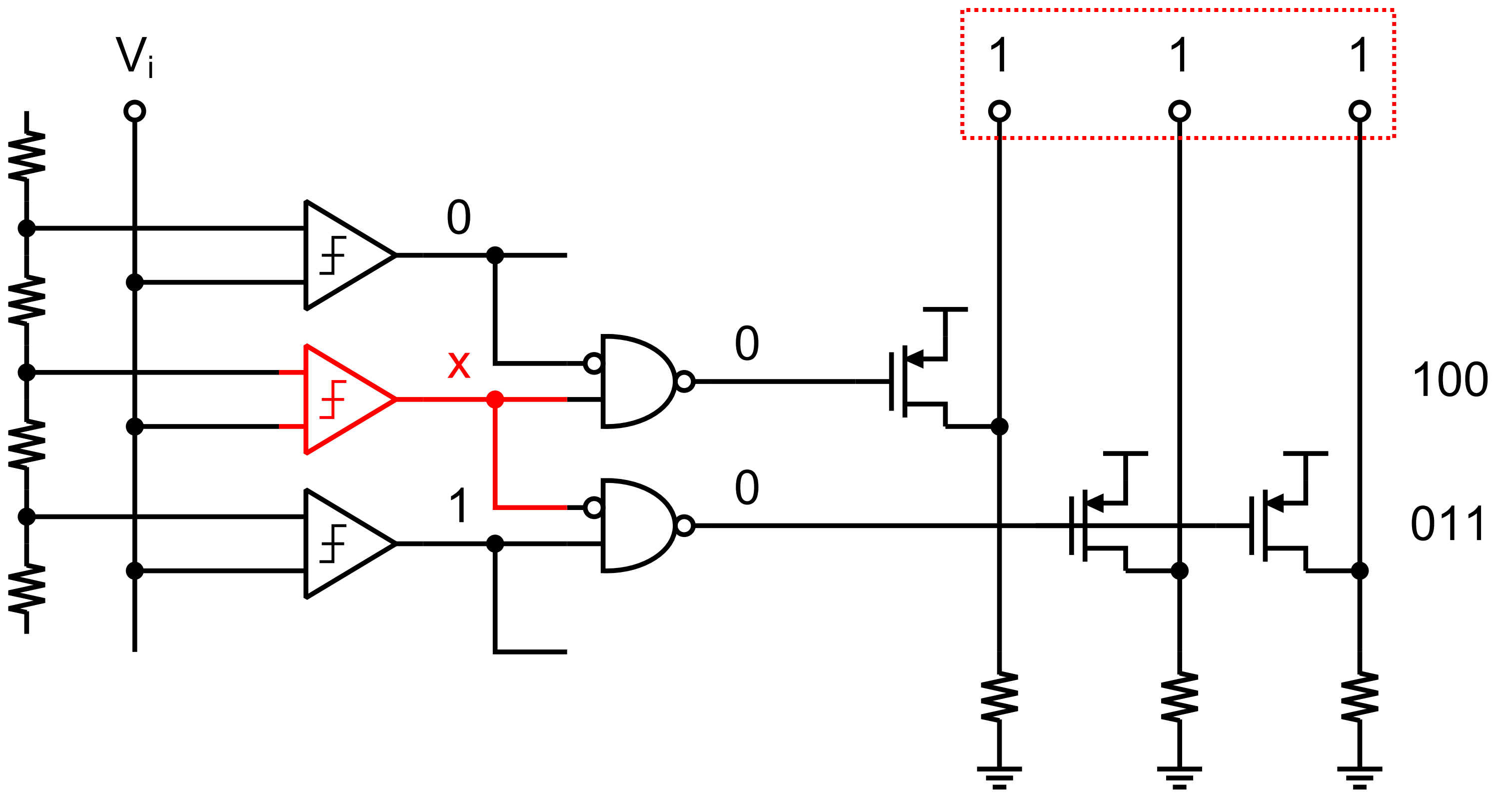

Assuming that the input is uniformly distributed over $V_{FS}$, then

$$BER = \frac{\Delta}{1LSB}$$

$$V_o(t) = V_i(0) \cdot A_{V1} A_{V2} \cdot \exp(t \cdot g_m / C_L)$$

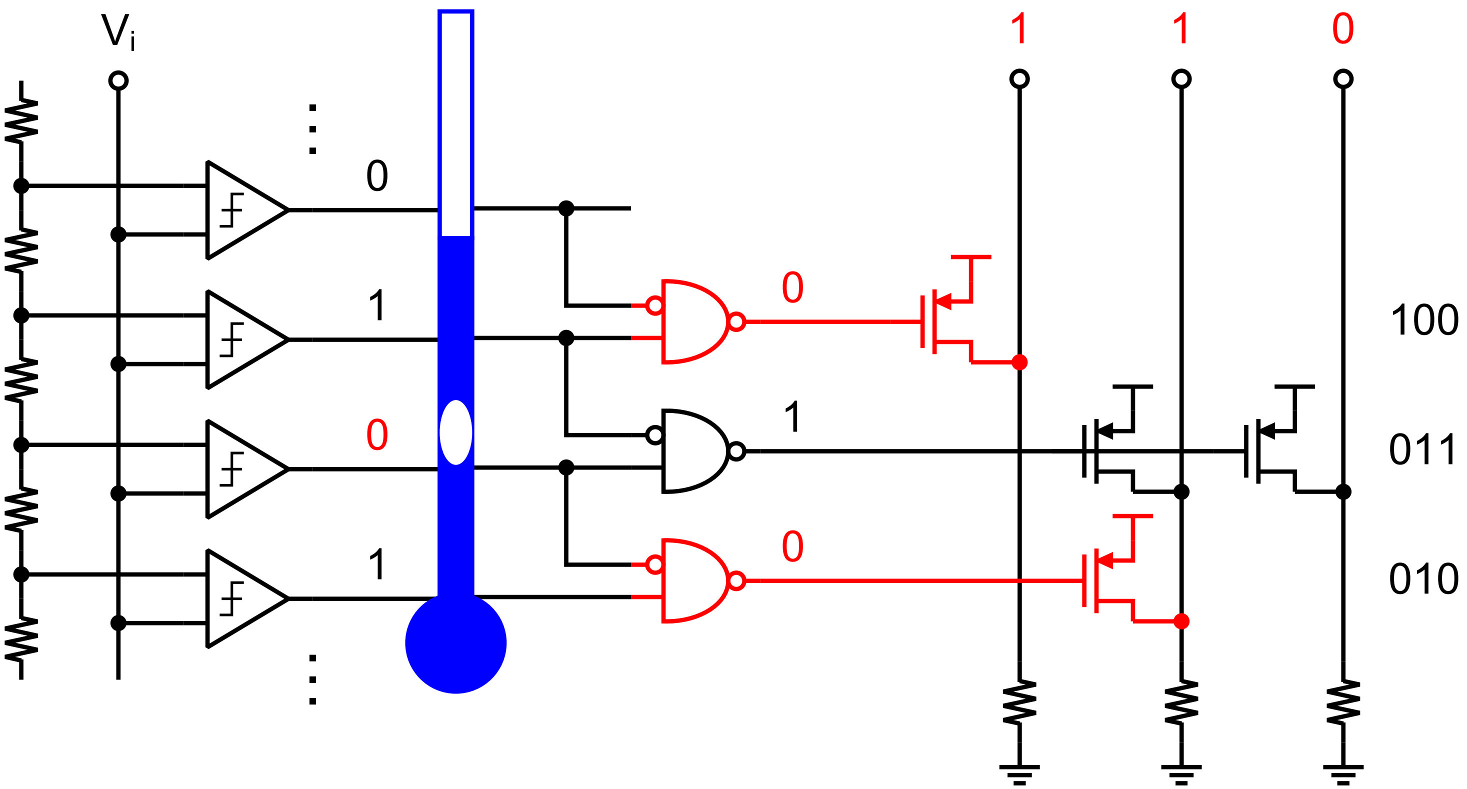
- Cascade preamp stages (typical flash comparator has 2-3 PA stages)
- Use pipelined multi-stage latches; PA can be pipelined too
- **Avoid branching off comparator logic outputs**

# Comparator Metastability



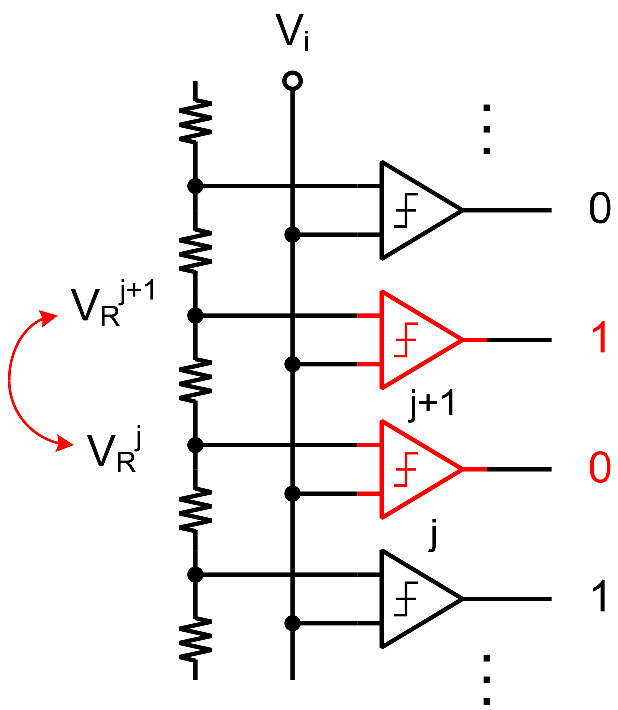

Logic levels can be misinterpreted by digital gates (branching off, diff. outputs)

# Bubbles (Sparkles) in Thermometer Code

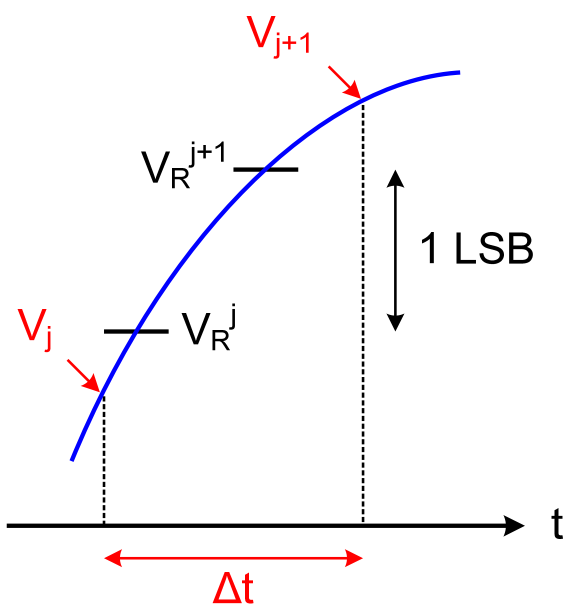



Static/dynamic comparator errors cause bubbles in thermometer code

# Bubbles (Sparkles)

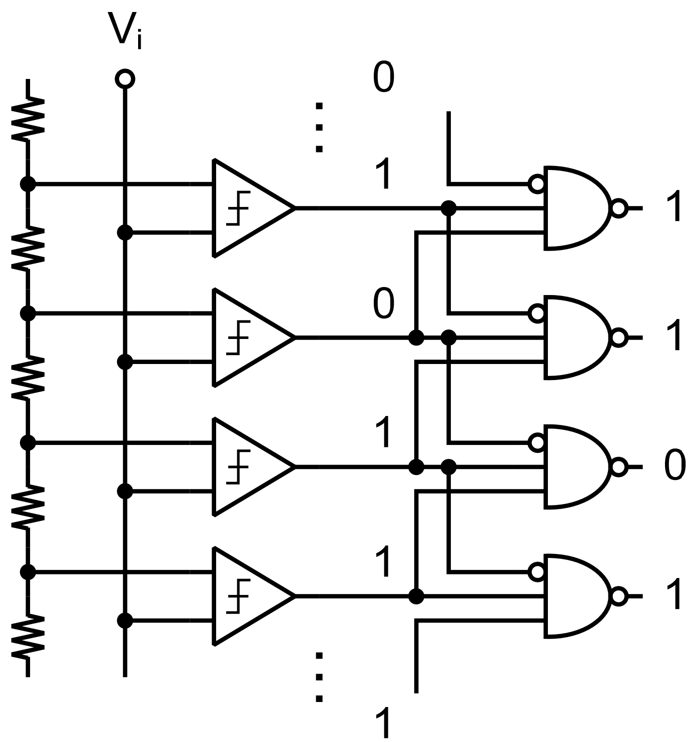



Comparator offset




Timing error

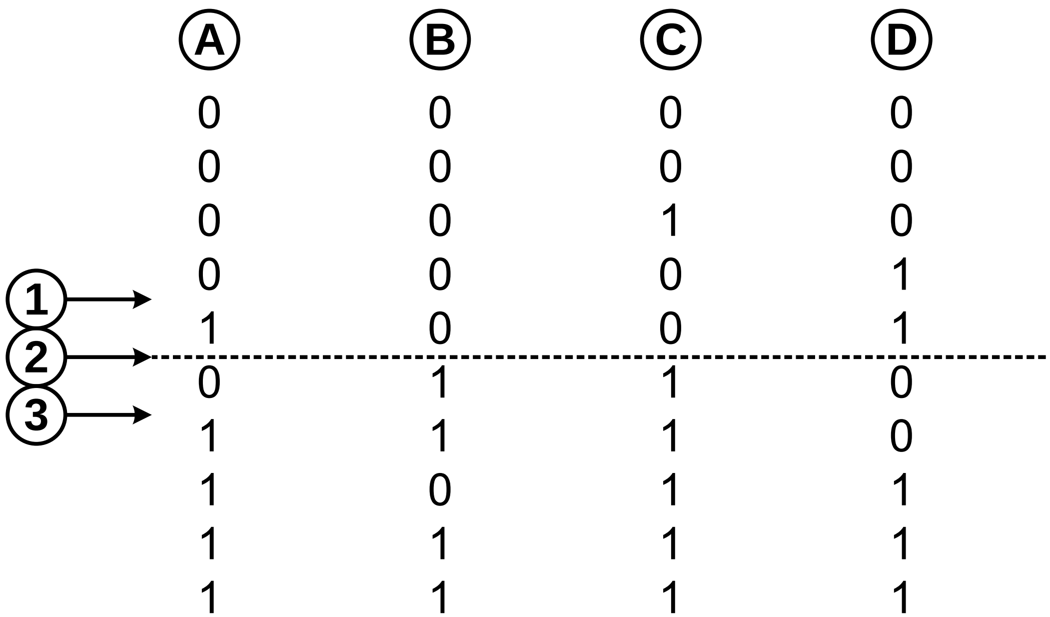
# Bubble-Tolerant Boundary Detector




- 3-input NAND
- Detect “011” instead of “01” only
- “Single” bubble correction
- Biased correction


Ref: J. G. Peterson, “A monolithic video A/D converter,” *IEEE Journal of Solid-State Circuits*, vol. 14, pp. 932-937, issue 6, 1979.

# Built-In Bias




| Case | "011" Det. | "001" Det. |
|---|---|---|
| A | ③ | ① |
| B | Fail | ② |
| C | ② | Fail |
| D | Fail | Fail |

Inspecting more neighboring comparator outputs improves performance

# Majority Voting Logic

$$C_j^* = C_{j-1}C_j + C_jC_{j+1} + C_{j-1}C_{j+1}$$

| | A | | B | | C | | D | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| ① | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| ② | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| ③ | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Case | "011" Det. | Majority voting |
|---|---|---|
| A | ③ | ② |
| B | Fail | ② |
| C | ② | ② |
| D | Fail | Fail |

Ref: C. W. Mangelsdorf, "A 400-MHz input flash converter with error correction," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 184-191, issue 1, 1990.

# Gray Encoding

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$

$$G_2 = T_2\overline{T_6}$$

$$G_3 = T_4$$

**Only one transition b/t adjacent codes**

| Thermometer | | | | | | | Gray | | | Binary | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ | $T_6$ | $T_7$ | $G_3$ | $G_2$ | $G_1$ | $B_3$ | $B_2$ | $B_1$ |

- One comparator output is ONLY used once → No branching!
- Gray encoding fails benignly in the presence of bubbles
- Codes are also robust over metastability errors

# Gray Encoding

| Thermometer | | | | | | | | | | | | | | | Gray | | | | Decimal |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 13 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 15 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 12 |

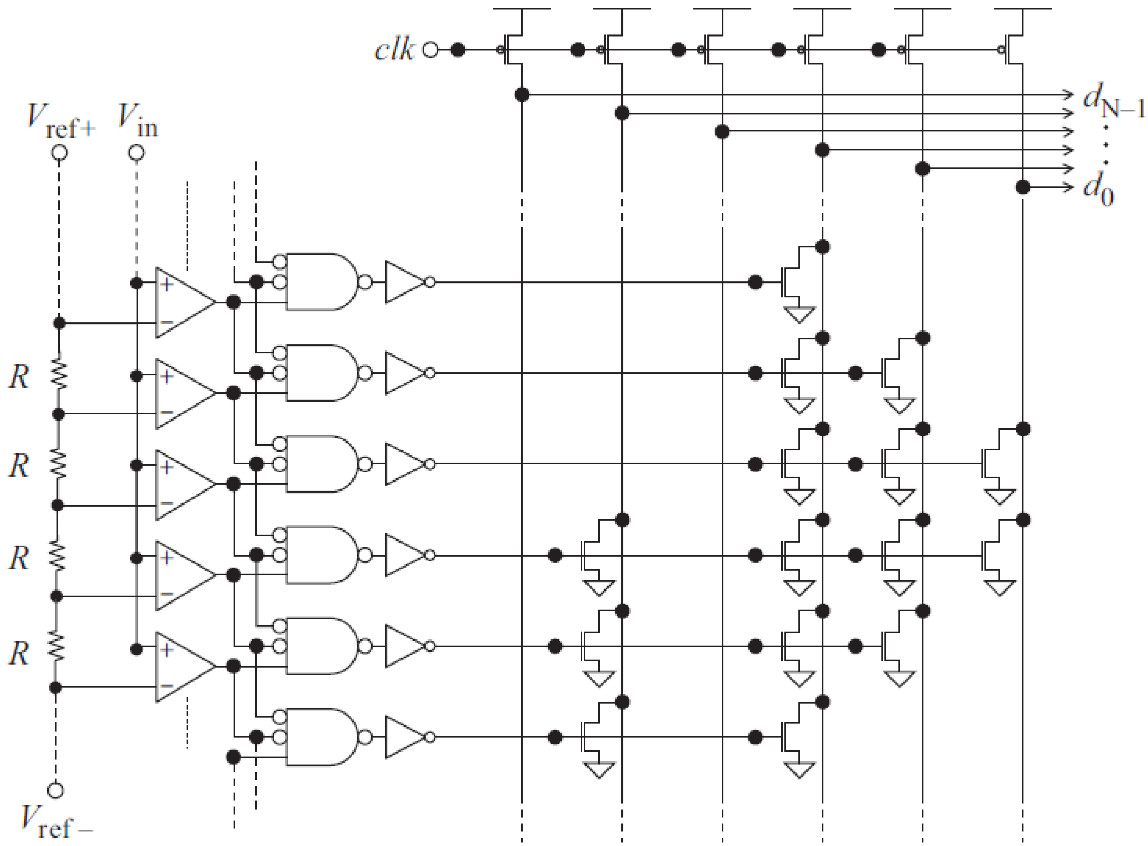
$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

Conversion of Gray code to binary code is quite time-consuming → "quasi" Gray code

Ref: Y. Akazawa, et al., "A 400MSPS 8b flash AD conversion LSI," in *IEEE International Solid-State Circuits Conference*, Dig. Tech. Papers, 1987, pp. 98-99.

# Flash ADC: Binary Decoders

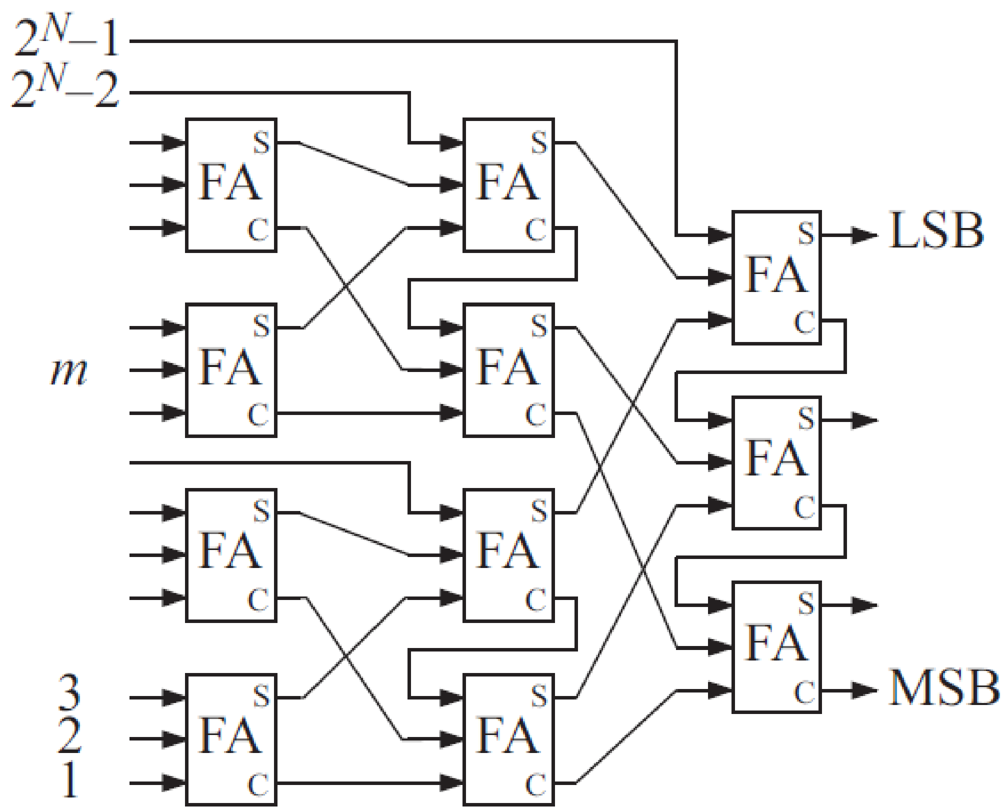
# Gray Encoded ROM Decoder




Thermometer-to-Binary Decoders for Flash Analog-to-Digital Converters

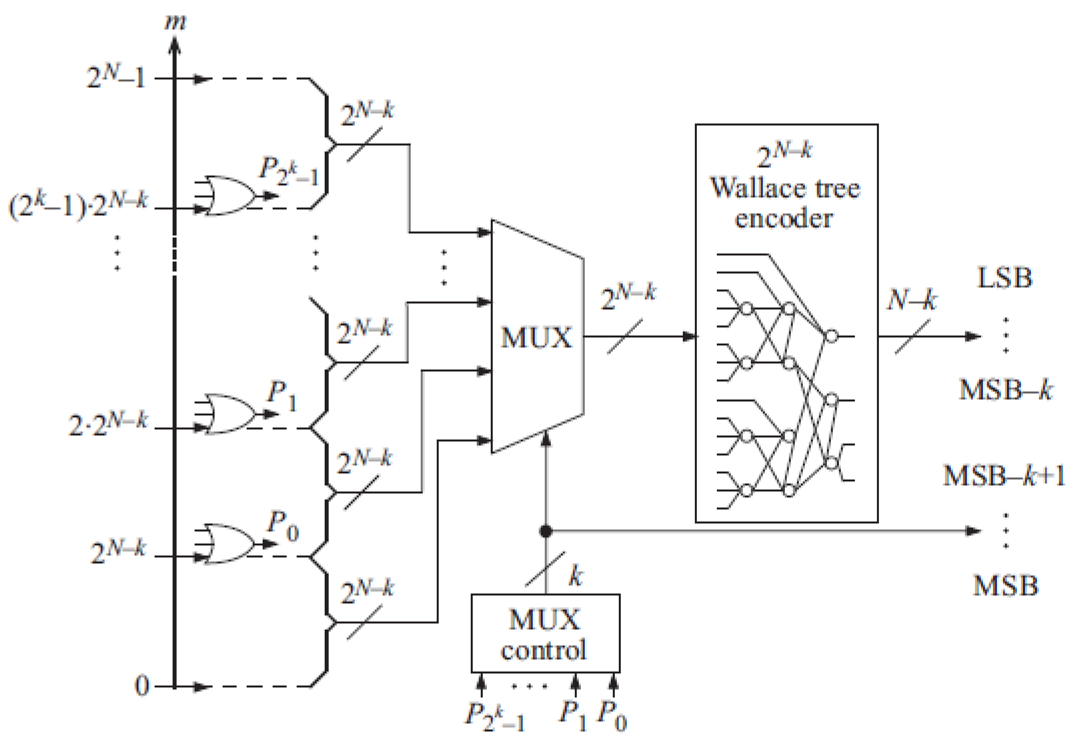
Erik Säll and Mark Vesterbacka

# Wallace Tree Adder (1s Adder)

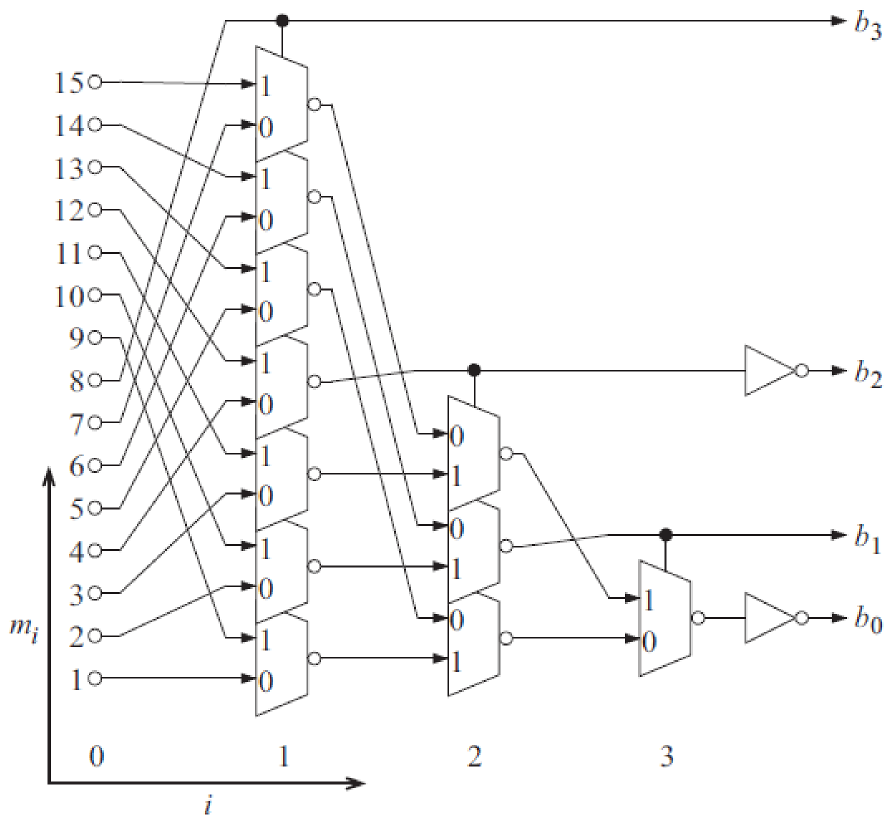



Wallace tree decoder for an $N = 4$-bit flash ADC.

# Folded Wallace Tree Decoder

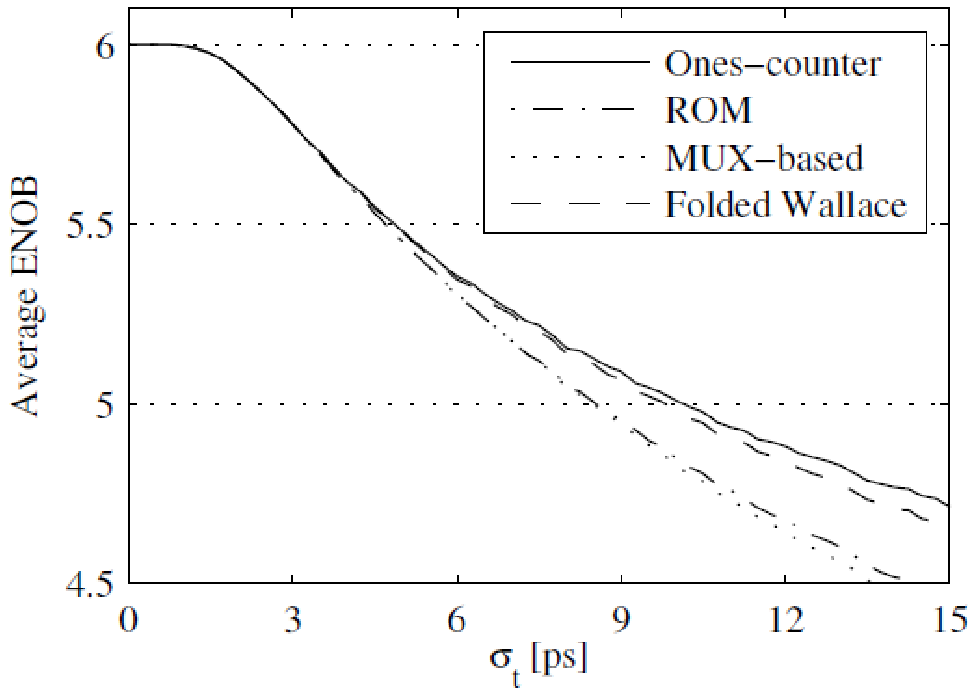


# MUX-based Decoder




Multiplexer-based decoder for $N = 4$ bits.

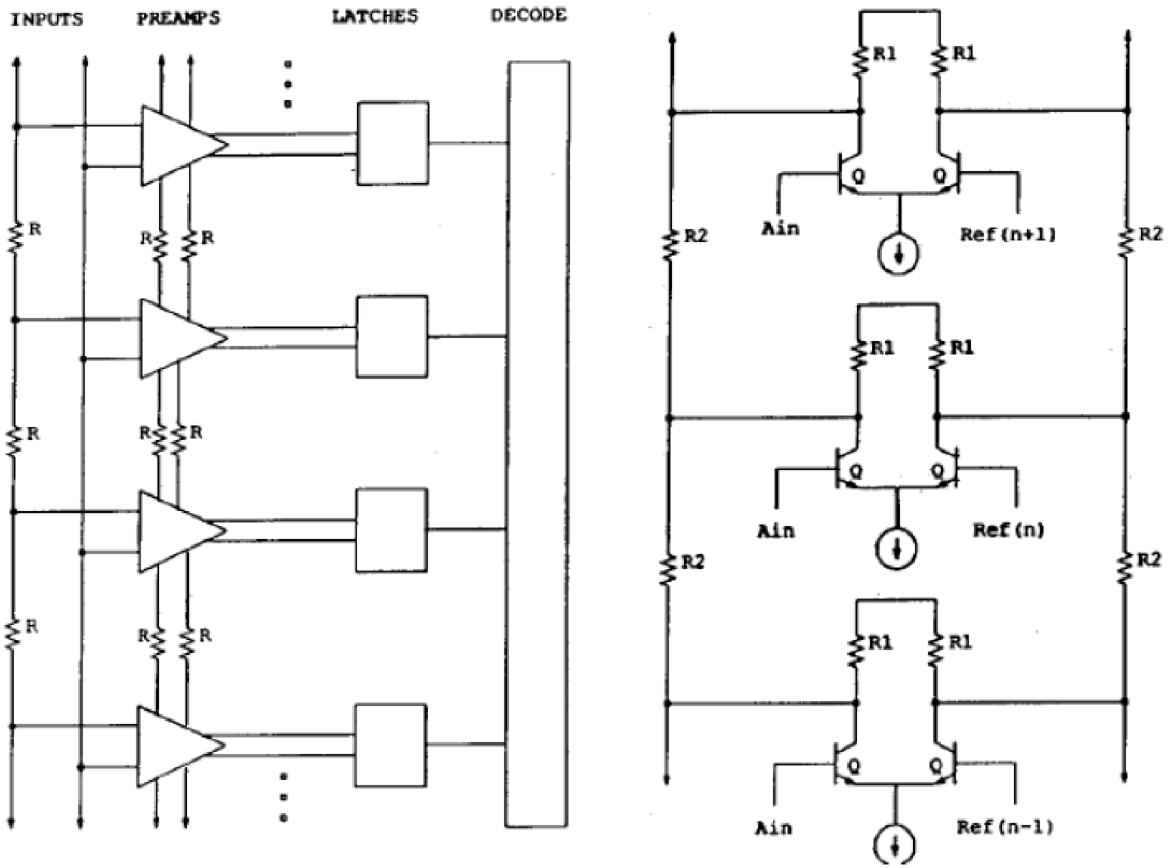
# Comparison of Decoder Schemes




- Mostly custom design at higher speeds
- Pipeline the digital backend at high-sampling rates to meet clock timing
  - $T_{pd} < T_{CK} - (t_{pcq} + t_{setup})$
  - $T_{cd} > t_{hold} - t_{ccq}$

# Flash ADC: Other Techniques

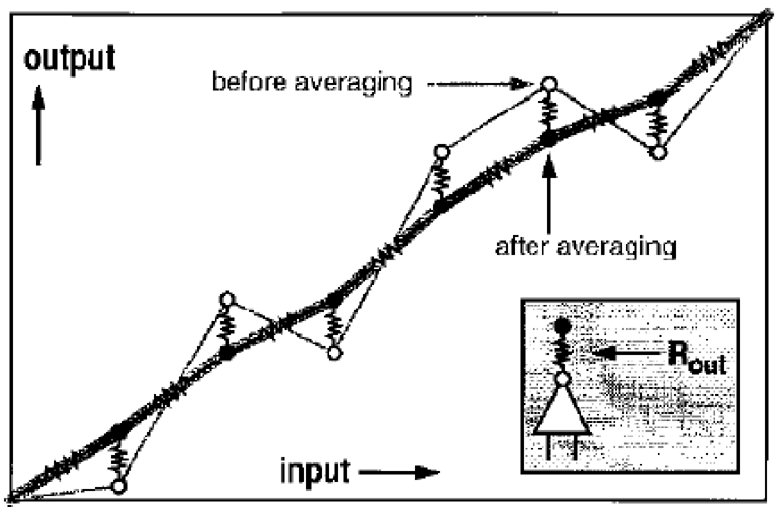
# Offset Averaging (1)



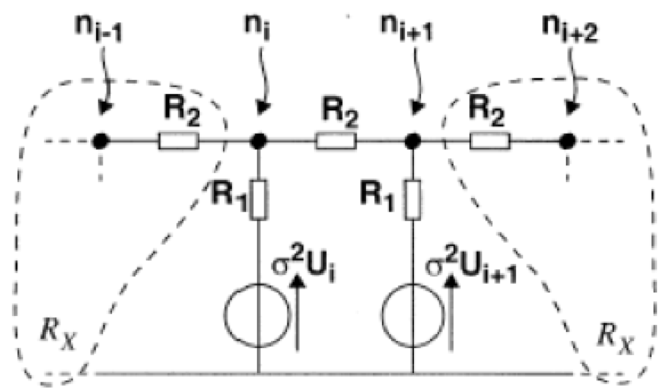

R2/R1=1.3

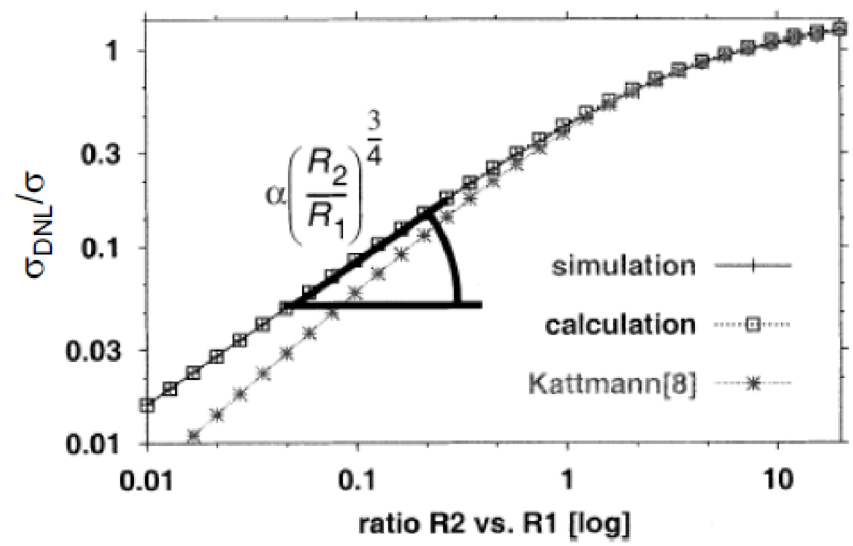
[Kattmann & Barrow, ISSCC 1991]

# Offset Averaging (2)



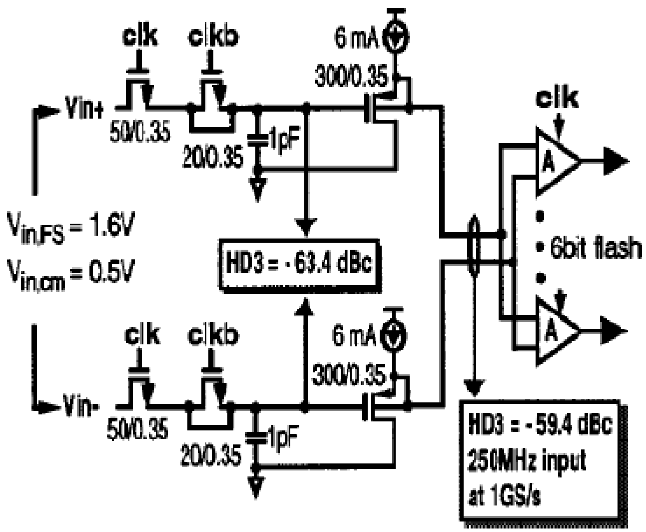

[Bult & Buchwald, JSSC 12/1997]

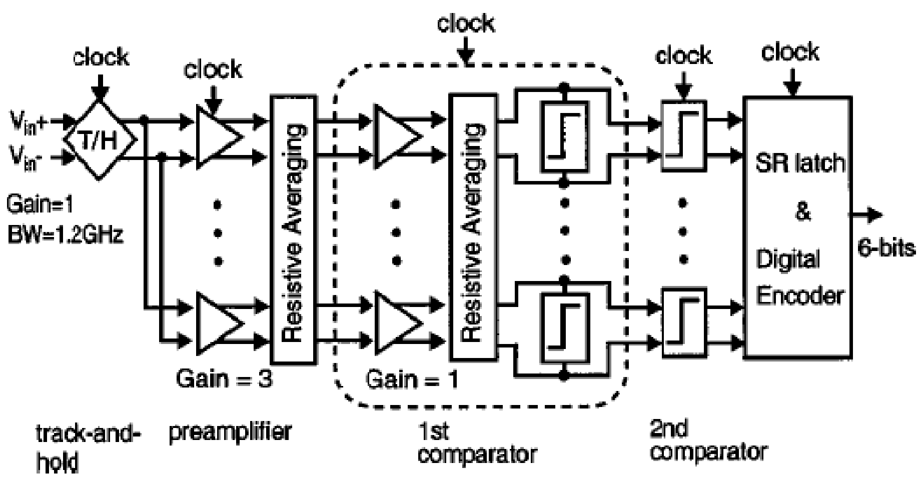



[Scholtens & Vertregt, JSSC 12/2002]

# Flash ADC with Averaging



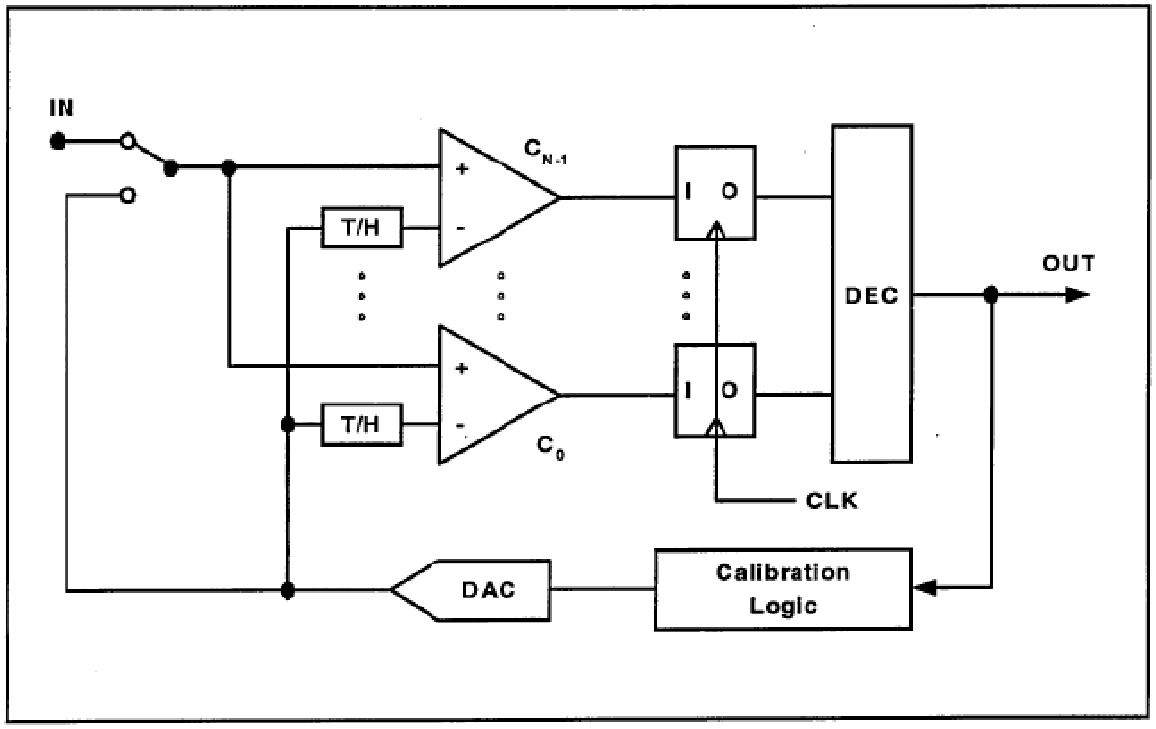




[Choi & Abidi, JSSC 12/2001]

| | |
|---|---|
| Resolution | 6 bits |
| Conversion Rate | 1.3 GS/s |
| INL/DNL @ Fs = 1 GHz | 0.35 LSB / 0.2 LSB |
| Input Range | 1.6 $V_{p-p}$ differential |
| Input Capacitance (T/H) | 1 pF |
| Bit Error Rate @ fs = 1 GHz | < $10^{-10}$ |
| SFDR @ fin = 100 MHz | > 44 dB up to 1.3 GS/s |
| SNDR @ fin = 630 MHz<br>@ fin = 650 MHz | 35 dB @ 1 GS/s<br>32 dB @ 1.3 GS/s |
| Power Dissipation<br>(50% due to logic and clock) | 500 mW @ 1 GS/s<br>545 mW @ 1.3 GS/s |
| Voltage Supply | 3.3 V |
| Active/Total Die Area | 2x0.4 $mm^2$ / 2.2x2.2 $mm^2$ |
| Technology | 0.35-μm CMOS |

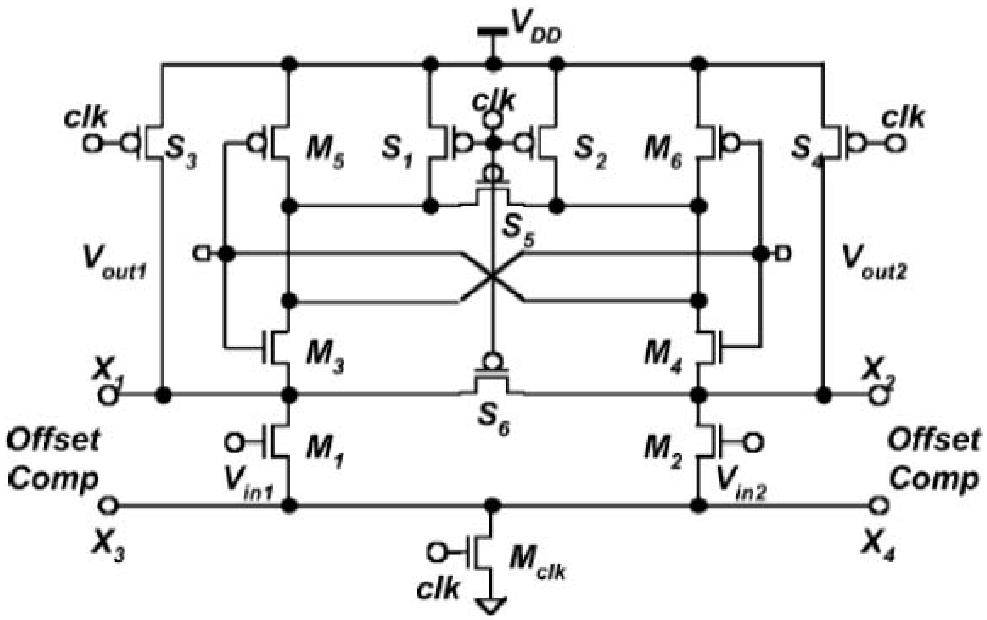
Averaging networks designed to reduce input referred offset by 3x

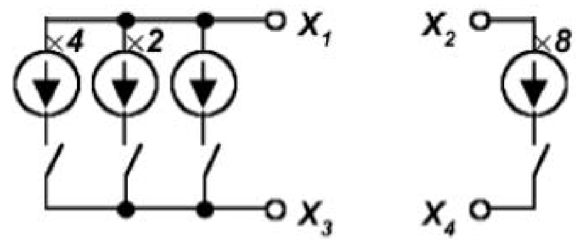
# Offset Calibration




S. Sutardja, "360 Mb/s (400 MHz) 1.1 W 0.35µm CMOS PRML read channels with 6 burst 8-20× over-sampling digital servo," ISSCC Dig. Techn. Papers, Feb. 1999.

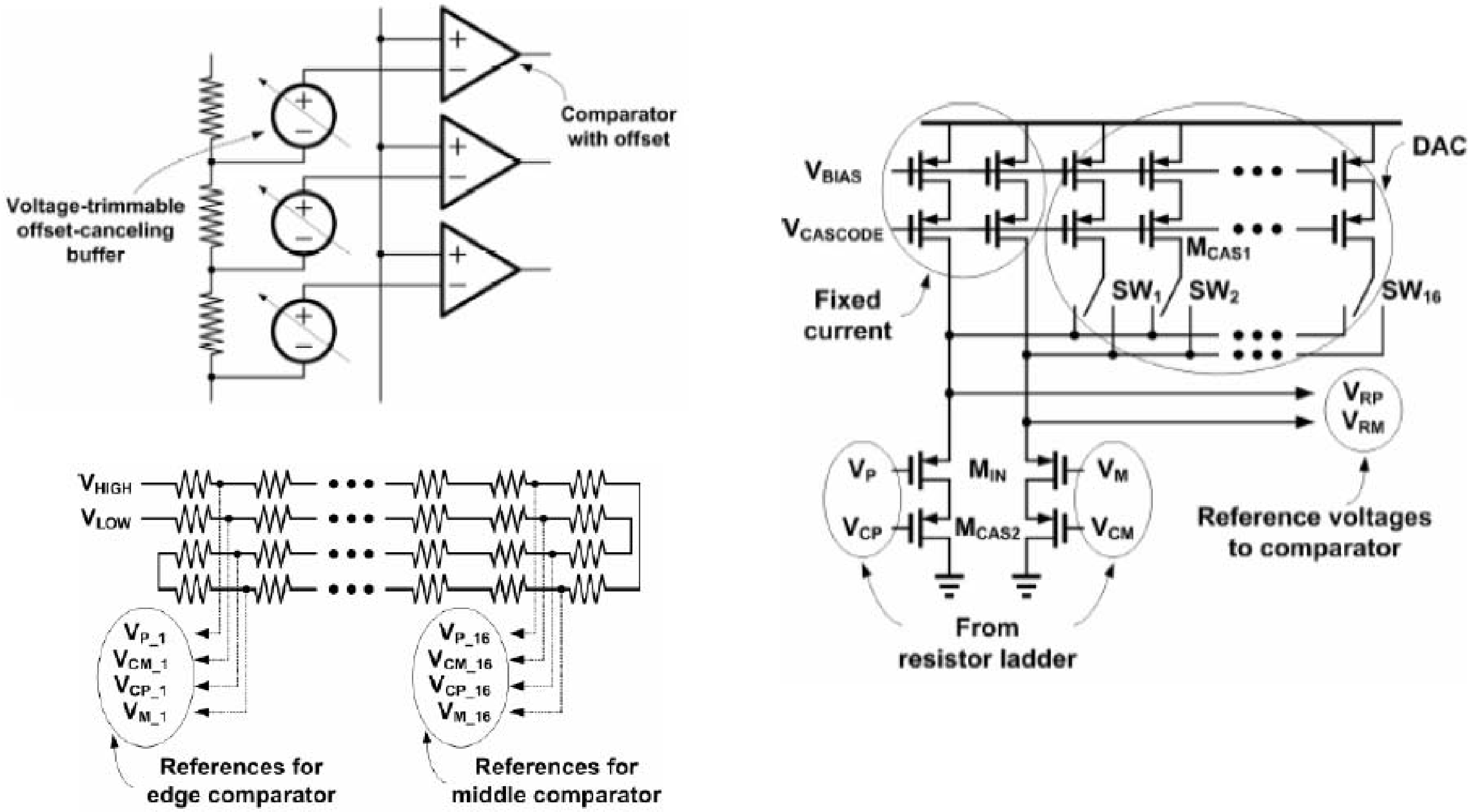
# Comparator with Offset Correcting DAC




[K.-L.J. Wong and C.-K.K. Yang, "Offset compensation in comparators with minimum input-referred supply noise," JSSC, May 2004.]

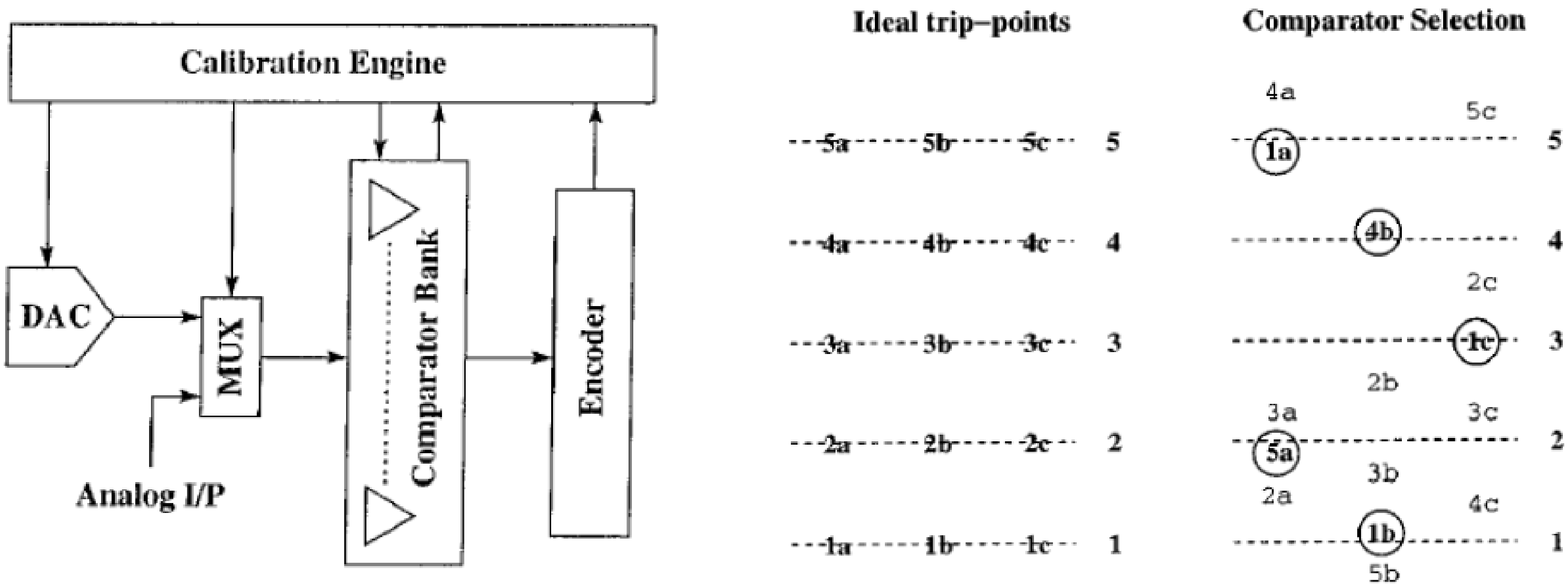
# High-Performance Flash with Calibration (1)




[Park & Flynn, "A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS," CICC 2006]

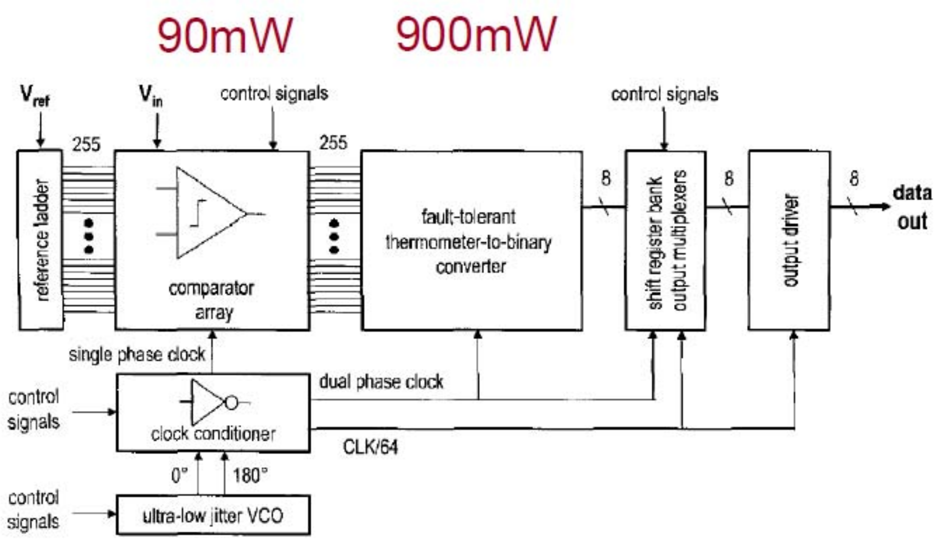
# Comparator Redundancy (1)

- Idea: Build a "sea of imprecise comparators", then determine which ones to use…




C. Donovan, M. P Flynn, "A 'digital' 6-bit ADC in 0.25-µm CMOS," IEEE J. Solid-State Circuits, pp. 432-437, March 2002.

# Comparator Redundancy (2)



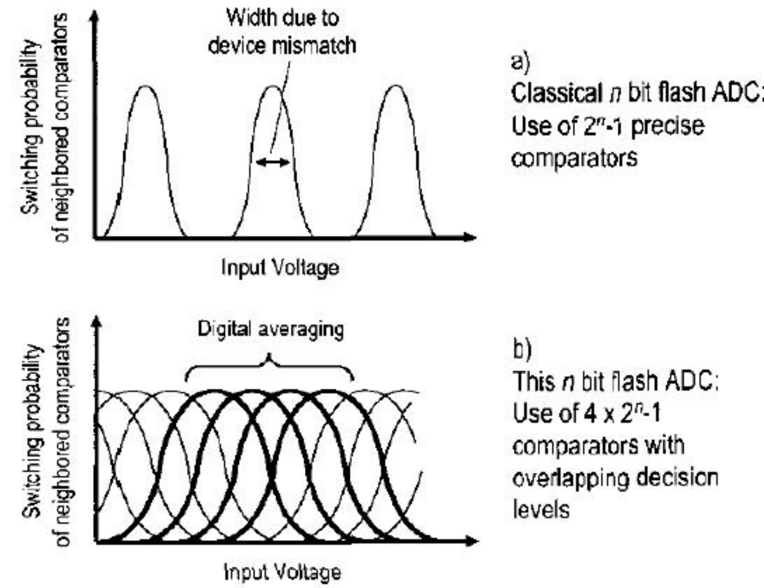
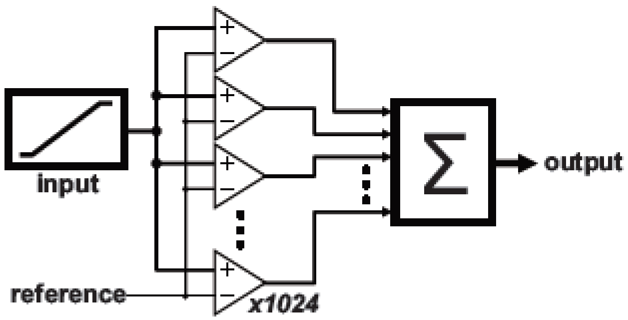
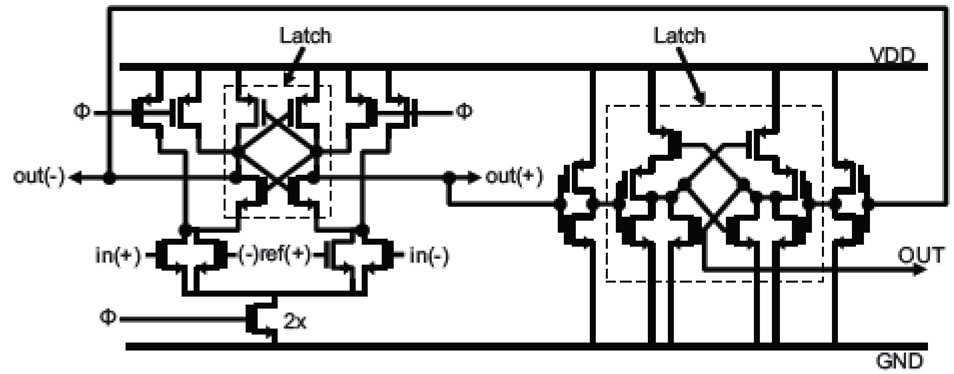



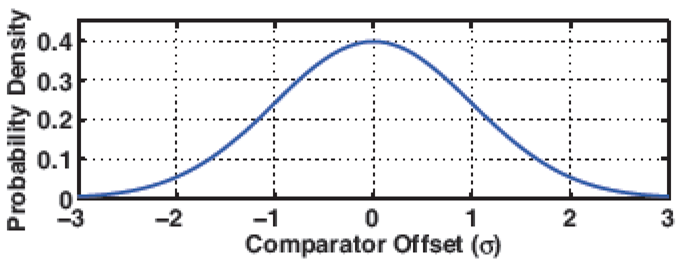

Fig. 1 Illustration of the ADC operation scheme.

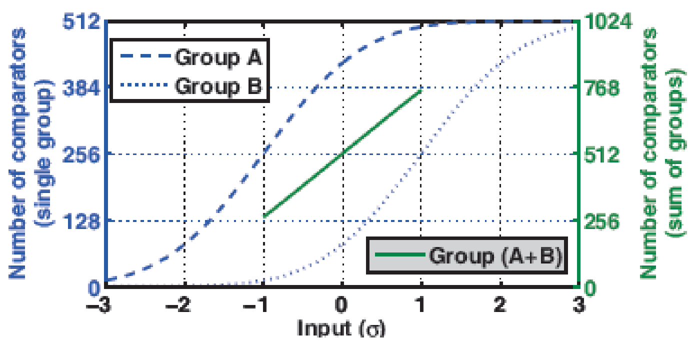
Paulus et al., "A 4GS/s 6b flash ADC in 0.13um CMOS," *VLSI Circuits Symposium*, 2004

# Stochastic Flash ADC




- Fully synthesized ADC using 'digital' comparator cells (large offsets)
- Use more than 1 comparator for a reference threshold
  - Use 'detection theory' to make accurate decisions around a threshold, by using more than one observation
- Low speed designs (<20 MS/s)

A 6b Stochastic Flash Analog-to-Digital Converter Without Calibration or Reference Ladder

Skyler Weaver[1], Benjamin Hershberg[1], Daniel Knierim[2], and Un-Ku Moon[1]

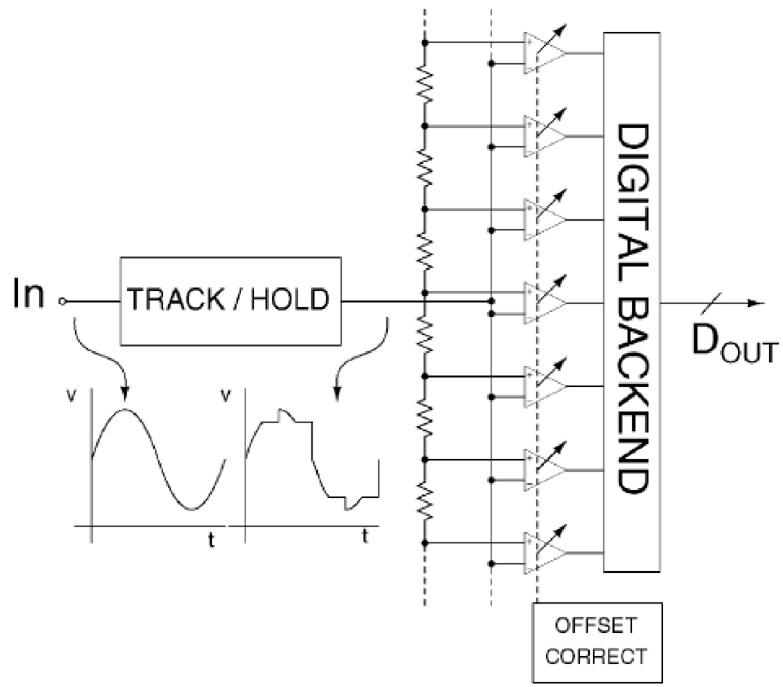
# Flash ADC: Case Study

# Case Study: Distortion Compensating Flash ADC

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 9, SEPTEMBER 2006 1959

## A Distortion Compensating Flash Analog-to-Digital Conversion Technique

Venkata Srinivas, Shanthi Pavan, Ashish Lachhwani, and Naga Sasidhar



# T/H Distortion

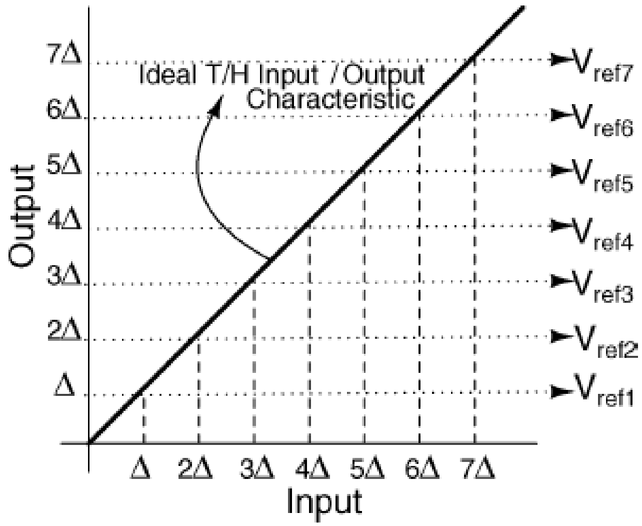



Fig. 2. Flash ADC behavior with an ideal track-and-hold.

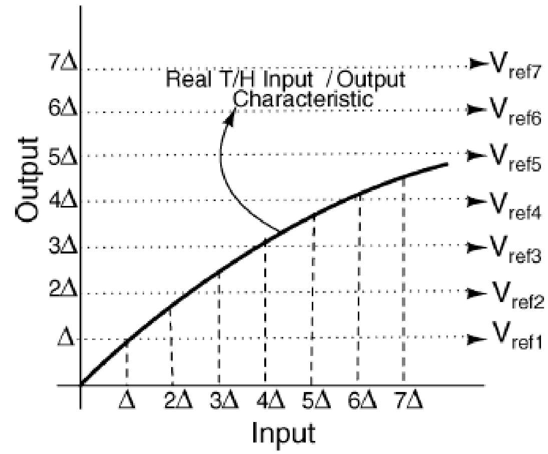
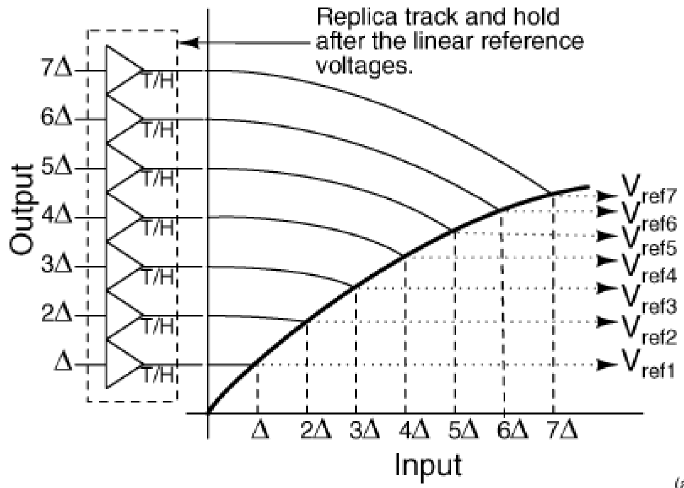
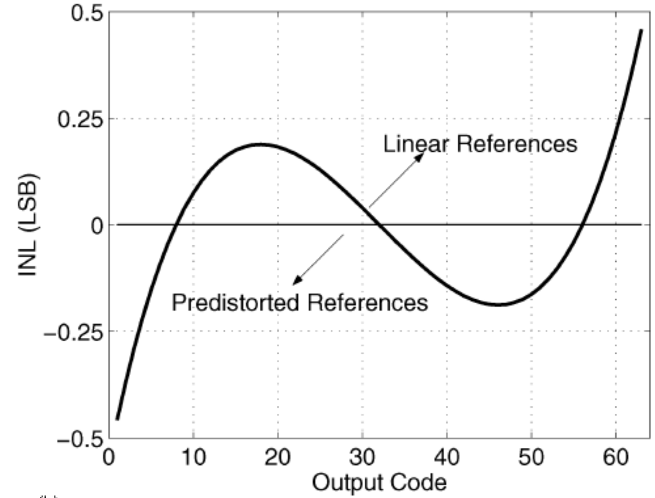



Fig. 3. Flash ADC behavior with a real track-and-hold having static nonlinearity.

# Pre-distorted References



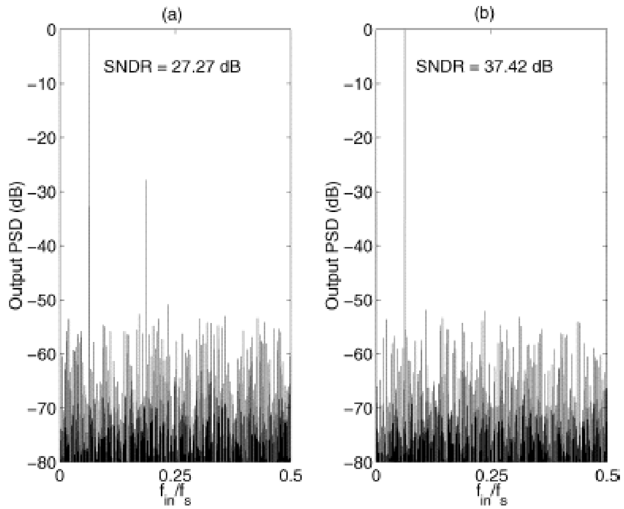
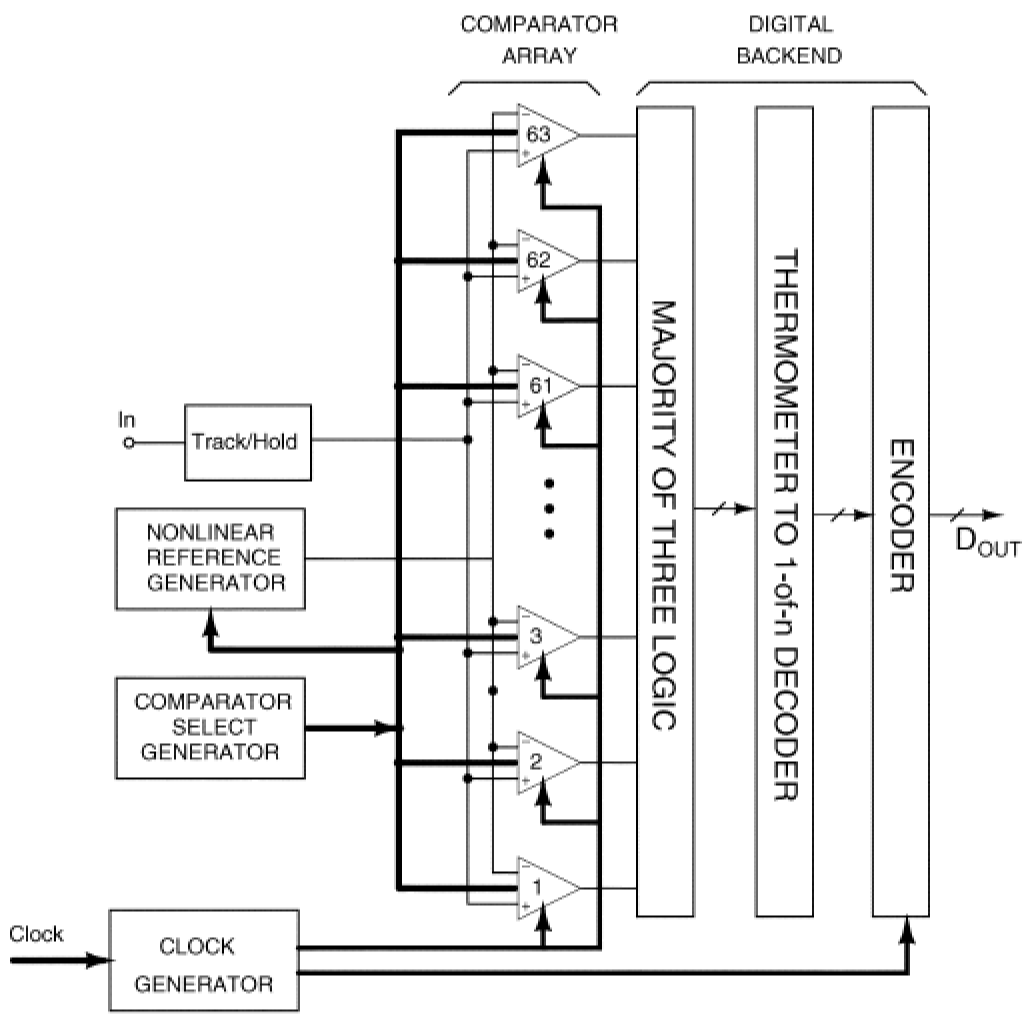
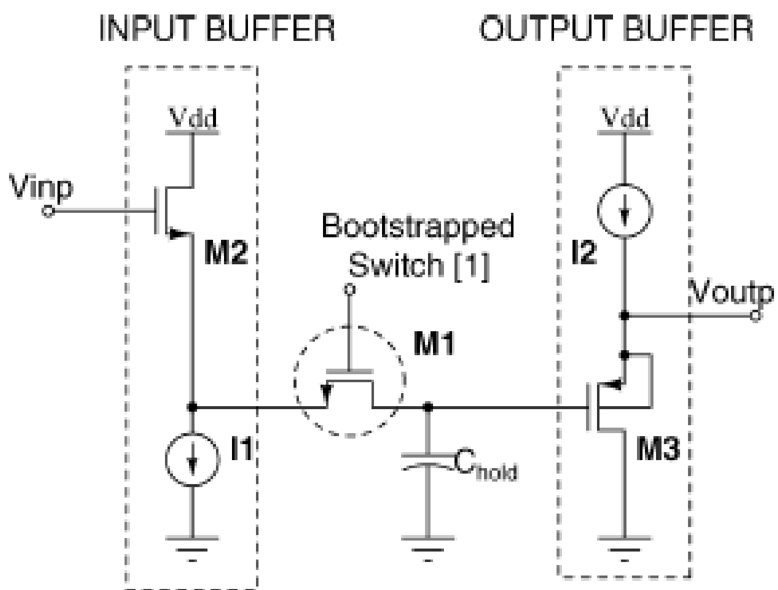




Fig. 5. ADC output spectrum with track-and-hold having static nonlinearity with (a) linear references and (b) predistorted references.

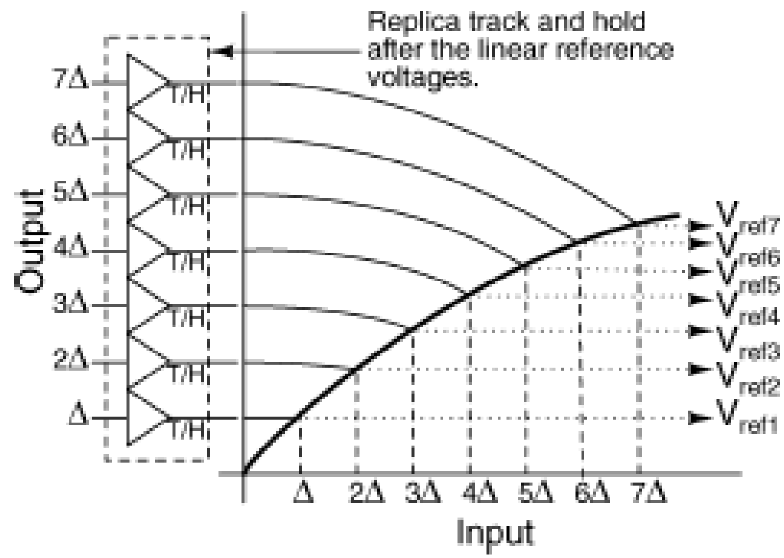
# ADC Architecture



# T/H Circuit

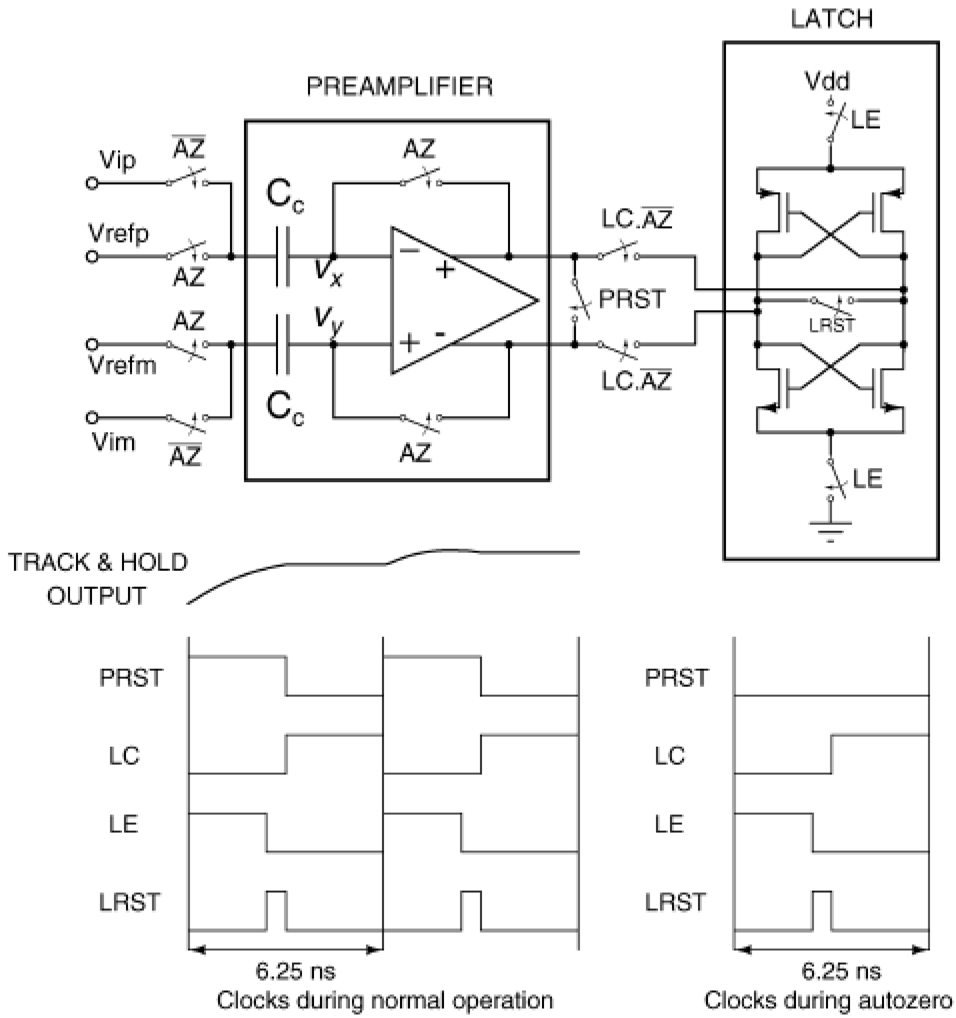


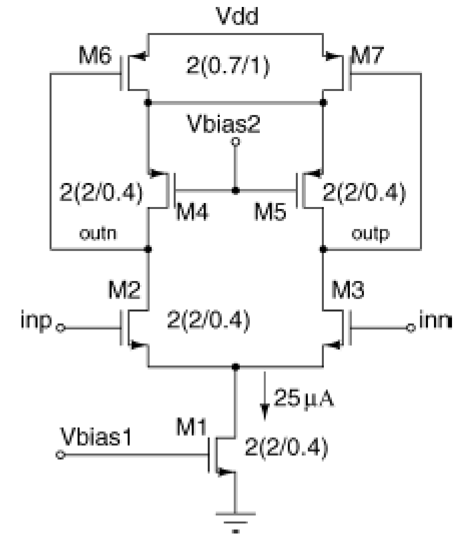
INPUT BUFFER
OUTPUT BUFFER
Vdd
Vdd
Vinp
M2
Bootstrapped Switch [1]
M1
I2
Voutp
I1
C hold
M3

Replica track and hold after the linear reference voltages.
7Δ
6Δ
5Δ
4Δ
3Δ
2Δ
Δ
T/H
Output
V ref7
V ref6
V ref5
V ref4
V ref3
V ref2
V ref1
Δ 2Δ 3Δ 4Δ 5Δ 6Δ 7Δ
Input

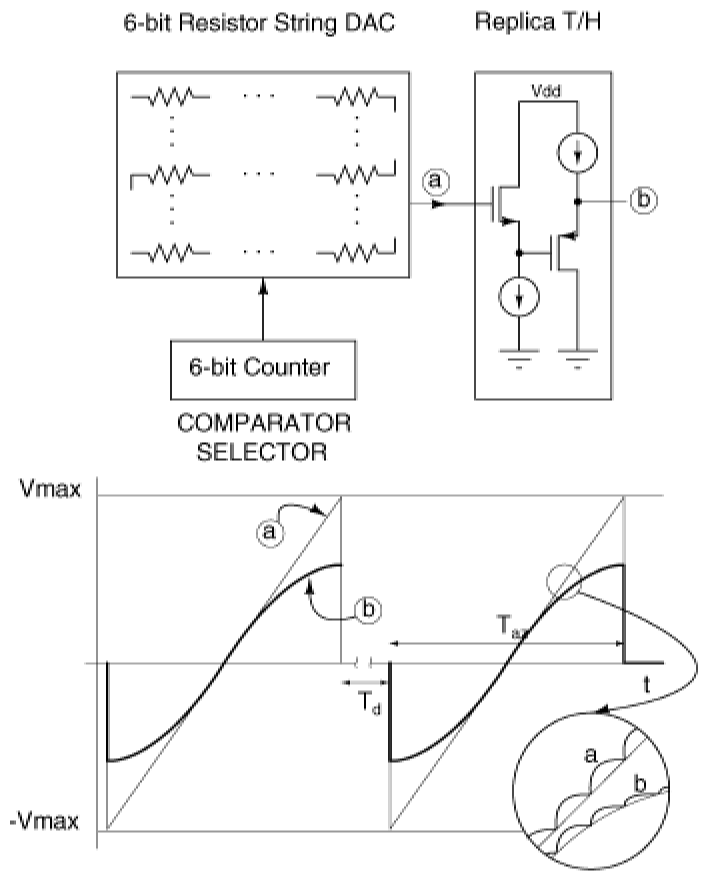
# Comparator




Schematic of the preamplifier.

# Non-linear Reference Generator




g. 12. Nonlinear reference generator.

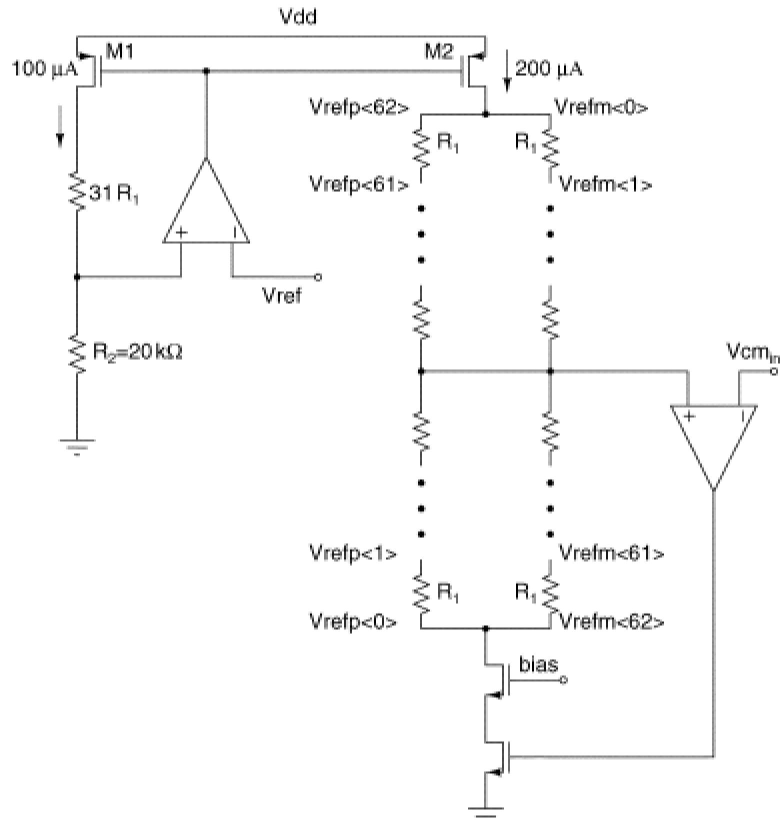
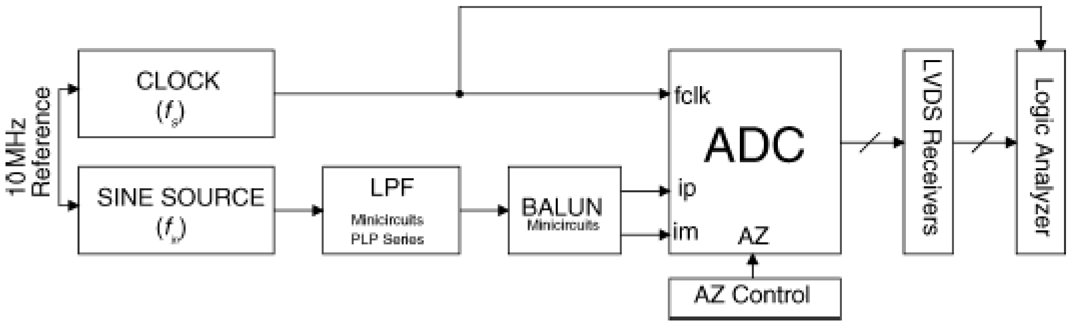



Fig. 13. Linear reference generator.

# ADC Testing



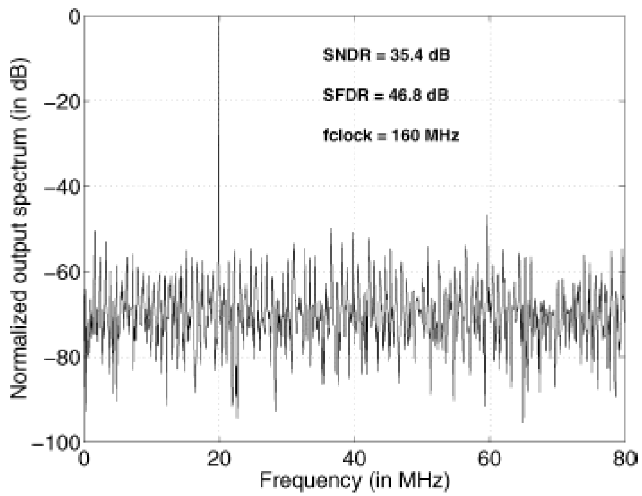




Fig. 19. Normalized output spectrum of the ADC.

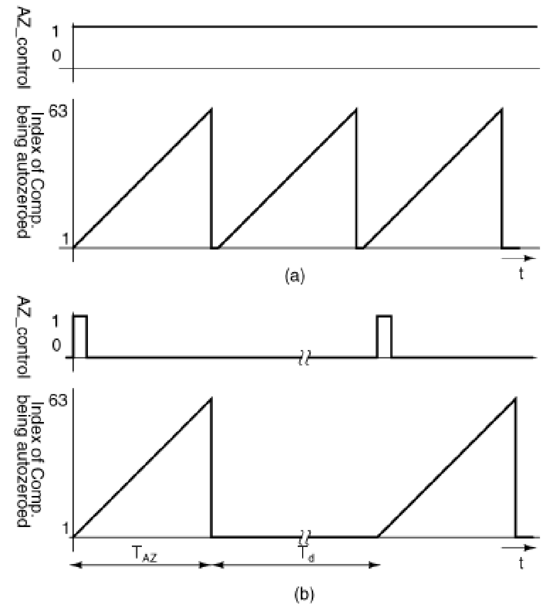
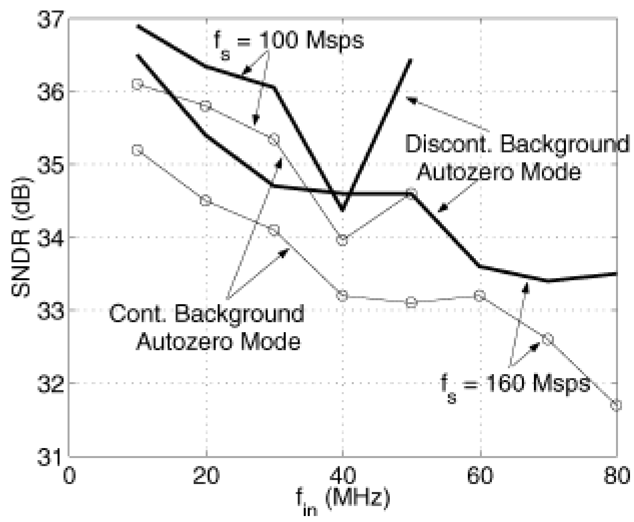
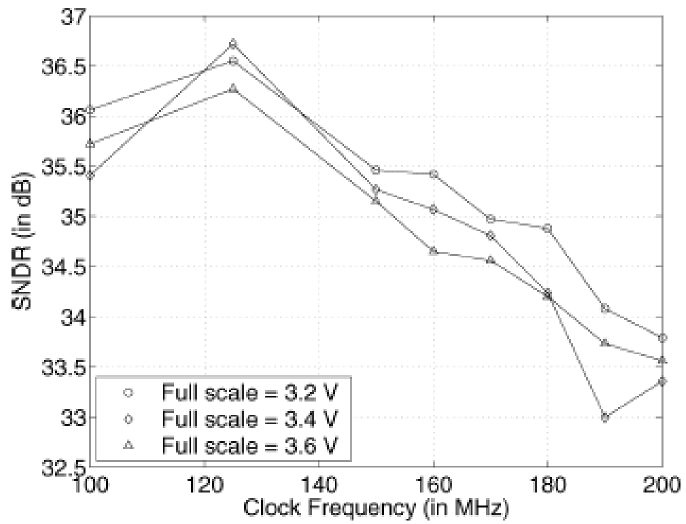



Fig. 20. Illustration of (a) continuous background autozero mode and (b) discontinuous background autozero mode.

# Test Results




Summary of ADC Performance

| | |
|---|---|
| Resolution | 6 bits |
| Technology | 0.35-$\mu$m CMOS 2P4M |
| Supply voltage | 3.3 V |
| Nominal input swing | 3.4 $V_{pp}$ differential |
| DNL (nominal input range) | 0.3 LSB |
| INL (nominal input range) | 0.3 LSB |
| SNDR | 36.0 dB @ $f_{in}$ =49.9 MHz, $f_s$ =100 MHz<br>33.6 dB @ $f_{in}$ =79.9 MHz, $f_s$ =160 MHz |
| Power consumption | 50 mW @ $f_s$ =160 MHz |
| Active Area | 2.0×0.4 mm$^2$ |
| Chip package | DIP40 |

## Figure of Merit

$$\frac{\text{Energy}}{(\text{conversion\_step})} = \frac{P_{\text{diss}}}{2^{\text{ENOB}} \times f_{\text{samp}}}$$

# Title

# References


1. Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters," 2nd Ed., Springer, 2005.
2. M. Gustavsson, J. Wikner, N. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, 2000.