Data Converter Basics

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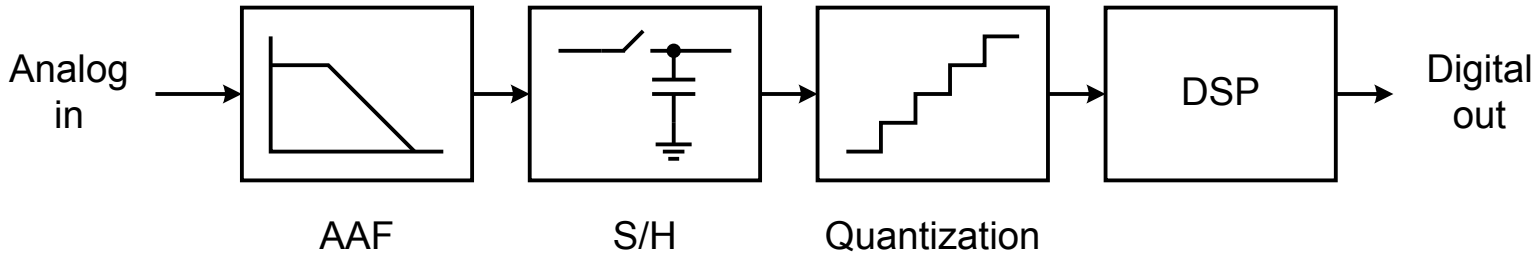
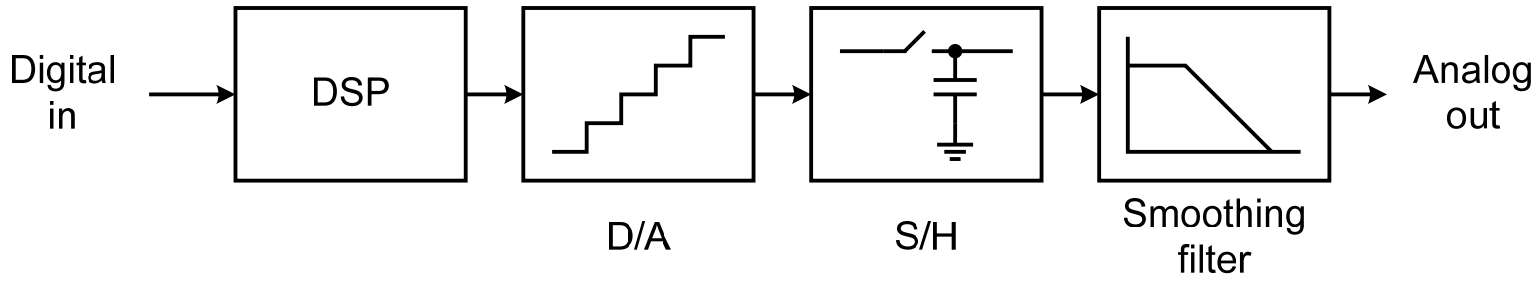
A/D and D/A Conversion

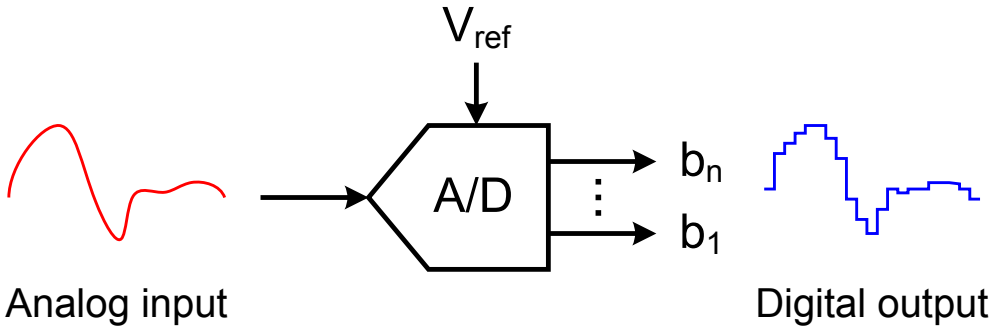
A/D Conversion



D/A Conversion



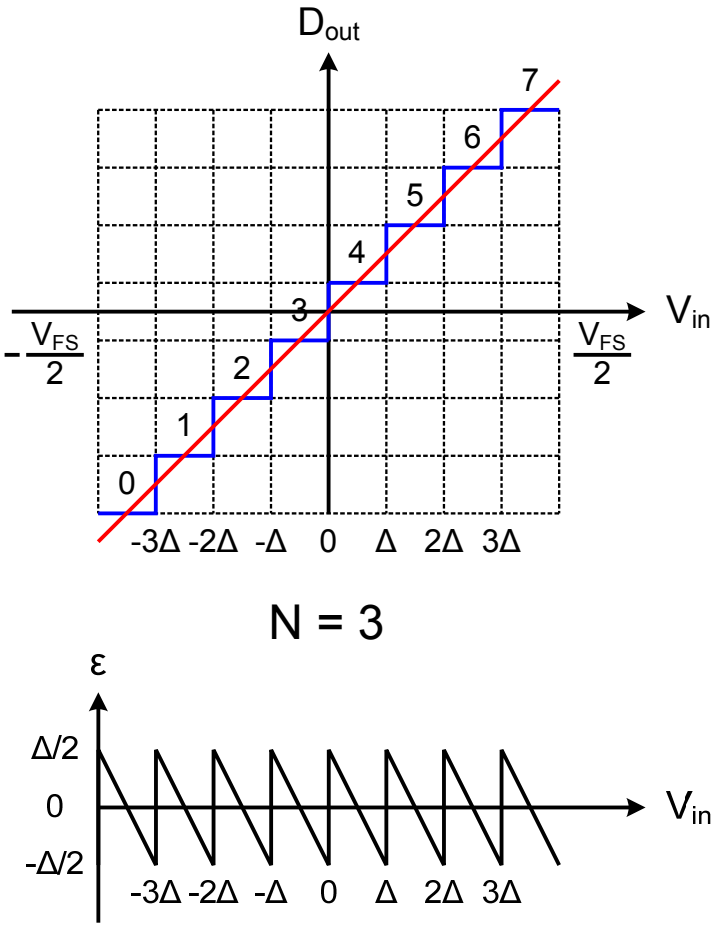
Quantization



$$\underline{\text{Division}}: \quad D_{out} = \left\lfloor 2^N \cdot \frac{V_{in}}{V_{FS}} \right\rfloor$$

- Quantization = division + normalization + truncation
- Full-scale range (V_{FS}) is determined by V_{ref}

Quantization Error



$$\Delta = \frac{V_{FS}}{2^N} = LSB$$

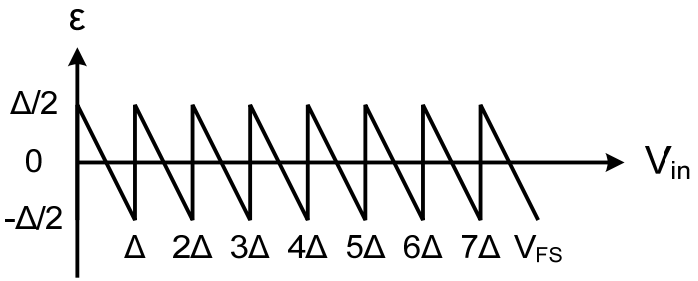
$$V_{in} \in [0, V_{FS}]$$

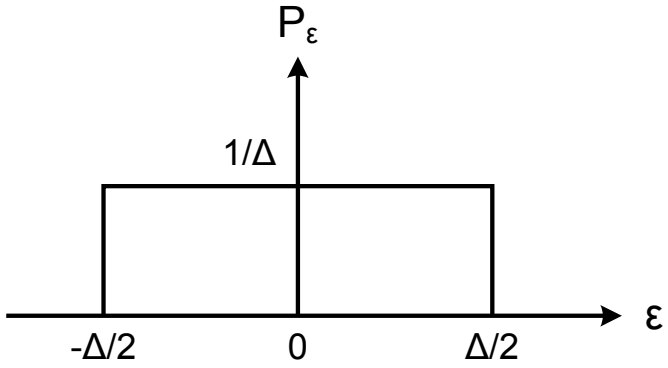
$$\varepsilon = D_{out}\Delta - V_{in} = D_{out}\left(\frac{V_{FS}}{2^N}\right) - V_{in}$$

$$-\frac{\Delta}{2} \le \varepsilon \le \frac{\Delta}{2}$$

"Random" quantization error is usually regarded as noise

Quantization Noise





Assumptions:

- N is large
- $0 \le V_{in} \le V_{FS}$ and $V_{in} >> \Delta$
- V_{in} is active
- ε is Uniformly distributed
- Spectrum of ε is white

$$\sigma_\varepsilon^2 = \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 \cdot \frac{1}{\Delta} \cdot d\varepsilon = \frac{\Delta^2}{12}$$

Signal-to-Quantization Noise Ratio (SQNR)

Assume V_{in} is sinusoidal with $V_{p\text{-}p} = V_{FS}$,

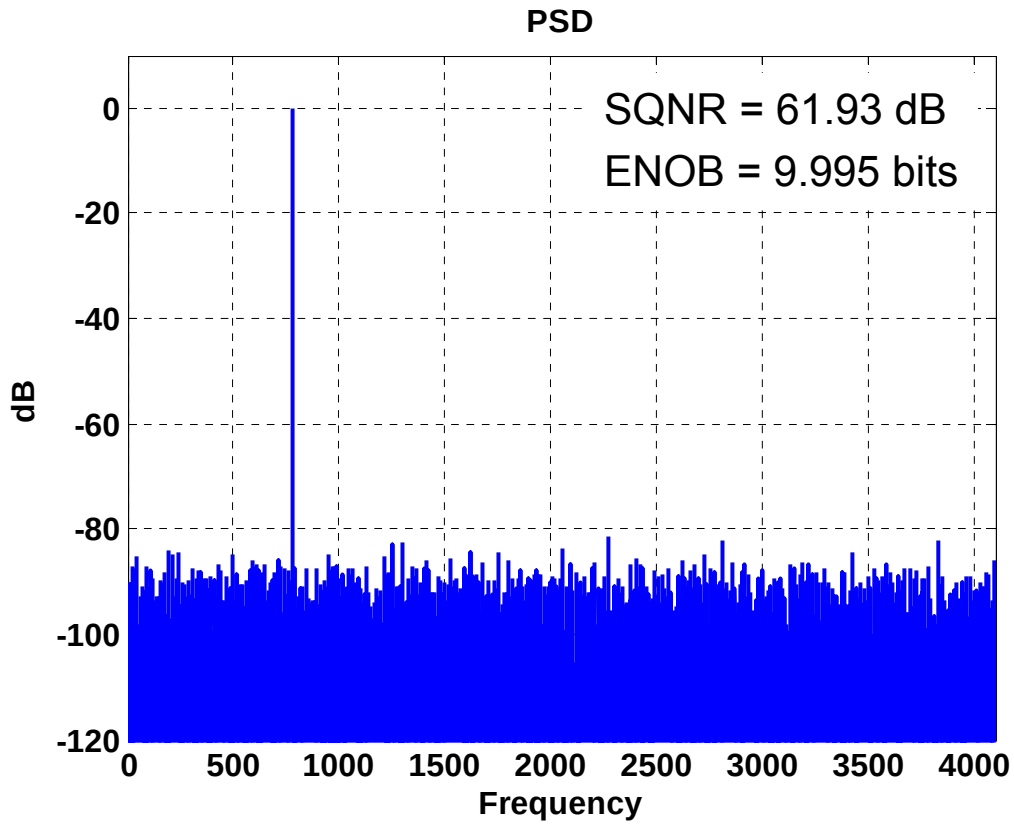
$$SQNR = \frac{V_{FS}^2/8}{\sigma_\varepsilon^2} = \frac{\left(2^N\Delta\right)^2/8}{\frac{\Delta^2}{12}} = 1.5\times 2^{2N},$$

$$SQNR = 6.02\times N + 1.76\ \text{dB}$$

N (bits)	SQNR (dB)
8	49.9
10	62.0
12	74.0
14	86.0

- SQNR depicts the theoretical performance of an ideal ADC
- In reality, ADC performance is limited by many other factors:
  - Electronic noise (thermal, 1/f, coupling/substrate, etc.)
  - Distortion (measured by THD, SFDR, IM3, etc.)

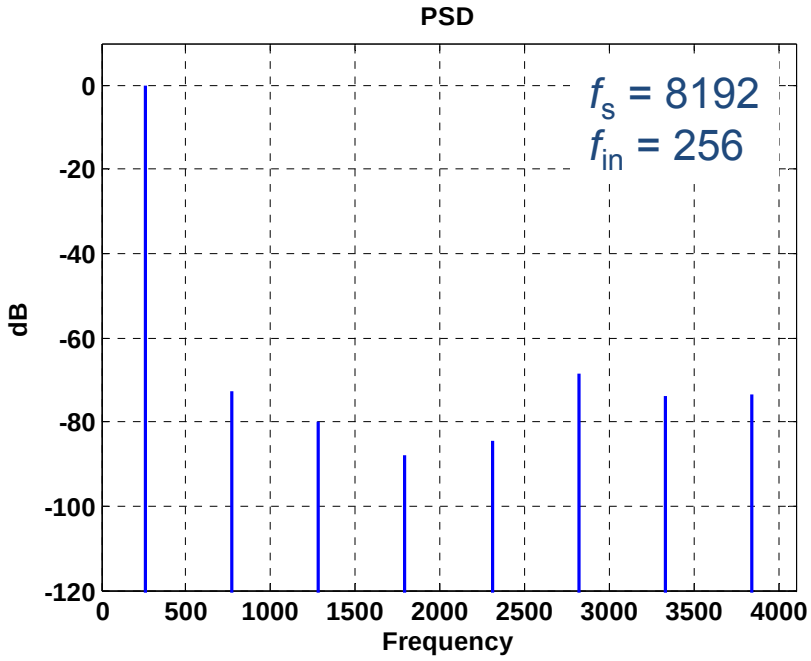
FFT Spectrum of Quantized Signal

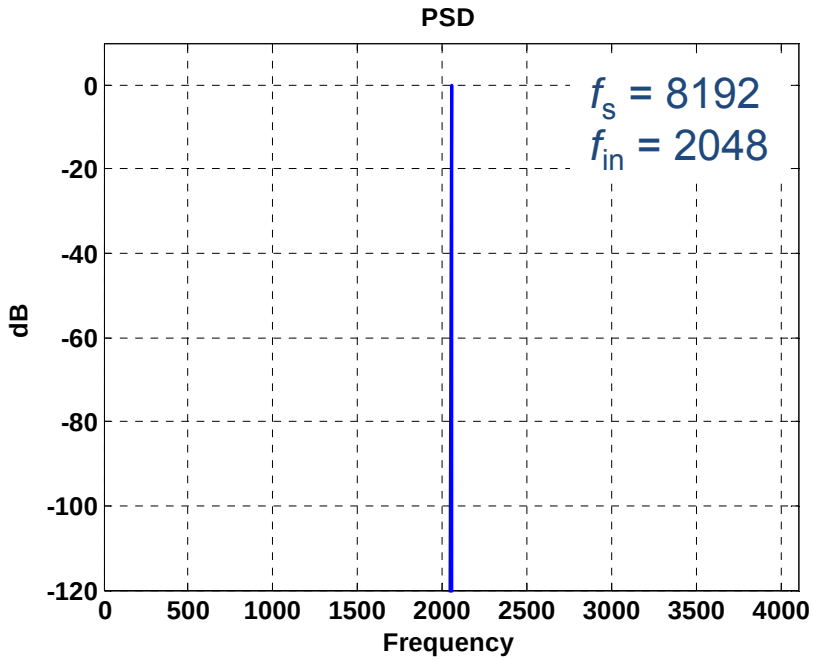


- N = 10 bits
- 8192 samples, only $f = [0, f_s/2]$ shown
- Normalized to V_{in}
- $f_s = 8192$, $f_{in} = 779$
- f_{in} and f_s must be incommensurate

$$\text{ENOB} = \frac{\text{SQNR} - 1.76\,\text{dB}}{6.02\,\text{dB}}$$

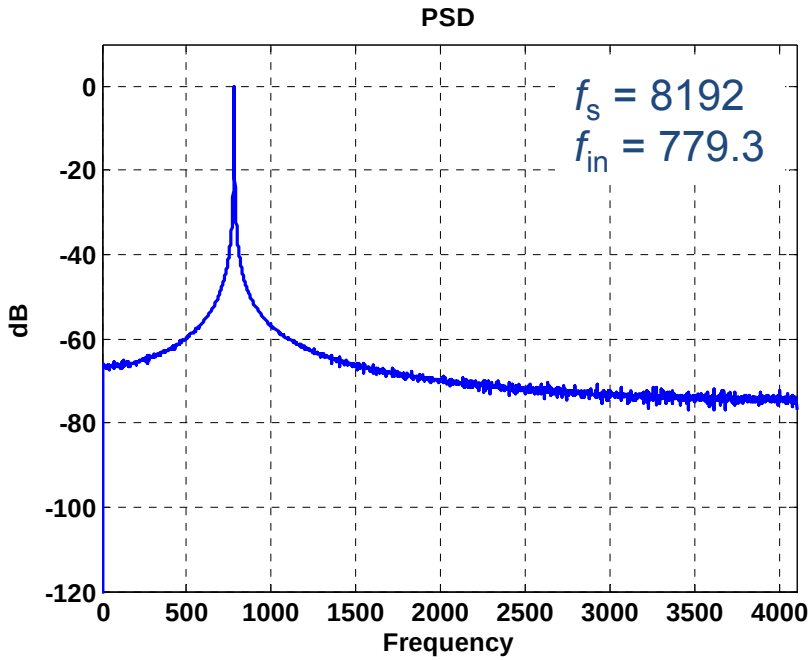
Coherent Sampling

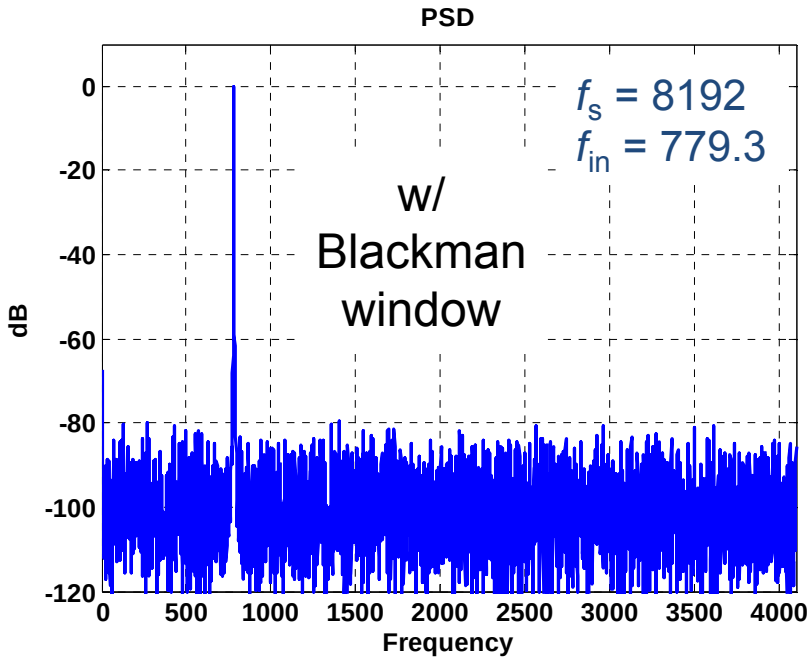




- Periodic sampling points result in periodic quantization errors
- Periodic quantization errors result in harmonic distortion

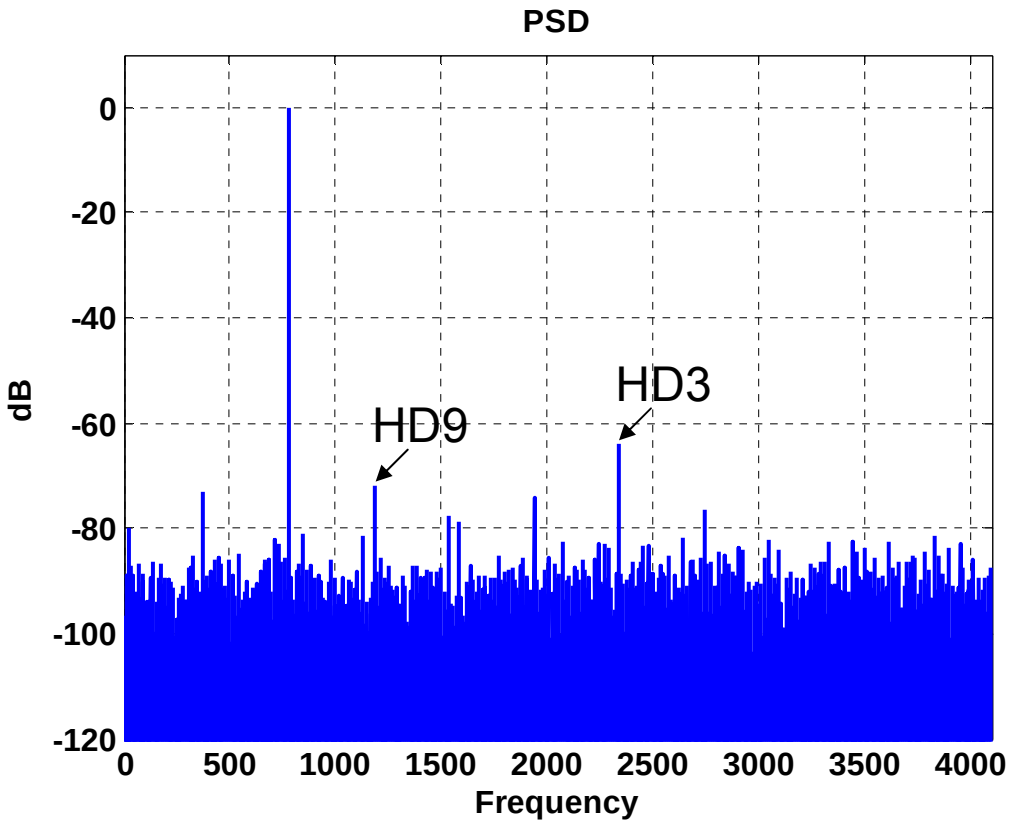
Spectrum Leakage





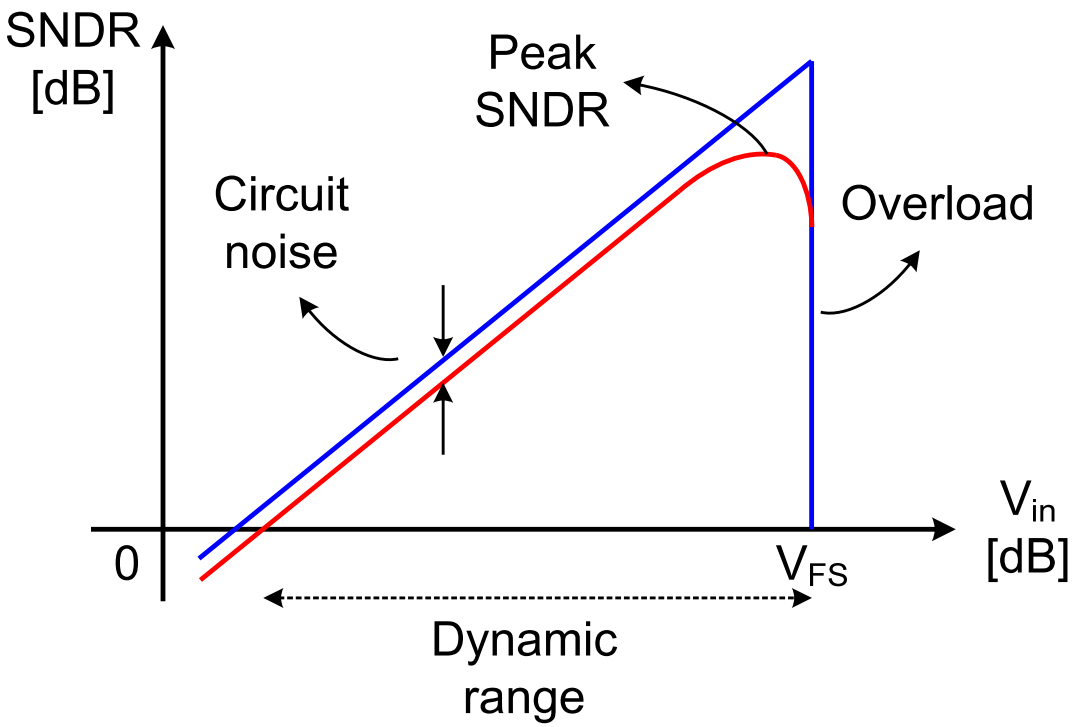
- TD samples must include integer number of cycles of input signal
- Windowing can be applied to eliminate spectrum leakage
- Trade-off b/t main-lobe width and sideband rejection for different windows

FFT Spectrum with Distortion



- High-order harmonics are aliased back, visible in [0, f_s/2] band
- E.g., HD3 @ 779x3+1=2338, HD9 @ 8192-9x779+1=1182

Dynamic Performance



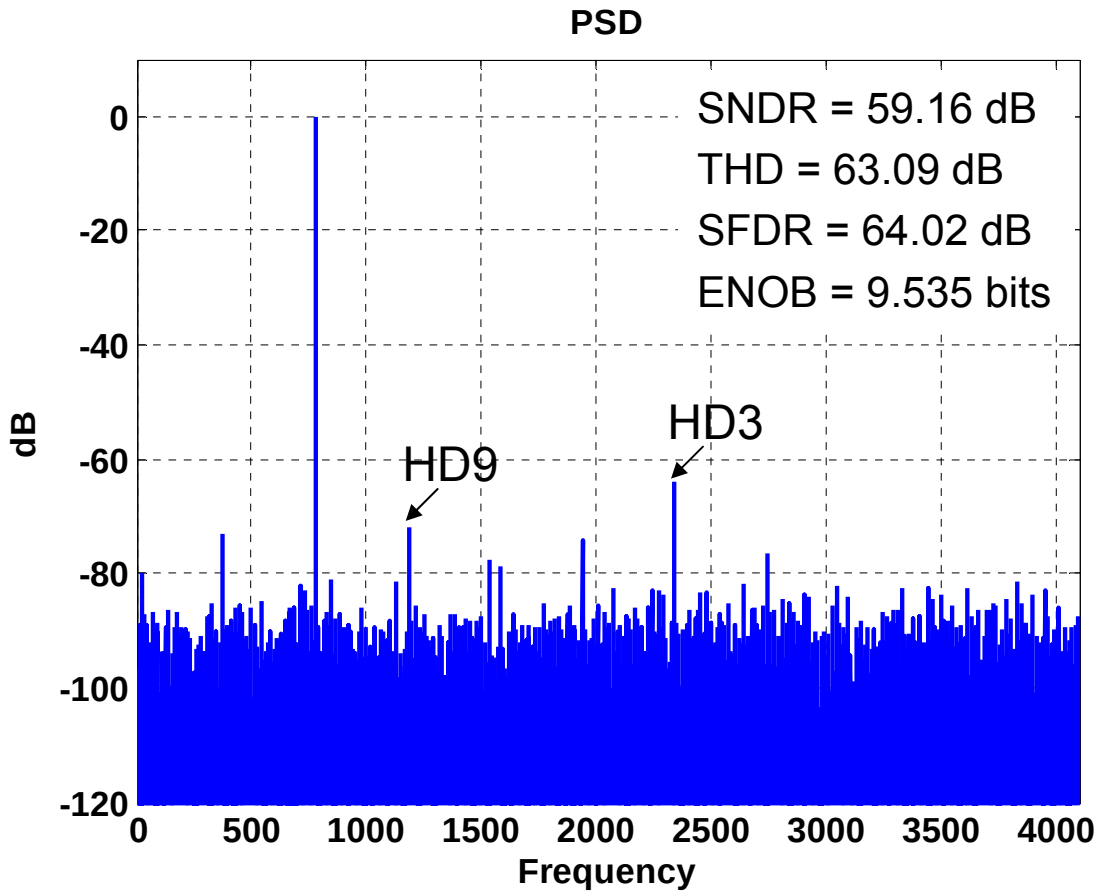
$$\text{SNR} = 10\text{LOG}_{10}\left(\frac{V_{in}^{2}/2}{\Delta^{2}/12+\sigma_{N}^{2}}\right) \propto V_{in}\,[\text{dB}]$$

- Peak SNDR limited by large-signal distortion of the converter
- Dynamic range implies the “theoretical” SNR of the converter

Dynamic Performance Metrics

- Signal-to-quantization-noise ratio (SQNR)
- Total harmonic distortion (THD)
- Signal-to-noise and distortion ratio (SNDR or SINAD)
- Spurious-free dynamic range (SFDR)
- Two-tone intermodulation product (IM3)
- Aperture uncertainty (related to the frontend S/H and clock)
- Dynamic range (DR)

Evaluating Dynamic Performance



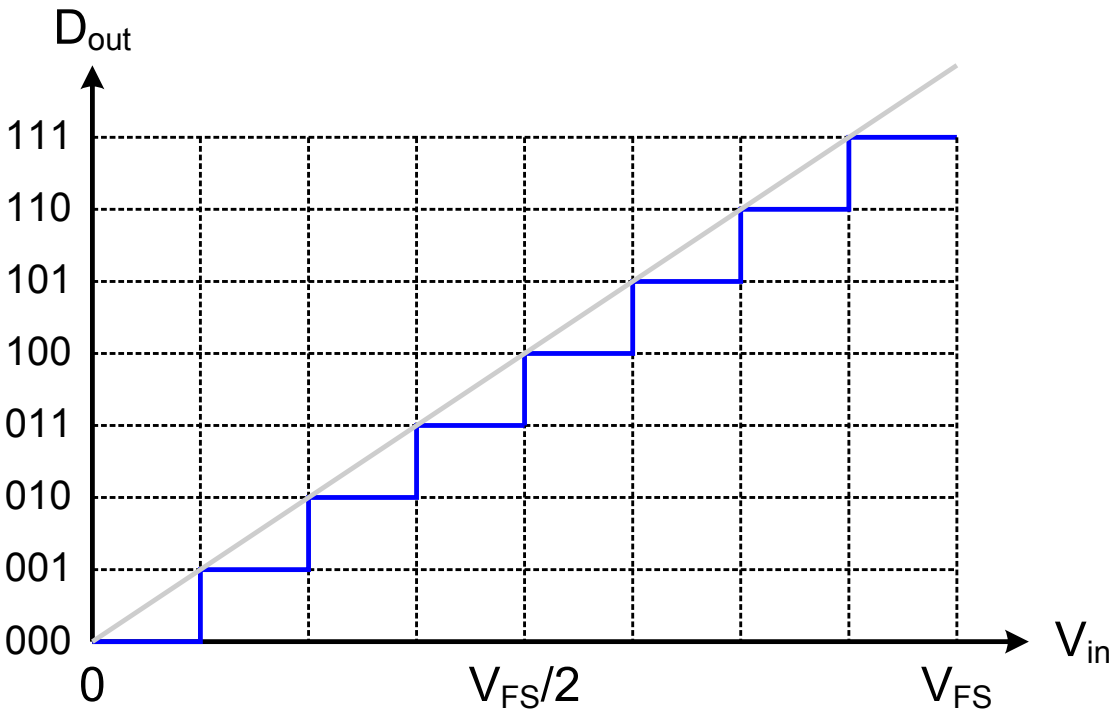
- Signal-to-noise plus distortion ratio (SNDR)
- Total harmonic distortion (THD)
- Spurious-free dynamic range (SFDR)

$$\text{ENOB} = \frac{\text{SNDR} - 1.76\ \text{dB}}{6.02\ \text{dB}}$$

Static Performance Metrics

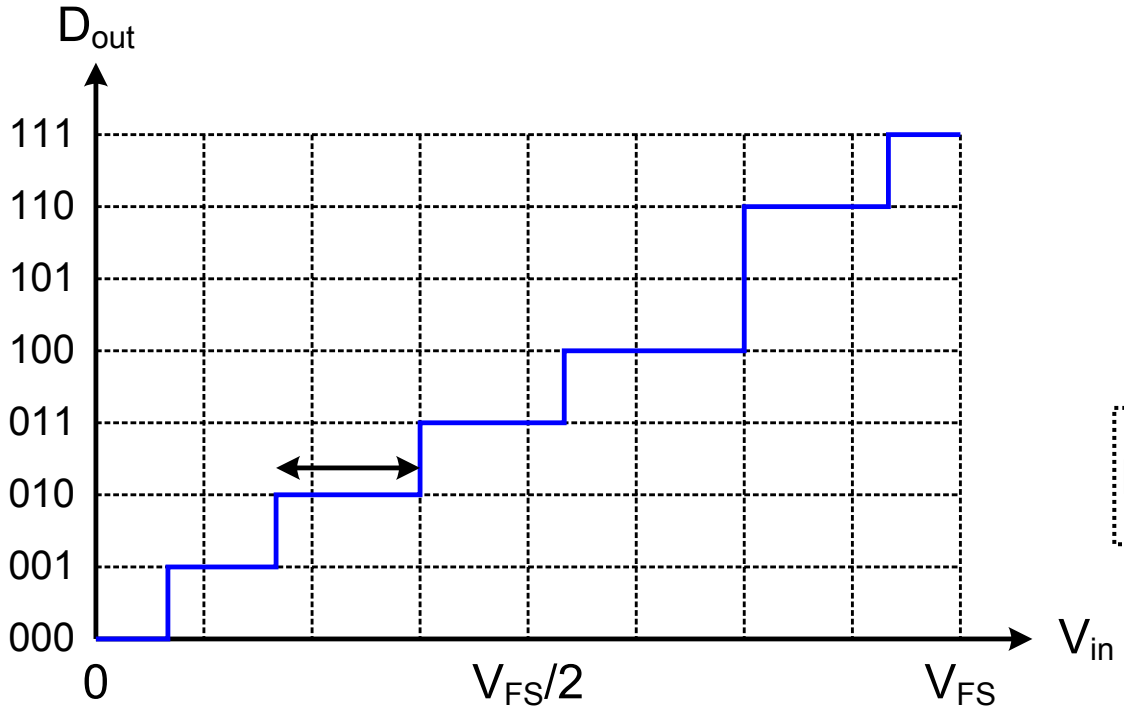
- Offset (OS)
- Gain error (GE)
- Monotonicity
- Linearity
  - Differential nonlinearity (DNL)
  - Integral nonlinearity (INL)

Ideal ADC Transfer Characteristic



Note the systematic offset! (floor, ceiling, and round)

DNL and Missing Code

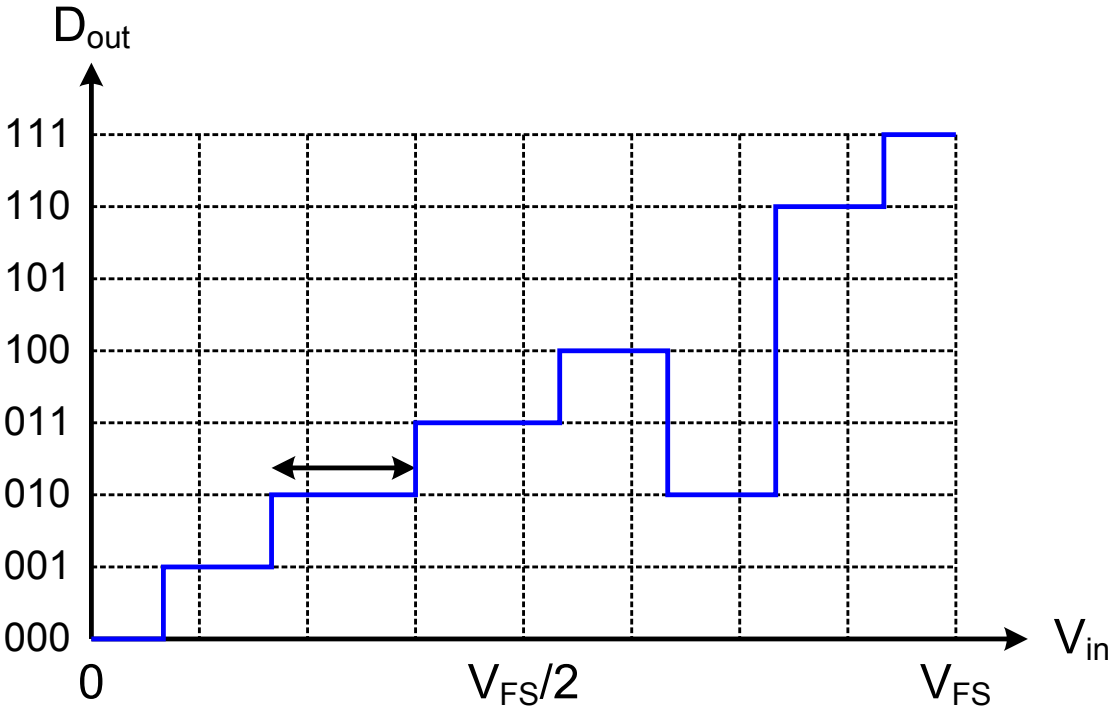


- DNL = ?
- Can DNL < -1?

$$DNL_i = \frac{i^{th}\ \text{Step Size} - \Delta}{\Delta}$$

DNL = deviation of an input step width from 1 LSB (= $V_{FS}/2^N = \Delta$)

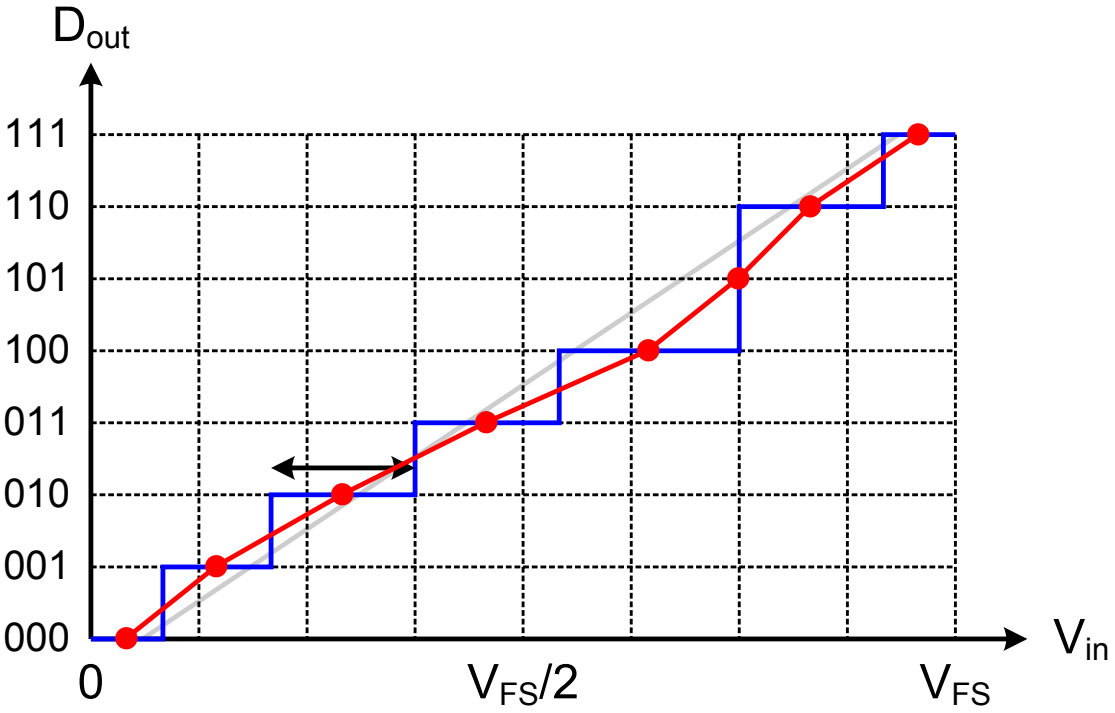
DNL and Nonmonotonicity



- DNL = ?
- How can we even measure this?

DNL = deviation of an input step width from 1 LSB (= $V_{FS}/2^N = \Delta$)

INL



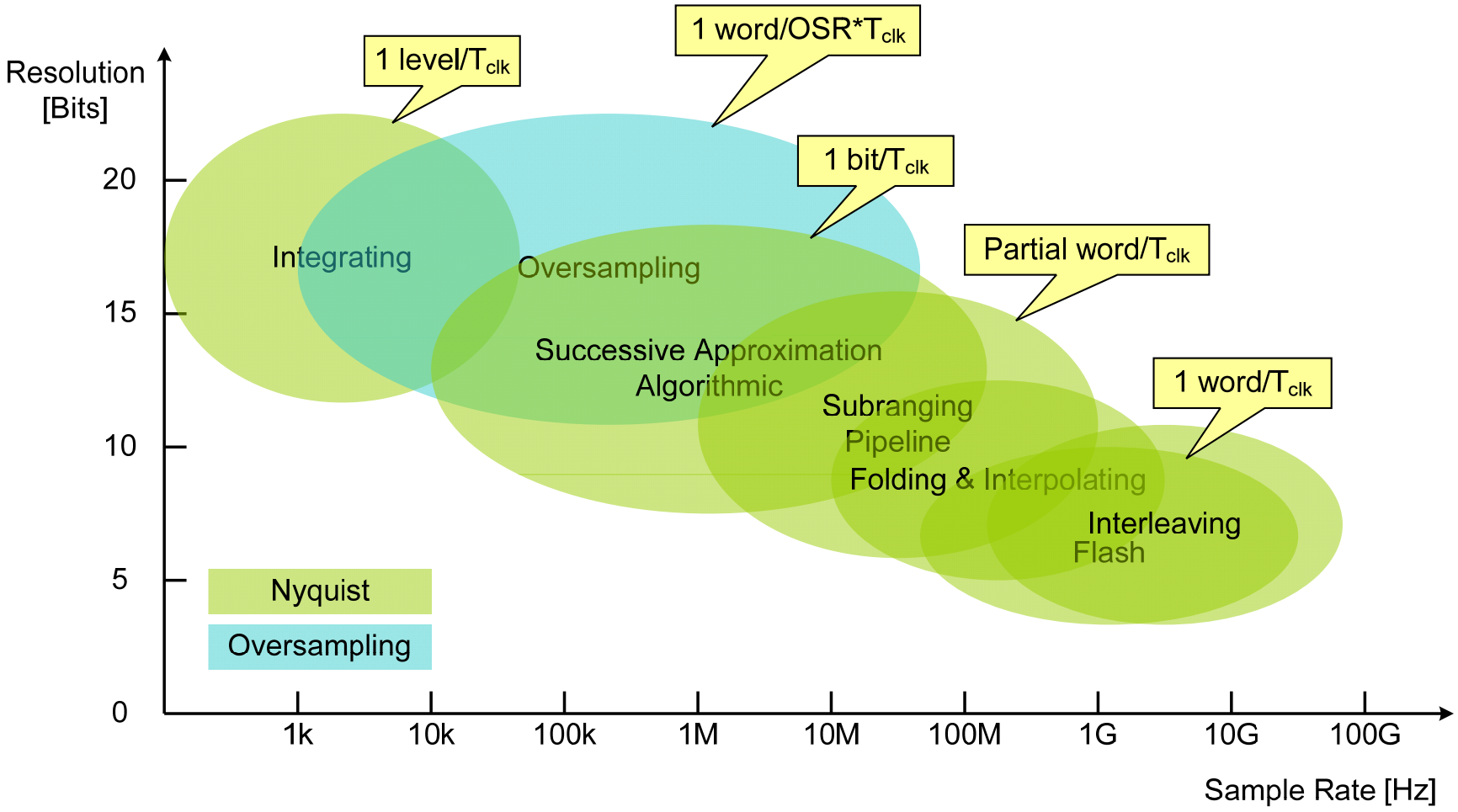
Any code

- Missing?
- Nonmonotonic?

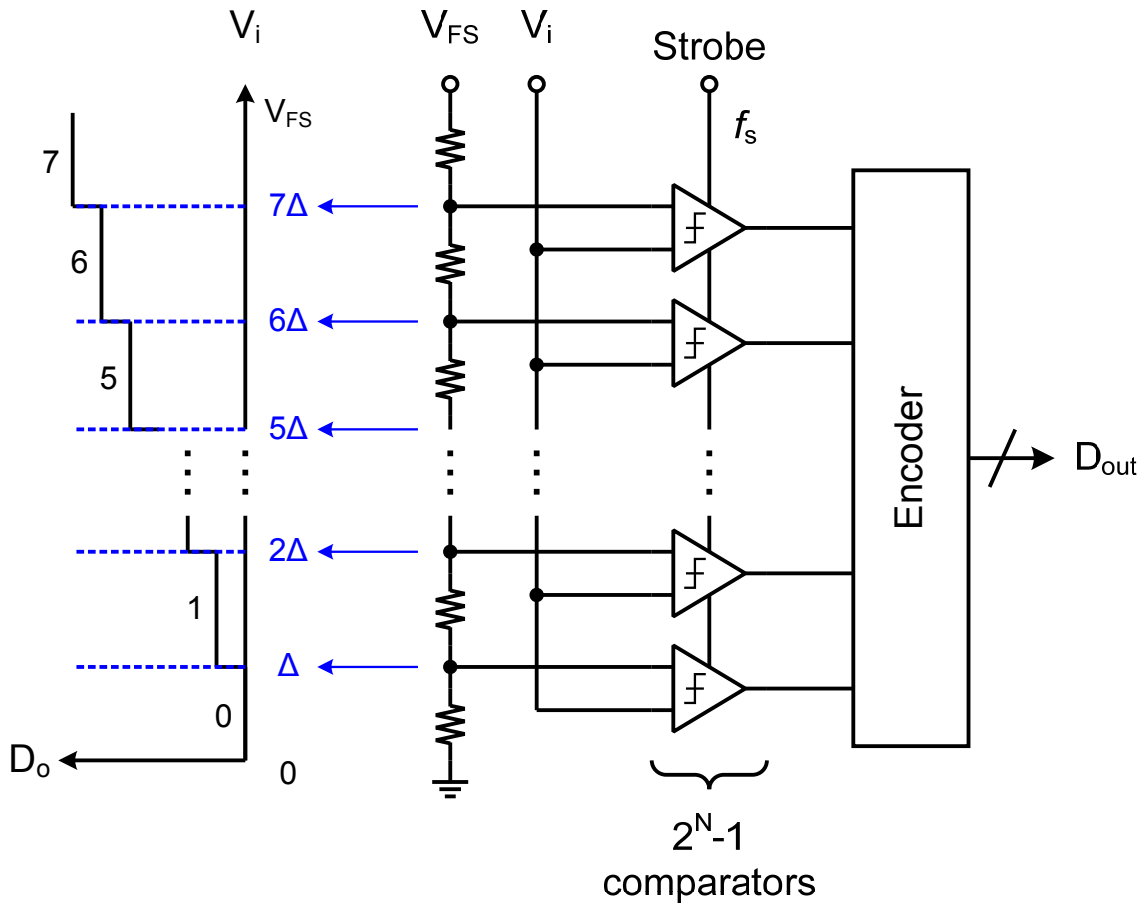
INL = deviation of the step midpoint from the ideal step midpoint

(method I and II …)

Accuracy-Speed Tradeoff

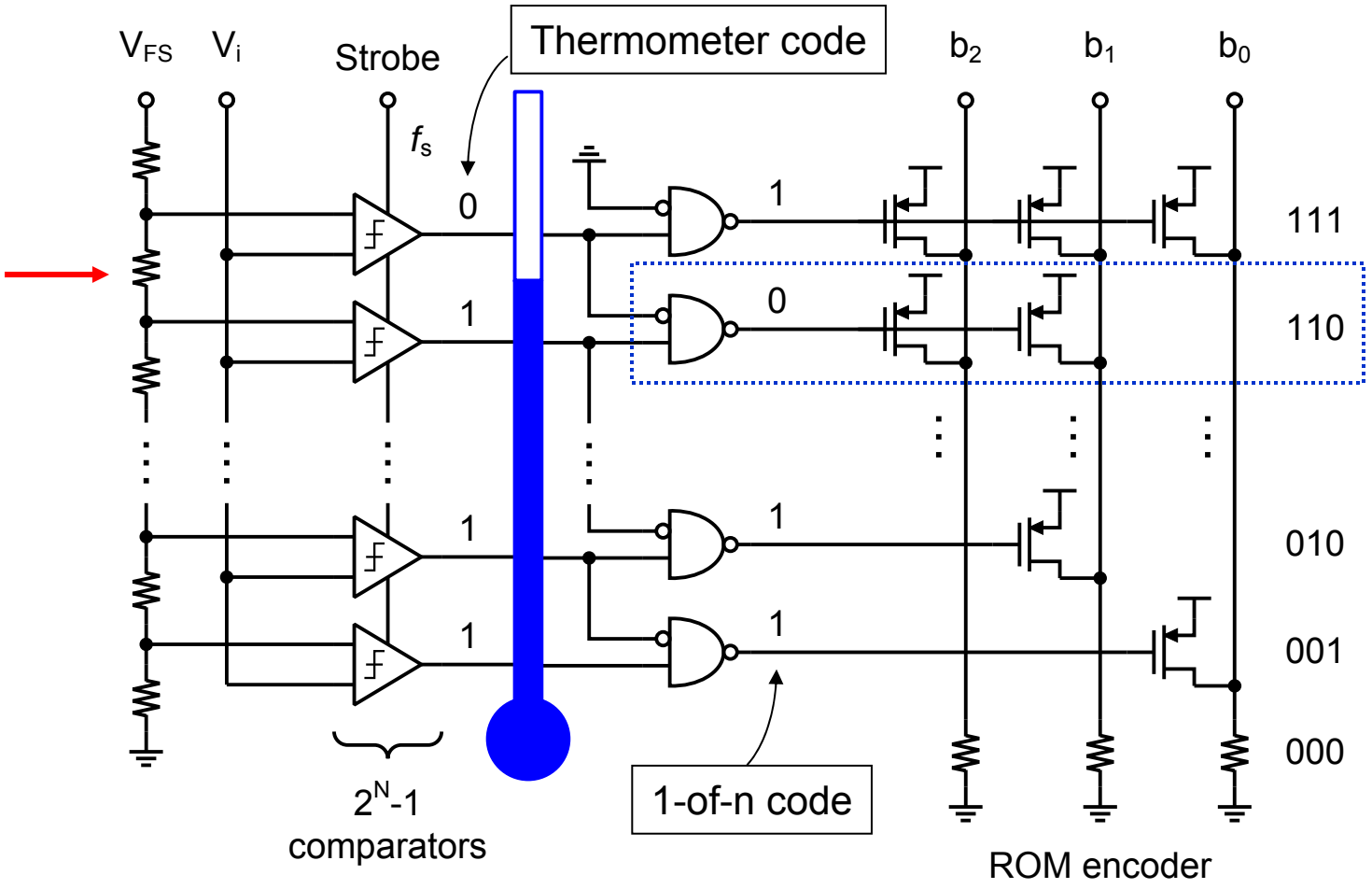


Flash ADC Architecture

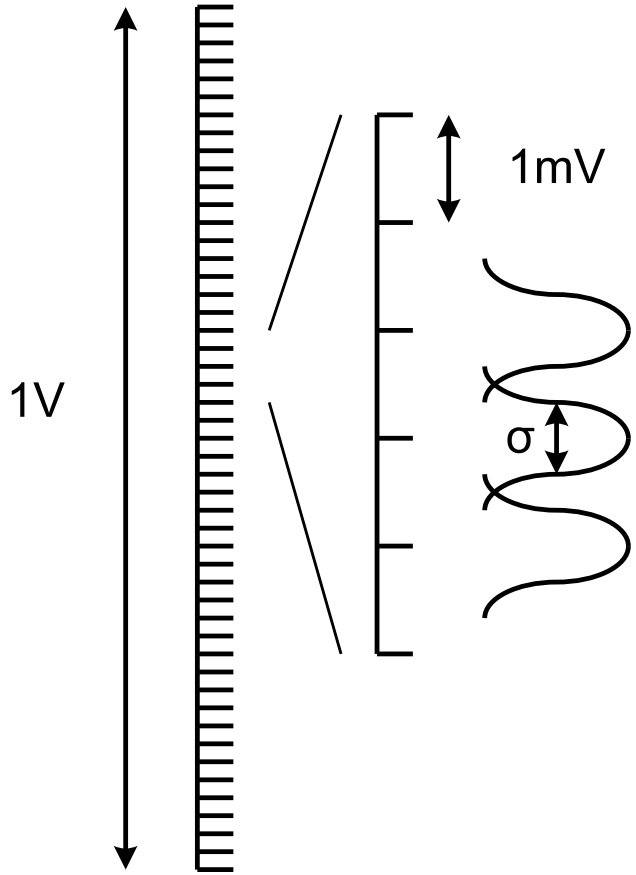


- Reference ladder consists of 2^N equal size resistors
- Input is compared to 2^N-1 reference voltages
- Massive parallelism
- Very fast ADC architecture
- Latency = 1 T = $1/f_s$
- Throughput = f_s
- Complexity = 2^N

Thermometer Code



Flash ADC Challenges



- V_{DD} = 1.8 V
- 10-bit → 1023 comparators
- V_{FS} = 1 V → 1 LSB = 1 mV
- DNL < 0.5 LSB → V_{os} < 0.5 LSB
- 0.5 mV = 3-5 σ → σ = 0.1-0.2 mV

- 2^N-1 very large comparators
- Large area, large power consumption
- Very sensitive design
- Limited to resolutions of 4-8 bits

References

1. Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters,” 2nd Ed., Springer, 2005.
2. M. Gustavsson, J. Wikner, N. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, 2000.