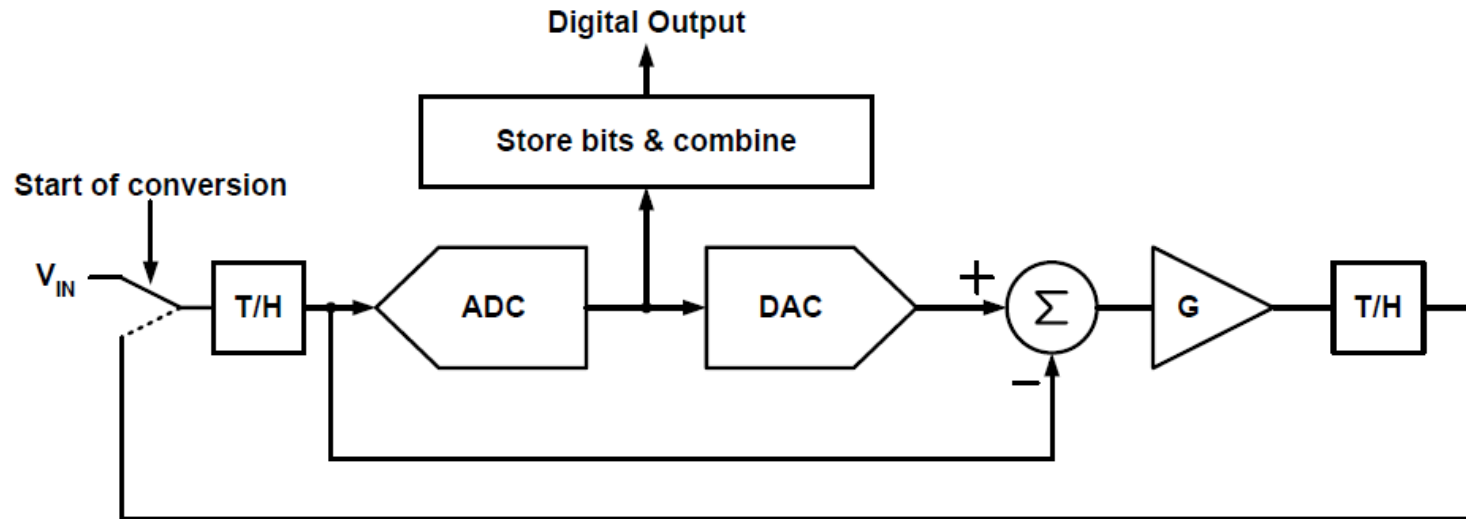


Algorithmic and Integrating ADCs

Vishal Saxena, Boise State University
(vishalsaxena@boisestate.edu)

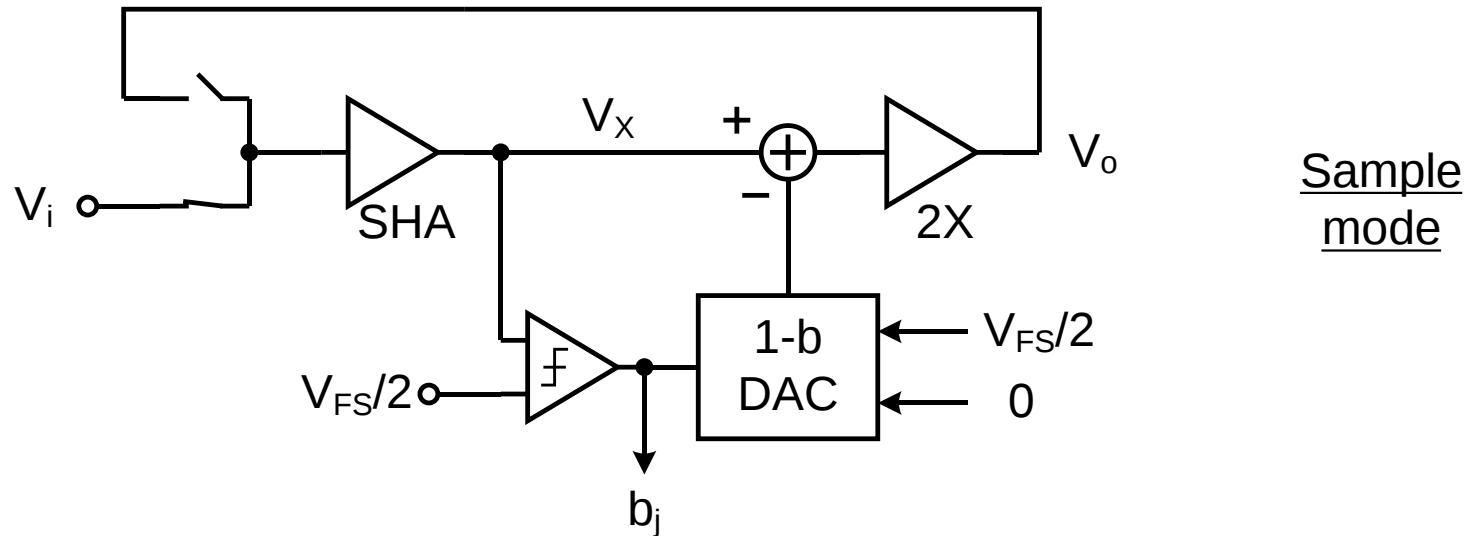
Algorithmic (Cyclic) ADC

Algorithmic (Cyclic) ADC



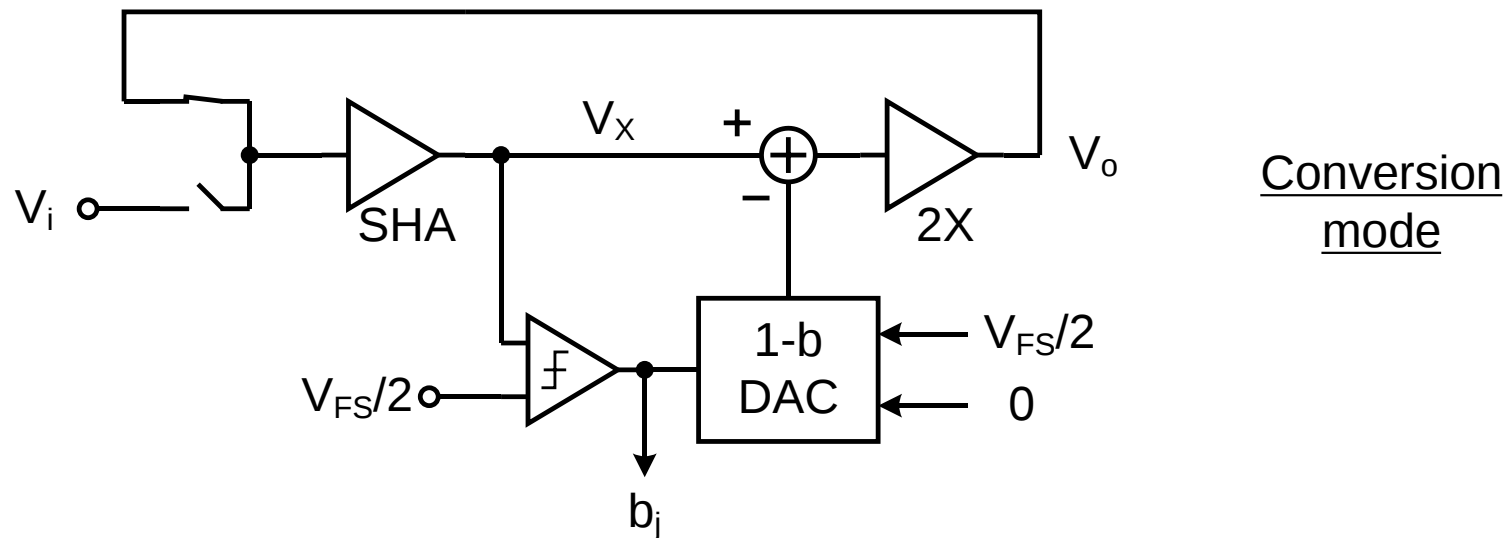
- Essentially same as pipeline
- But a single MDAC stage is used in a cyclic fashion for all operations
- Need many clock cycles per conversion

Algorithmic (Cyclic) ADC



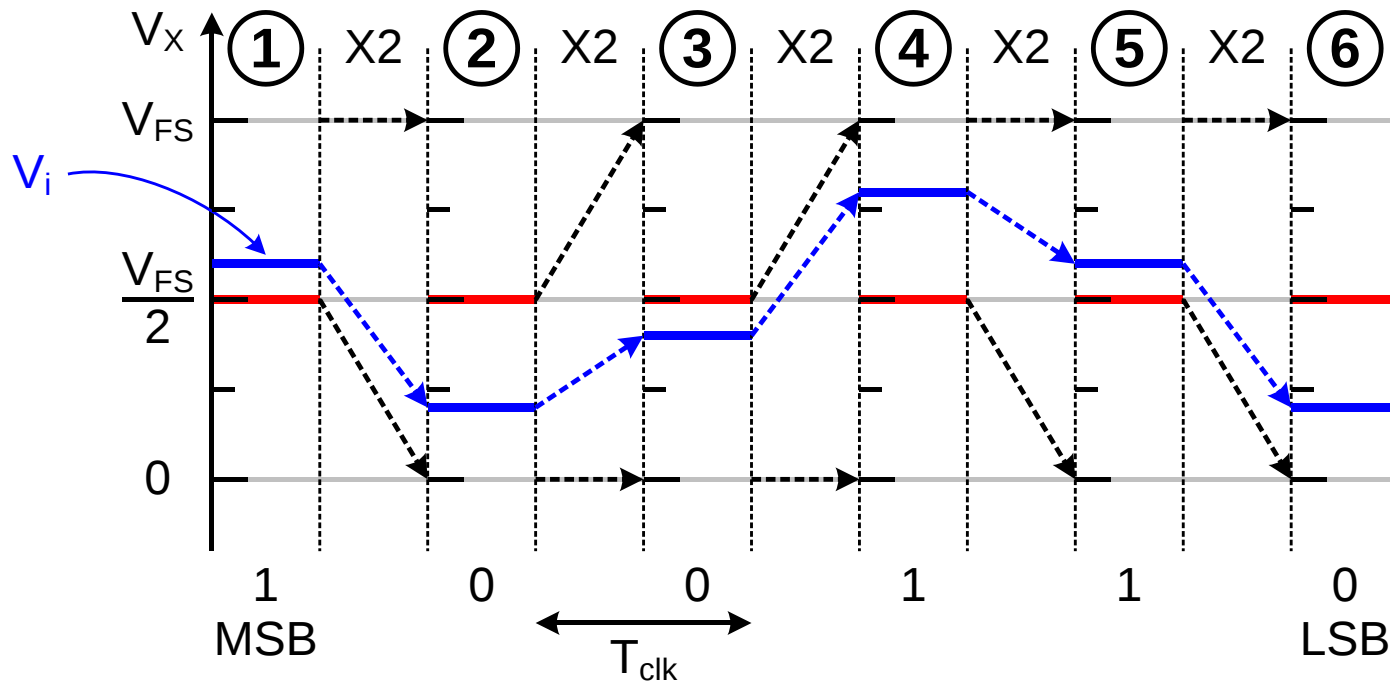
- Input is sampled first, then circulates in the loop for N clock cycles
- Conversion takes N cycles with one bit resolved in each T_{clk}

Modified Binary Search



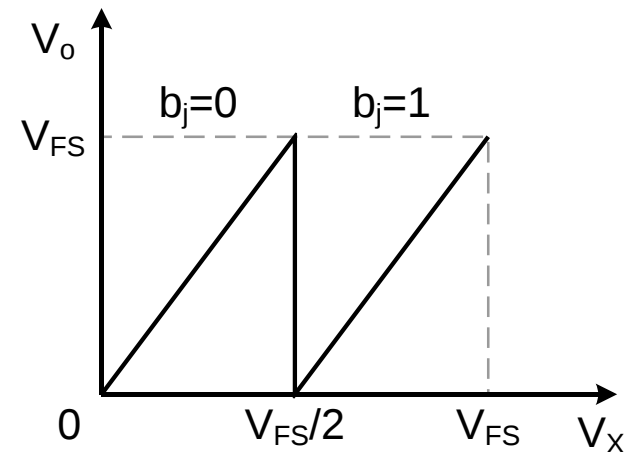
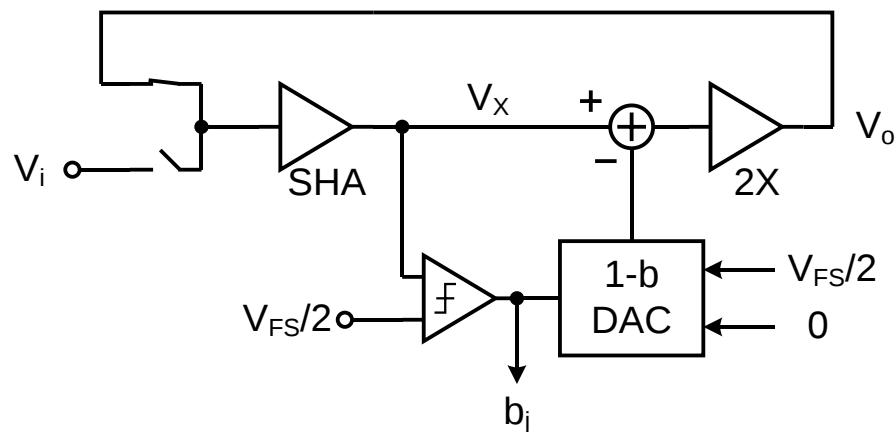
- If $V_x < V_{FS}/2$, then $b_j = 0$, and $V_o = 2 \cdot V_x$
- If $V_x > V_{FS}/2$, then $b_j = 1$, and $V_o = 2 \cdot (V_x - V_{FS}/2)$
- V_o is called conversion “**residue**”
- RA = residue amplifier

Modified Binary Search



- Constant threshold ($V_{FS}/2$) is used for each comparison
- Residue experiences 2X gain each time it circulates the loop

Loop Transfer Function



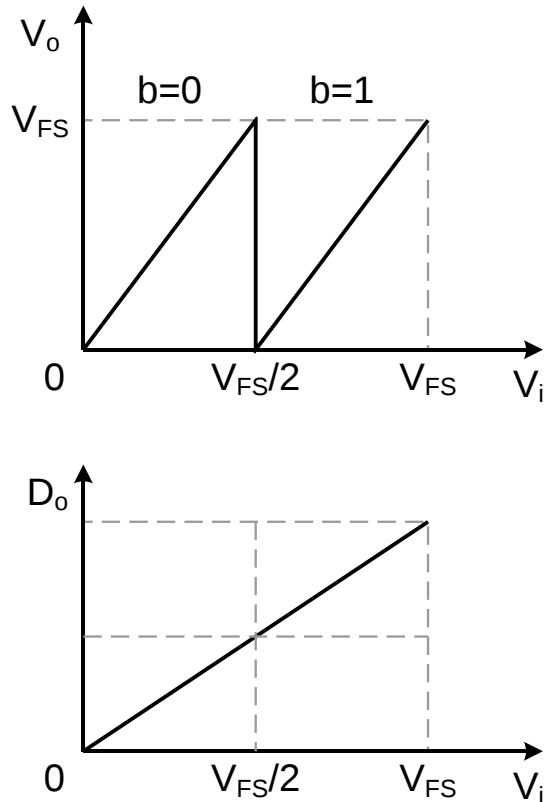
- Comparison $\rightarrow$ if $V_X < V_{FS}/2$, then $b_j = 0$; otherwise, $b_j = 1$
- Residue generation $\rightarrow V_o = 2 \cdot (V_X - b_j \cdot V_{FS}/2)$

Algorithmic ADC

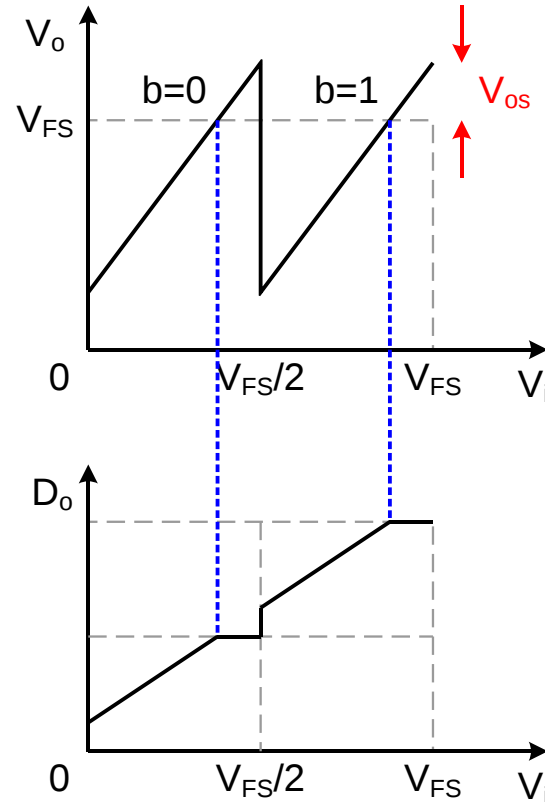
- Hardware-efficient, but relatively low conversion speed (bit-per-step)
- Modified binary search algorithm
- Loop-gain (2X) requires the use of a residue amplifier, but greatly simplifies the DAC $\rightarrow$ 1-bit, inherently linear (why?)
- Residue gets amplified in each circulation; the gain accumulated makes the later conversion steps insensitive to circuit noise and distortion
- Conversion errors (residue error due to comparator offset and/or loop-gain non-idealities) made in earlier conversion cycles also get amplified again and again – overall accuracy is usually limited by the MSB conversion step
- Redundancy is often employed to tolerate comparator/loop offsets
- Trimming/calibration/ratio-independent techniques are often used to treat loop-gain error, nonlinearity, etc.

Offset Errors

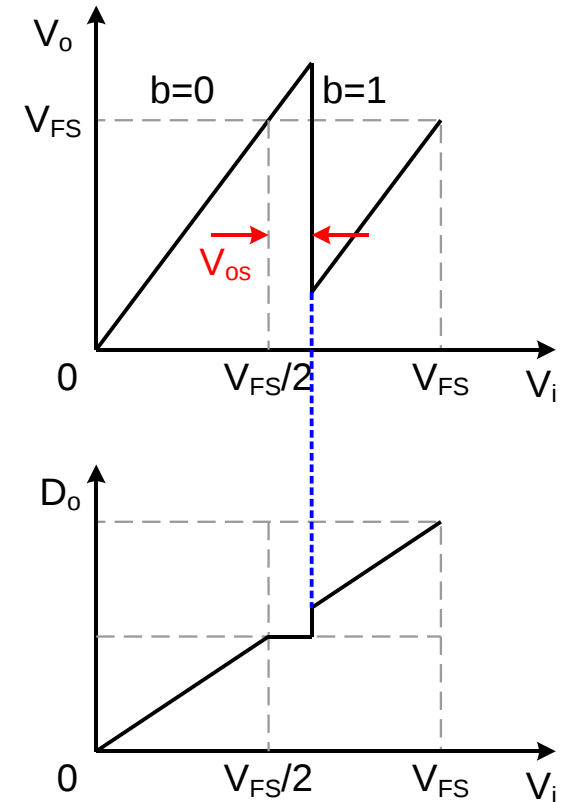
Ideal



RA offset



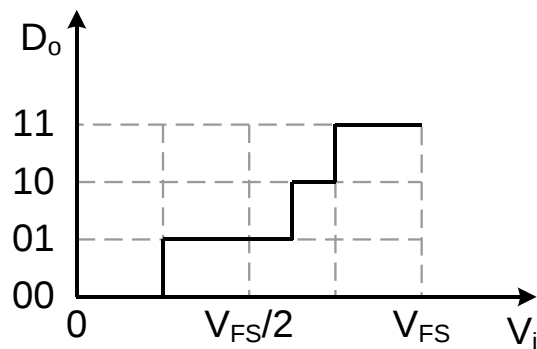
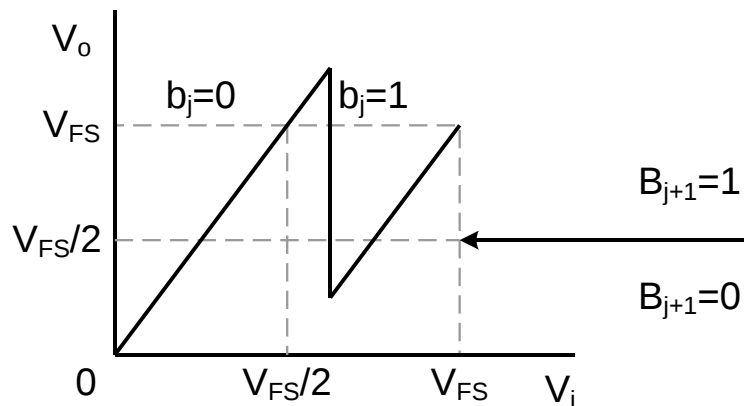
CMP offset



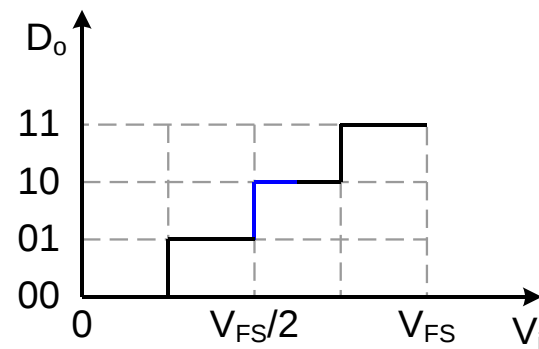
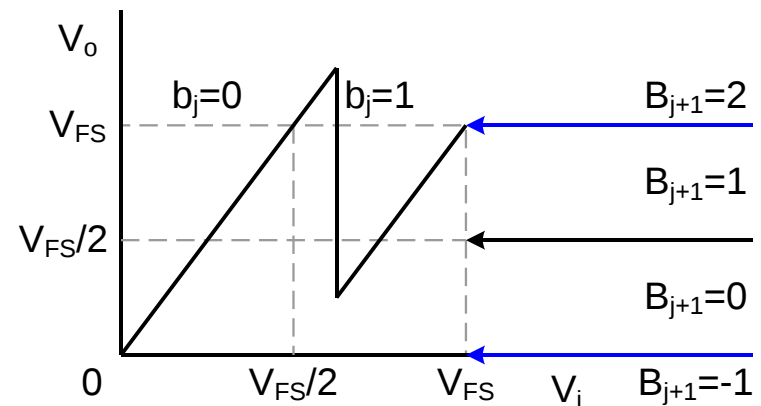
$$V_o = 2 \cdot (V_i - b_j \cdot V_{FS}/2) \rightarrow V_i = b_j \cdot V_{FS}/2 + V_o/2$$

Redundancy (DEC, RSD)

- RSD= Redundant Signed Digit



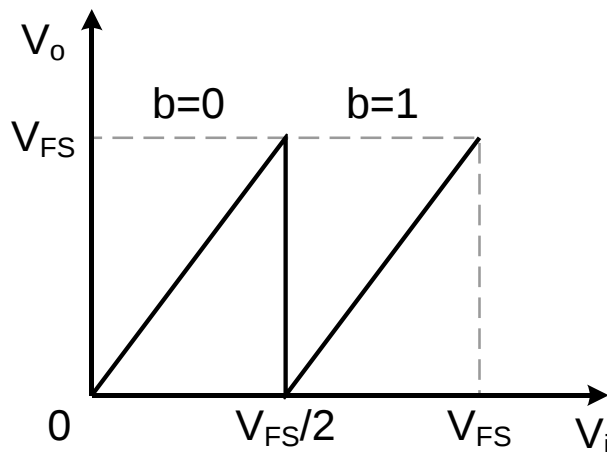
1 CMP



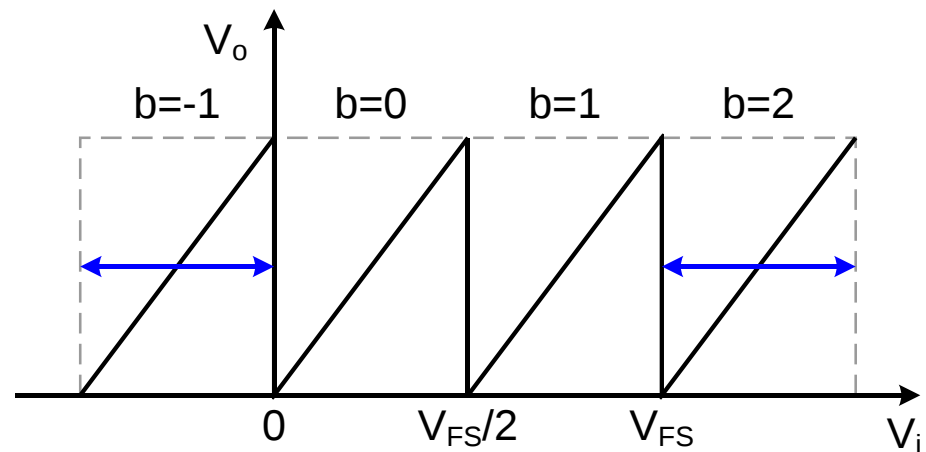
3 CMPs

Loop Transfer Function

Original

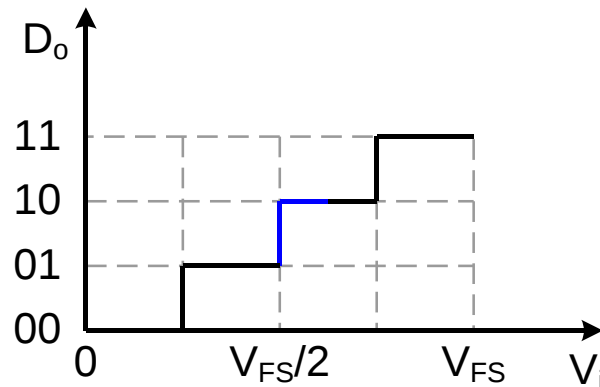
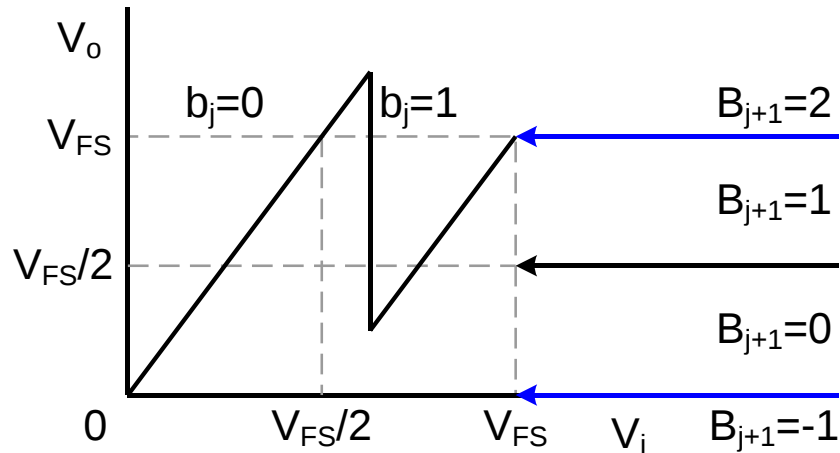


w/ Redundancy



- Subtraction/addition both required to compute final sum
- 4-level (2-bit) DAC required instead of 2-level (1-bit) DAC

Comparator Offset

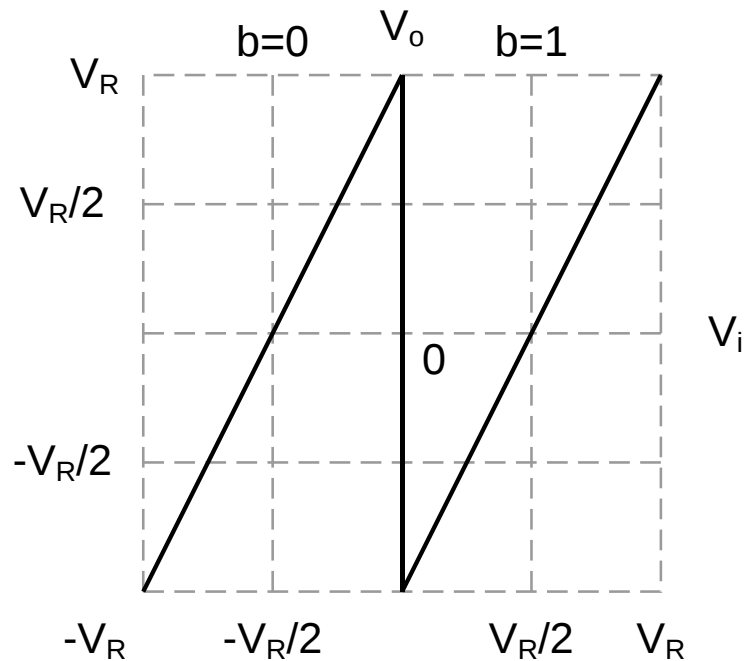


- Max tolerance of comparator offset is $\pm V_{FS}/4 \rightarrow$ simple comparators
- Similar tolerance also applies to RA offset
- Key to understand digital redundancy:

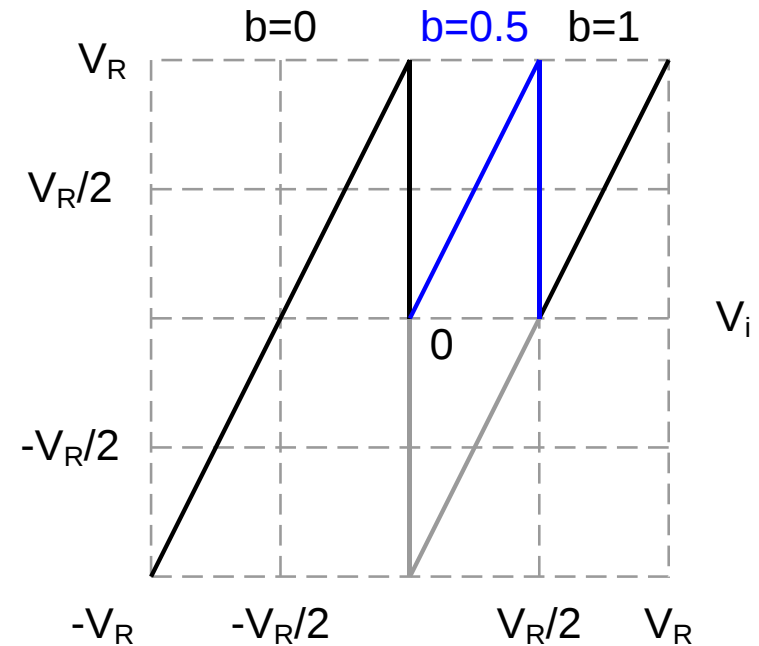
$$V_i = b_j \cdot \frac{V_{FS}}{2} + \frac{V_o}{2}$$

$b_j \Leftrightarrow V_o$

Modified 1-Bit Architecture

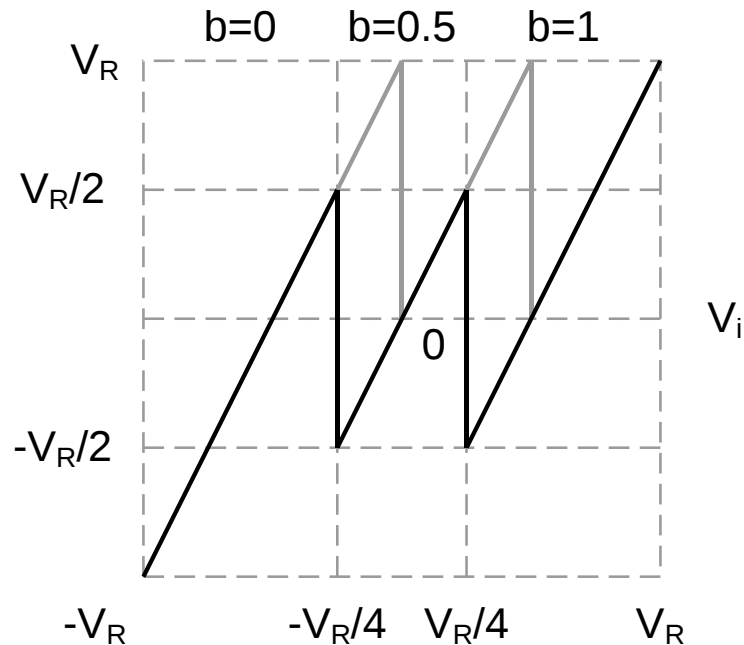


1-b/s RA transfer curve
w/ no redundancy

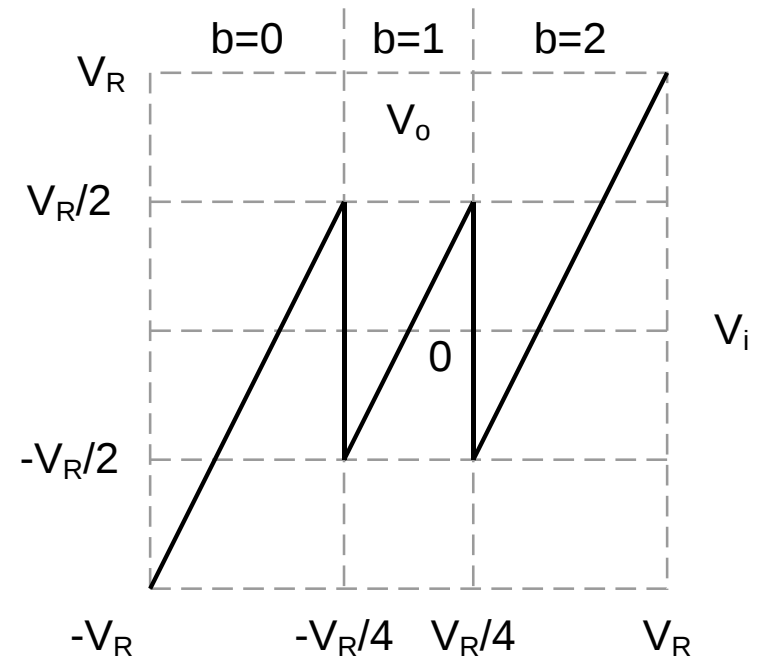


One extra CMP
added at $V_R/2$

From 1-Bit to 1.5-Bit Architecture

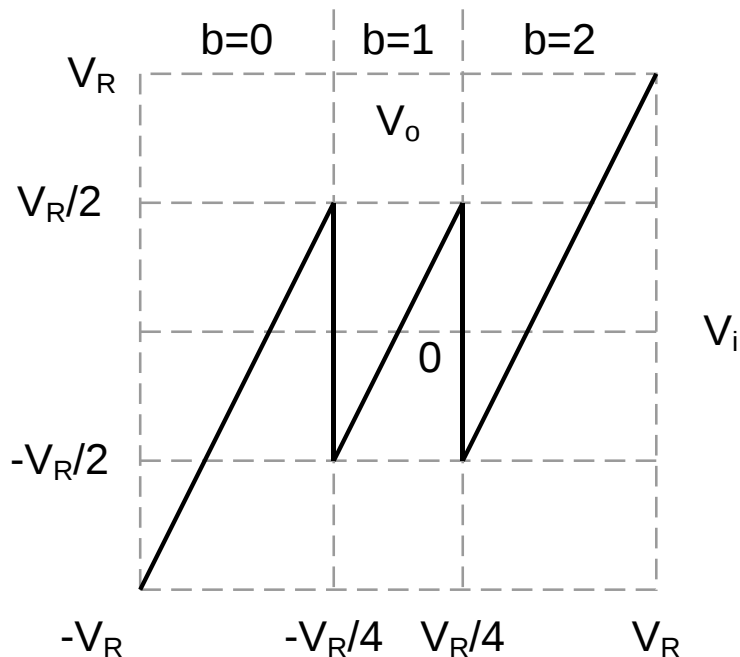


A systematic offset $-V_R/4$ introduced to both CMPs



A 2X scaling is performed on all output bits

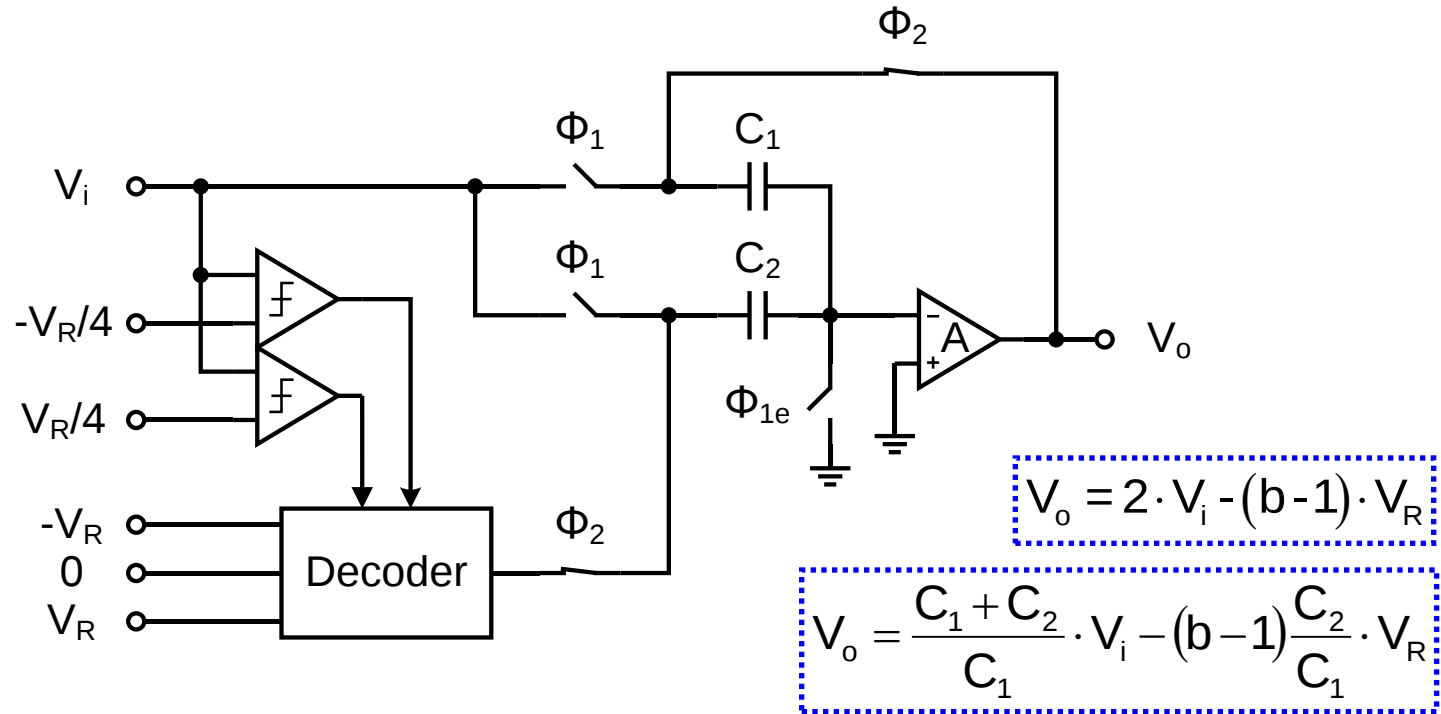
The 1.5-Bit Architecture



$$V_o = 2 \cdot V_i - (b-1) \cdot V_R$$

- 3 decision levels
→ $\text{ENOB} = \log_2 3 = 1.58$
- Max tolerance of comparator offset is $\pm V_R/4$
- An implementation of the Sweeney-Robertson-Tocher (SRT) division principle
- The conversion accuracy solely relies on the loop-gain error, i.e., the gain error and nonlinearity
- A 3-level DAC is required

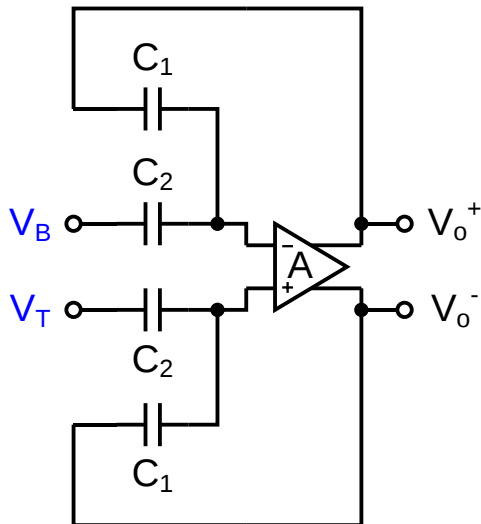
The Multiplier DAC (MDAC)



- 2X gain + 3-level DAC + subtraction all integrated
- A 3-level DAC is perfectly linear in fully-differential form
- Can be generalized to n.5-b/stage architectures

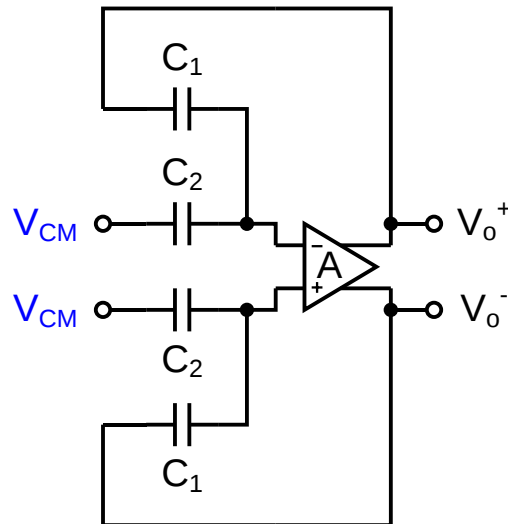
A Linear 3-Level DAC

$b = 0$



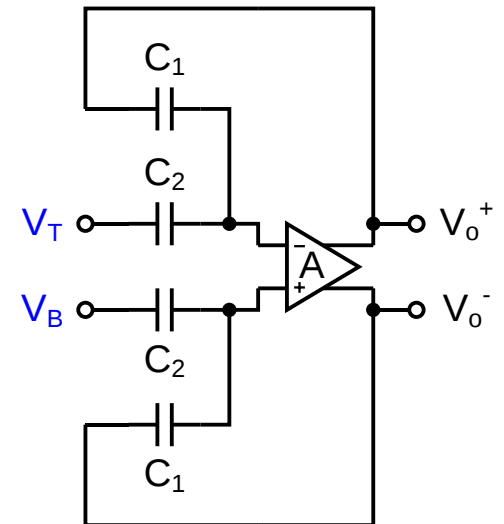
$$\begin{aligned} V_o &= V_o^+ - V_o^- \\ &= \frac{C_1 + C_2}{C_1} \cdot V_i - \frac{C_2}{C_1} \cdot (V_B - V_T) \\ &= 2 \cdot V_i + V_R \end{aligned}$$

$b = 1$



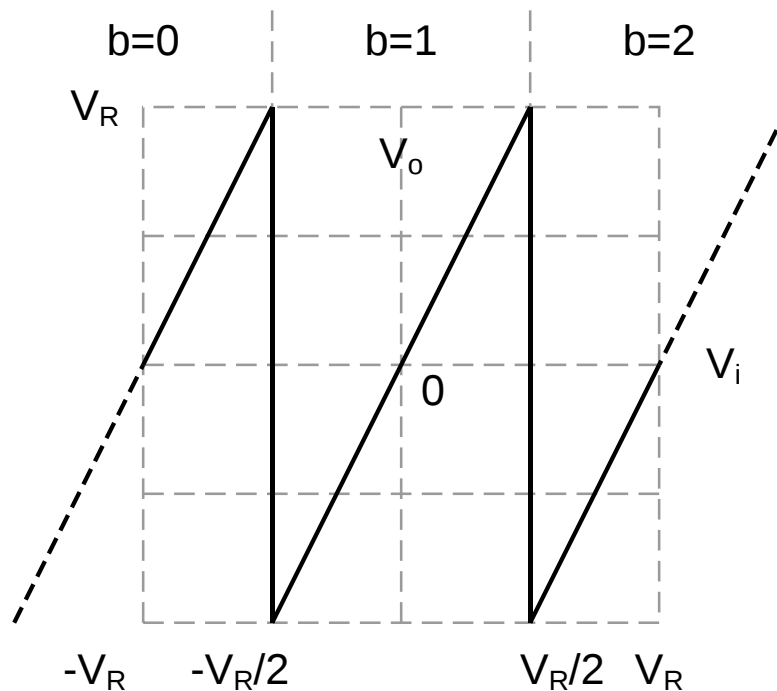
$$\begin{aligned} V_o &= V_o^+ - V_o^- \\ &= \frac{C_1 + C_2}{C_1} \cdot V_i + \frac{C_2}{C_1} \cdot (V_{CM} - V_{CM}) \\ &= 2 \cdot V_i \end{aligned}$$

$b = 2$



$$\begin{aligned} V_o &= V_o^+ - V_o^- \\ &= \frac{C_1 + C_2}{C_1} \cdot V_i - \frac{C_2}{C_1} \cdot (V_T - V_B) \\ &= 2 \cdot V_i - V_R \end{aligned}$$

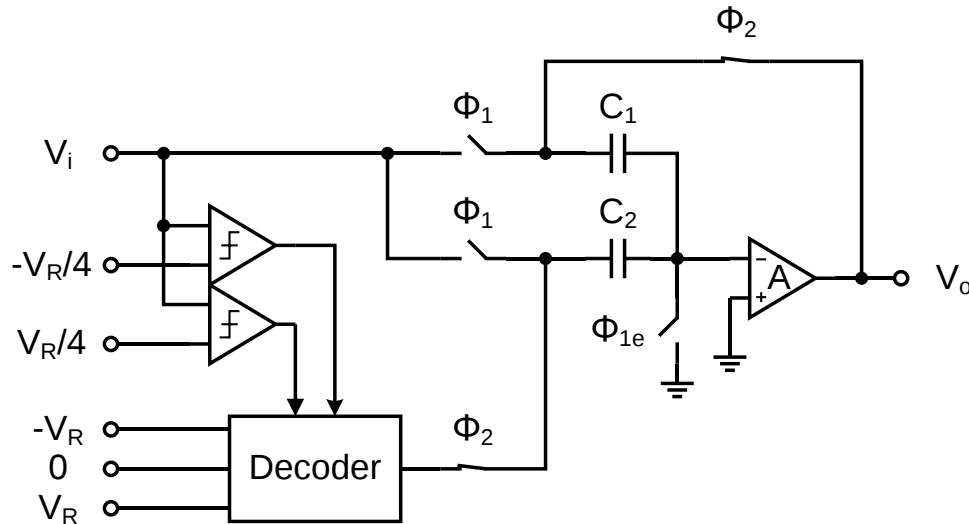
Alternative 1.5-Bit Architecture



How does
this work?

Ref: E. G. Soenen and R. L. Geiger, "An architecture and an algorithm for fully digital correction of monolithic pipelined ADC's," *IEEE Trans. on Circuits and Systems II*, vol. 42, issue 3, pp. 143-153, 1995.

Error Mechanisms of RA

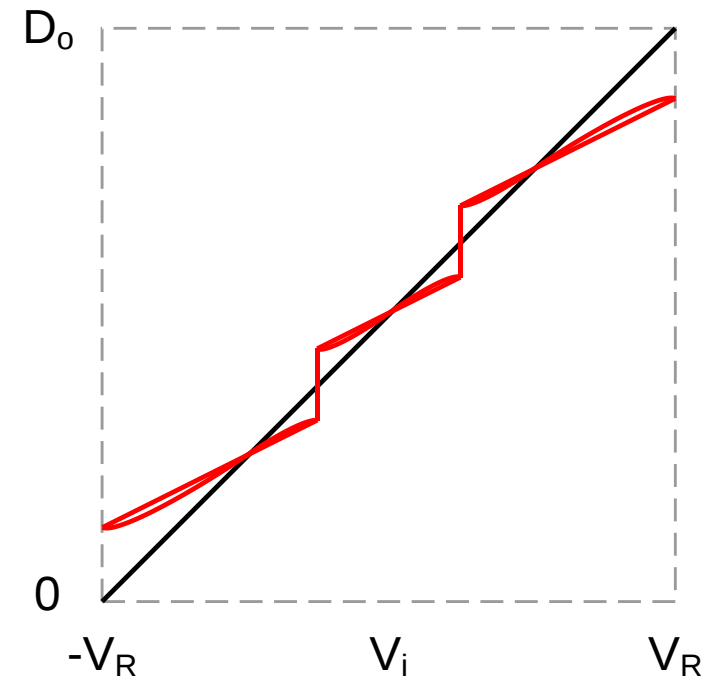
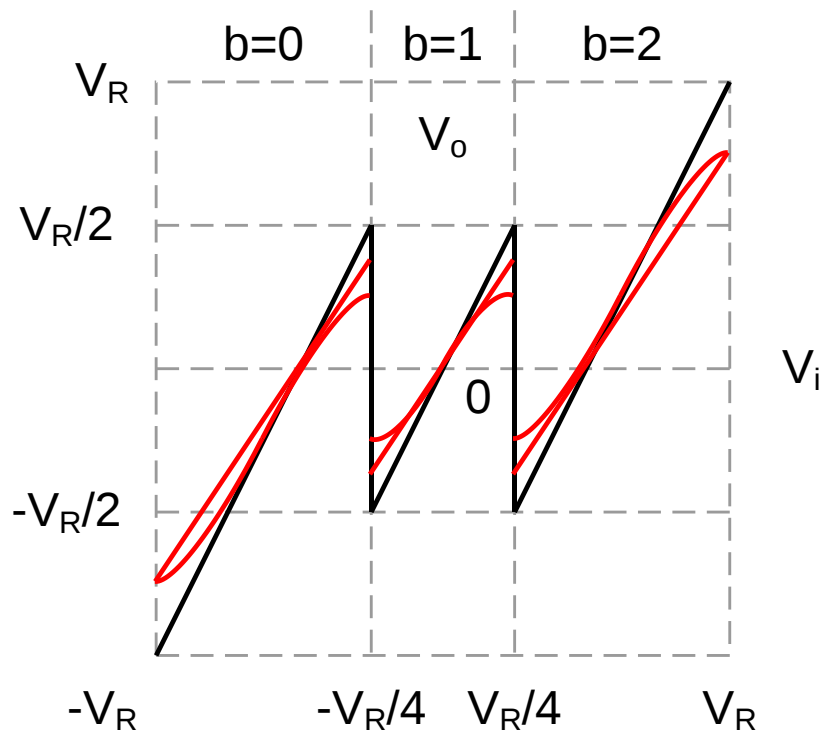


- Capacitor mismatch
- Op-amp finite-gain error and nonlinearity
- Charge injection and clock feedthrough (S/H)
- Finite circuit bandwidth

$$V_o = 2 \cdot V_i - (b-1) \cdot V_R$$

$$V_o(t = \infty) = \frac{C_1 + C_2}{C_1 + \frac{C_1 + C_2}{A(V_o)}} \cdot f_{S/H}(V_i) - (b-1) \frac{C_2}{C_1 + \frac{C_1 + C_2}{A(V_o)}} \cdot V_R$$

RA Gain Error and Nonlinearity



Raw accuracy is usually limited to 10-12 bits w/o error correction

Static Gain-Error Correction

Analog-domain method:

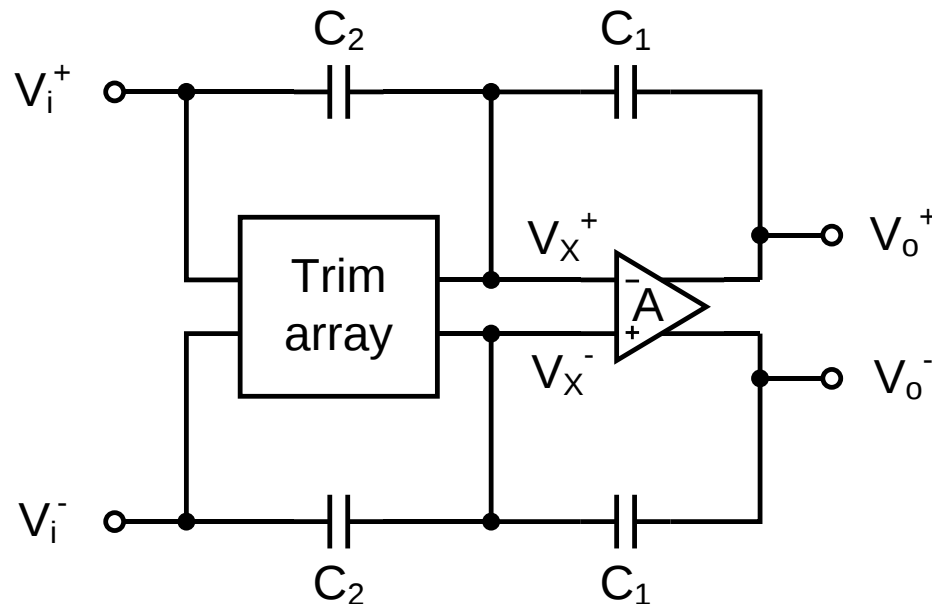
$$V_o = \frac{C_1 + C_2}{C_1 + \frac{C_1 + C_2}{A}} \cdot V_i - b \cdot \frac{C_2}{C_1 + \frac{C_1 + C_2}{A}} \cdot V_R = \boxed{ka_1 \cdot V_i - b \cdot (ka_2 \cdot V_R)}$$

Digital-domain method:

$$\left(\frac{V_i}{V_R} \right) = \frac{C_1 + \frac{C_1 + C_2}{A}}{C_1 + C_2} \cdot \left(\frac{V_o}{V_R} \right) + \frac{C_2}{C_1 + C_2} \cdot b \Rightarrow \boxed{D_i = kd_1 \cdot D_o + kd_2 \cdot b}$$

Do we need to correct for kd_2 error?

RA Gain Trimming

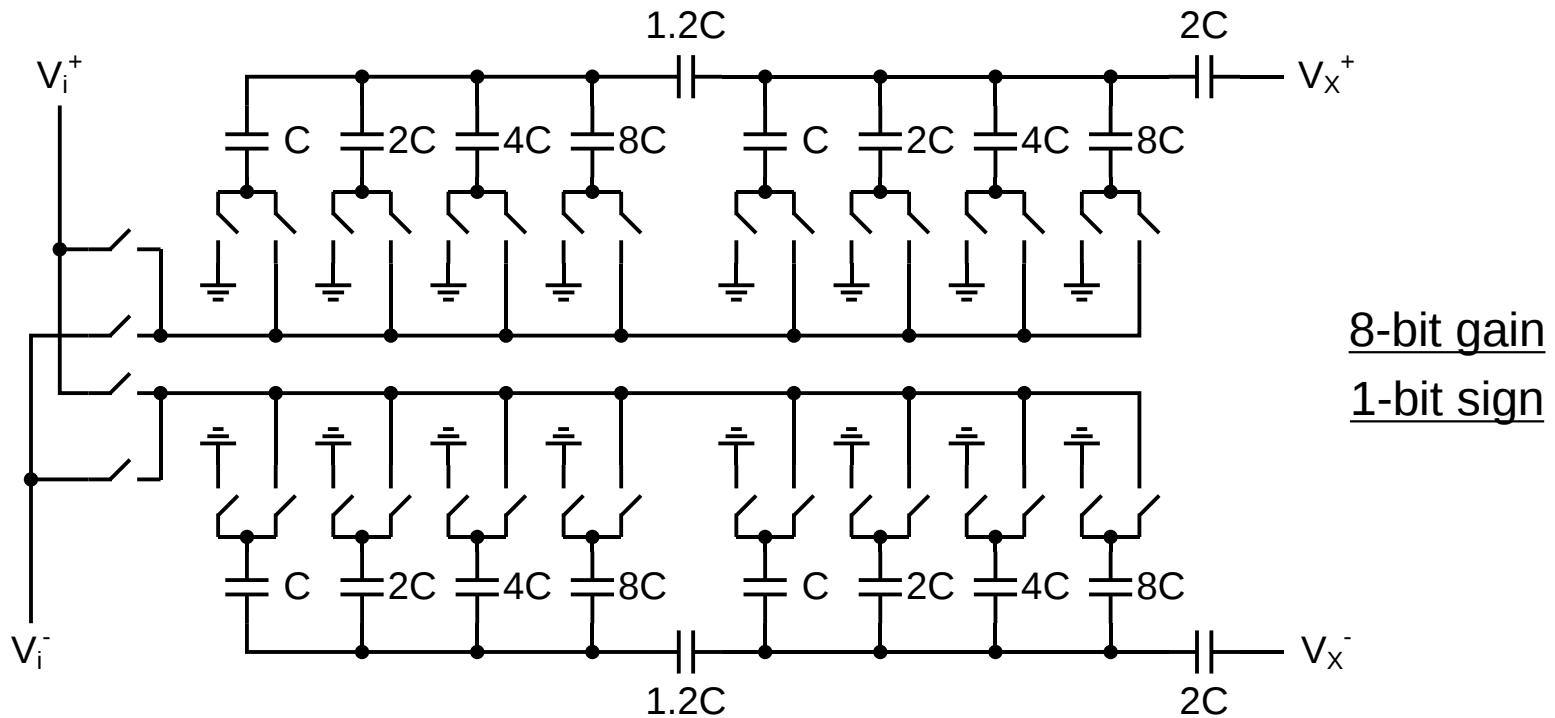


$C_1/C_2 = 1$ nominally

$$V_o = \frac{(C_1 + C_2)}{C_1 + \frac{C_1 + C_2}{A}} \cdot V_i - \frac{C_2}{C_1 + \frac{C_1 + C_2}{A}} \cdot (b - 1) V_R$$

- Precise gain-of-two is achieved by adjustment of the trim array
- Finite-gain error of op-amp is also compensated (**not nonlinearity**)

Split-Array Trimming DAC



- Successive approximation utilized to find the correct gain setting
- Coupling cap is slightly increased to ensure segmental overlap

Digital Radix Correction

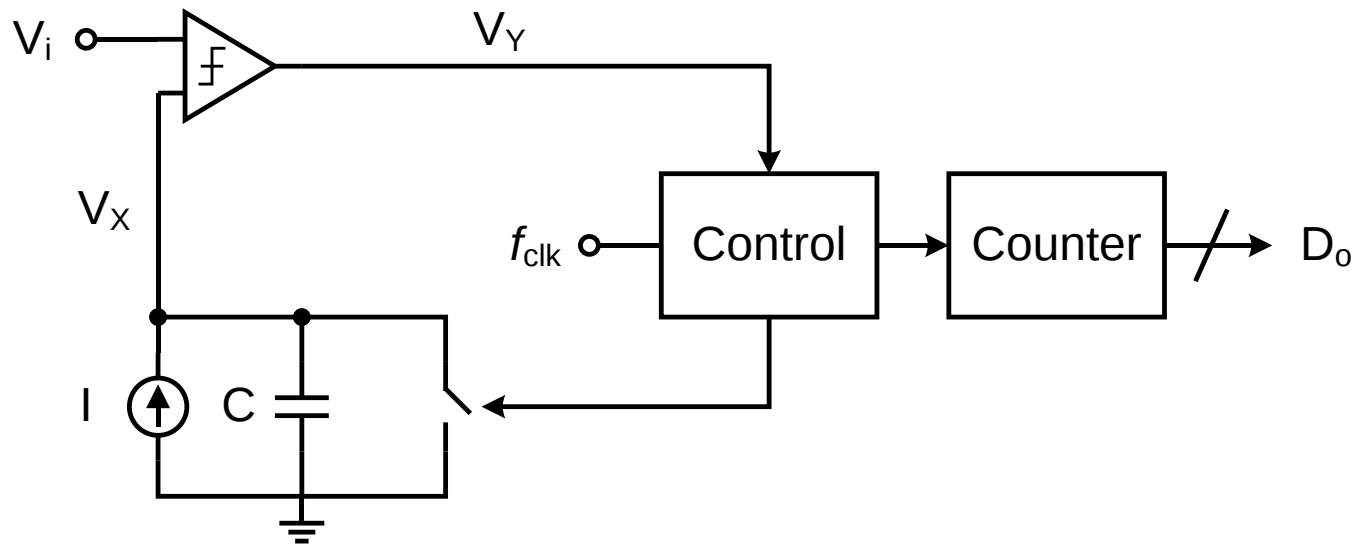
$$\left(\frac{V_i}{V_R}\right) = \frac{C_1 + \frac{C_1 + C_2}{A}}{C_1 + C_2} \cdot \left(\frac{V_0}{V_R}\right) + \frac{C_2}{C_1 + C_2} \cdot b \Rightarrow D_i = kd_1 \cdot D_0 + kd_2 \cdot b$$

Unroll this:

$$\begin{aligned} D_j &= kd_2 \cdot b_j + kd_1 \cdot D_{j+1} \\ &= kd_2 \cdot b_j + kd_1 \cdot (kd_2 \cdot b_{j+1} + kd_1 \cdot D_{j+2}) \\ &= (kd_2 \cdot b_j) + kd_1 \cdot (kd_2 \cdot b_{j+1}) + kd_1^2 \cdot D_{j+2} \\ &= (kd_2 \cdot b_j) + kd_1 \cdot (kd_2 \cdot b_{j+1}) + kd_1^2 \cdot (kd_2 \cdot b_{j+2}) + kd_1^3 \cdot D_{j+3} \\ &= (kd_2 \cdot b_j) + kd_1 \cdot (kd_2 \cdot b_{j+1}) + kd_1^2 \cdot (kd_2 \cdot b_{j+2}) + kd_1^3 \cdot (kd_2 \cdot b_{j+3}) + \dots \end{aligned}$$

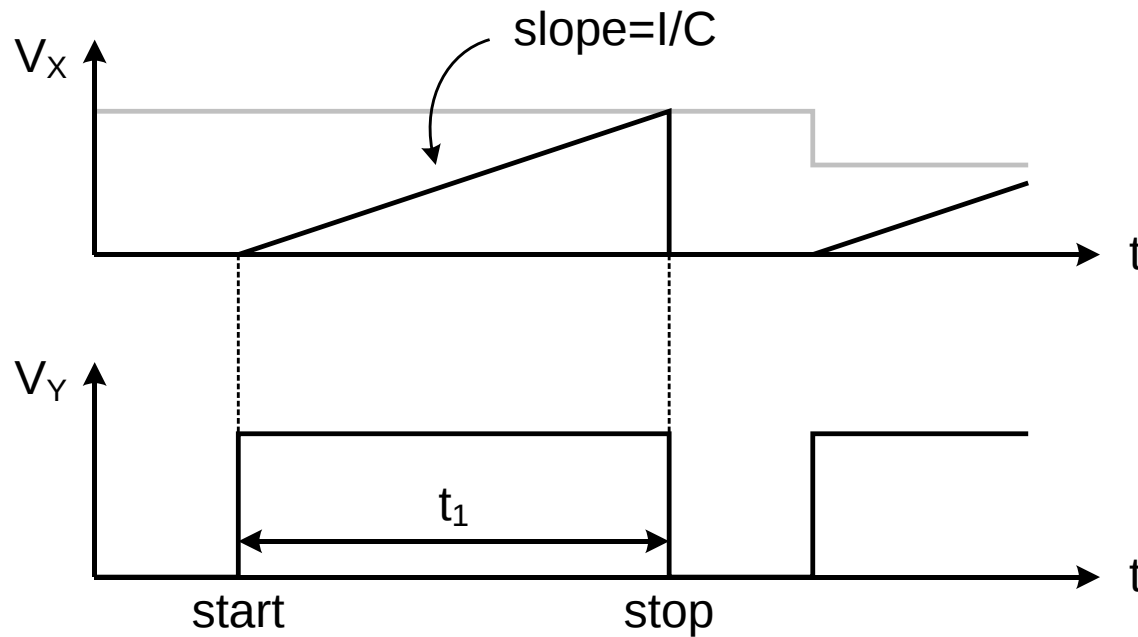
Integrating ADC

Single-Slope Integration ADC



- Sampled-and-held input (V_i)
- Counter keeps counting until comparator output toggles
- Simple, inherently monotonic, but very slow ($2^N \cdot T_{clk}$ /sample)

Single-Slope Integration ADC



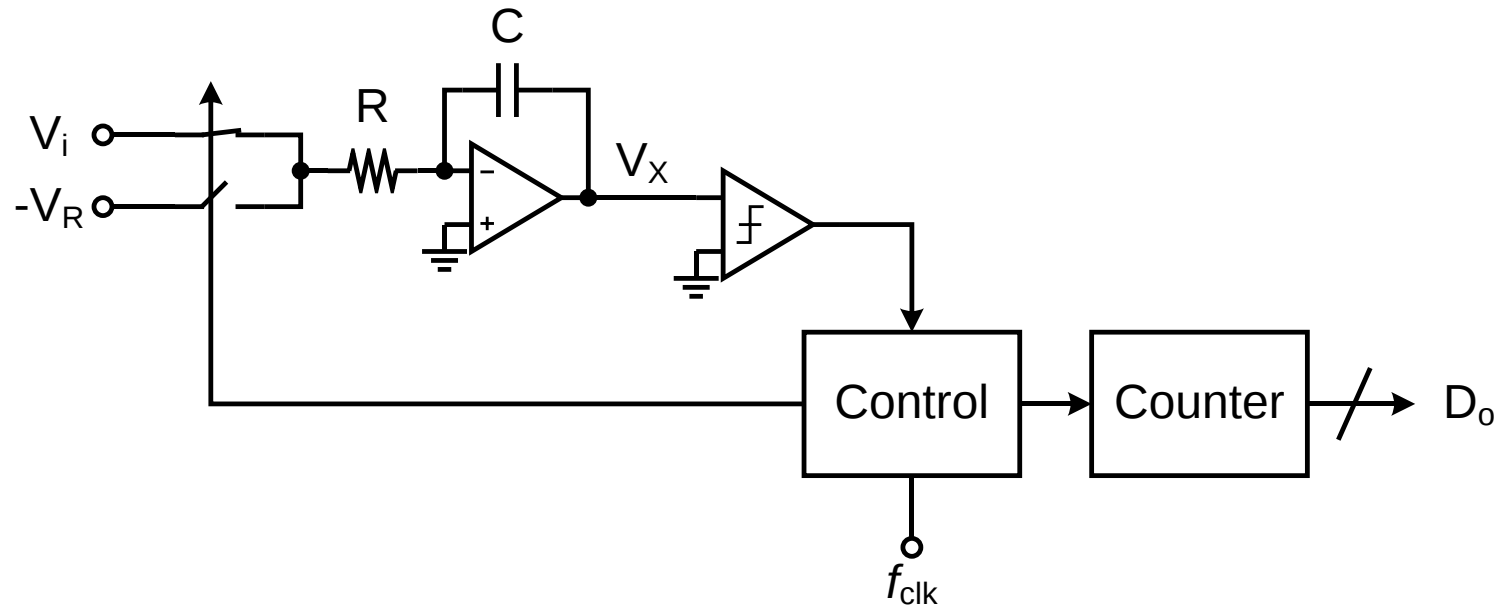
$$V_i = \frac{I}{C} \cdot t_1, \quad D_o = \left\lfloor \frac{t_1}{T_{\text{clk}}} \right\rfloor$$

$$\Rightarrow D_o = \left\lfloor \frac{V_i}{\left(\frac{I \cdot T_{\text{clk}}}{C} \right)} \right\rfloor,$$

$$\text{LSB} = \frac{I \cdot T_{\text{clk}}}{C}$$

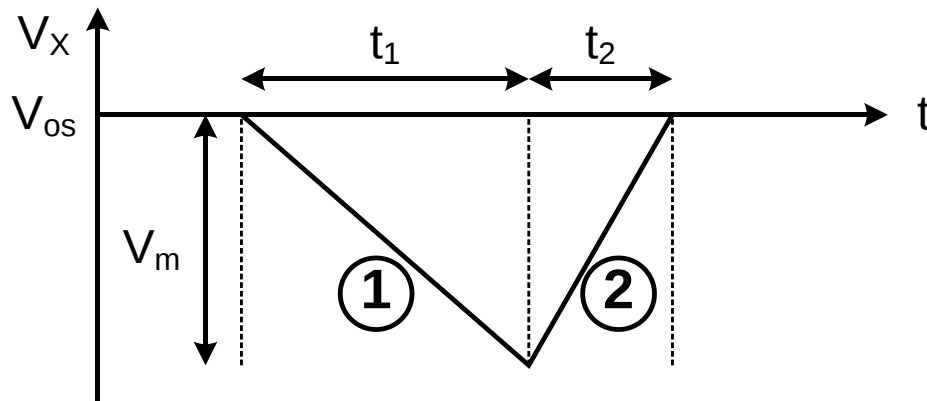
- INL depends on the linearity of the ramp signal
- Precision capacitor (C), current source (I), and clock (T_{clk}) required
- Comparator must handle wide input range of $[0, V_{\text{FS}}]$

Dual-Slope Integration ADC



- RC integrator replaces the I-C integrator
- Input and reference voltages undergo the same signal path
- Comparator only detects zero crossing

Dual-Slope Integration ADC

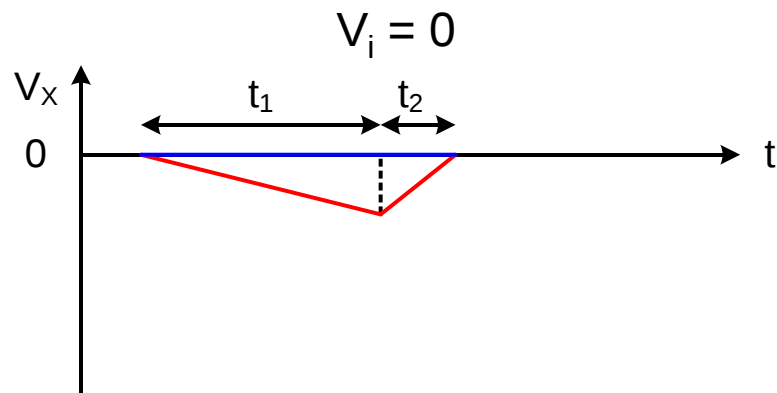


$$V_m = \frac{V_i}{RC} \cdot t_1 = \frac{V_R}{RC} \cdot t_2$$
$$\Rightarrow D_0 = \left\lfloor \frac{V_i}{V_R} \right\rfloor = \left\lfloor \frac{t_2}{t_1} \right\rfloor = \frac{N_2}{N_1}$$

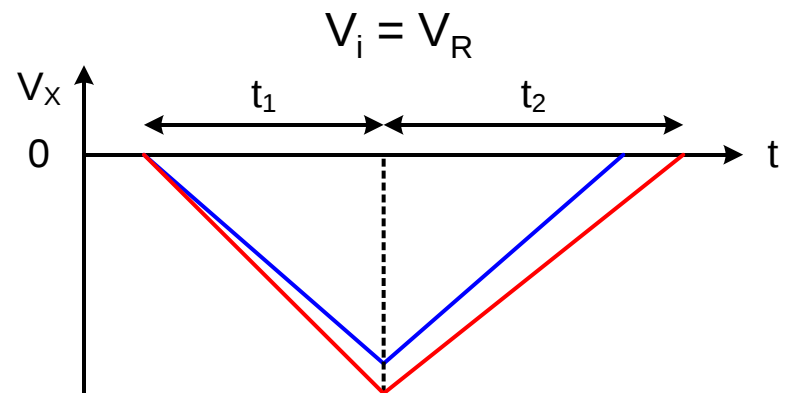
or $D_0 = N_2$ for fixed N_1

- Exact values of R , C , and T_{clk} are not required
- Comparator offset doesn't matter (what about its delay?)
- Op-amp offset introduces gain error and offset (why?)
- Op-amp nonlinearity introduces INL error

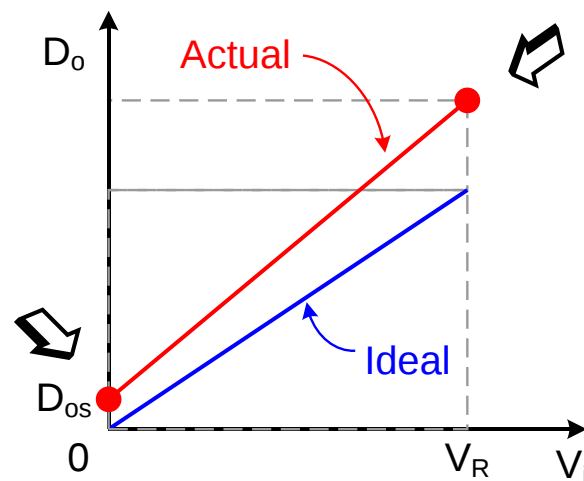
Op-Amp Offset



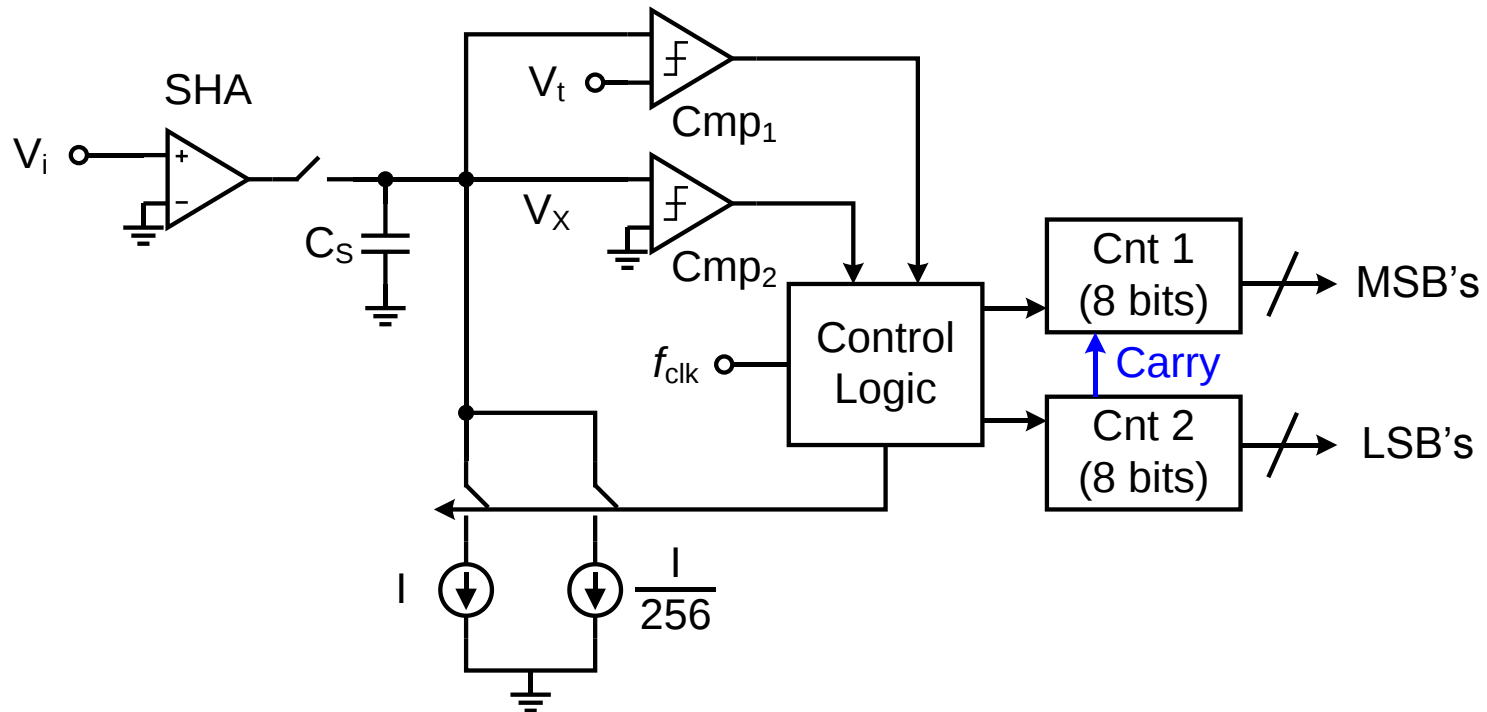
$N_2 \neq 0 \rightarrow$ Offset



Longer integration time!

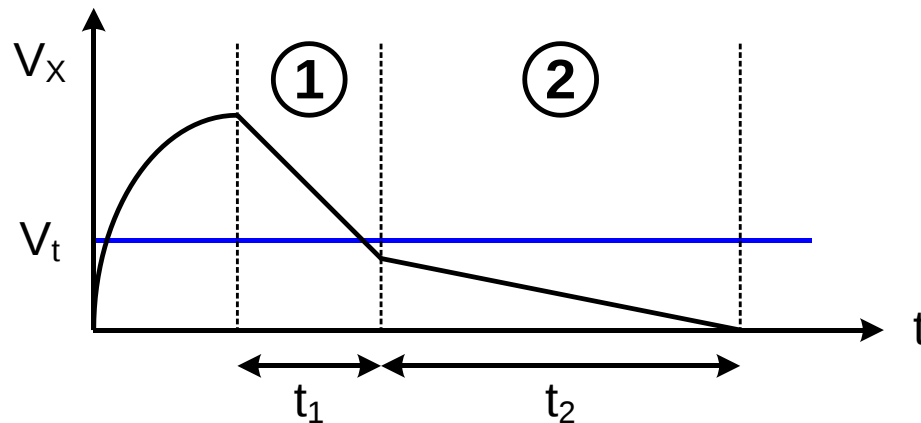


Subranging Dual-Slope ADC



- MSB discharging stops at the immediate next integer count past V_t
- Much faster conversion speed compared to dual-slope
- Two current sources (matched) and two comparators required

Subranging Dual-Slope ADC



$$\frac{dV_x(1)}{dt} = \frac{I}{C},$$
$$\frac{dV_x(2)}{dt} = \frac{I}{256C}$$

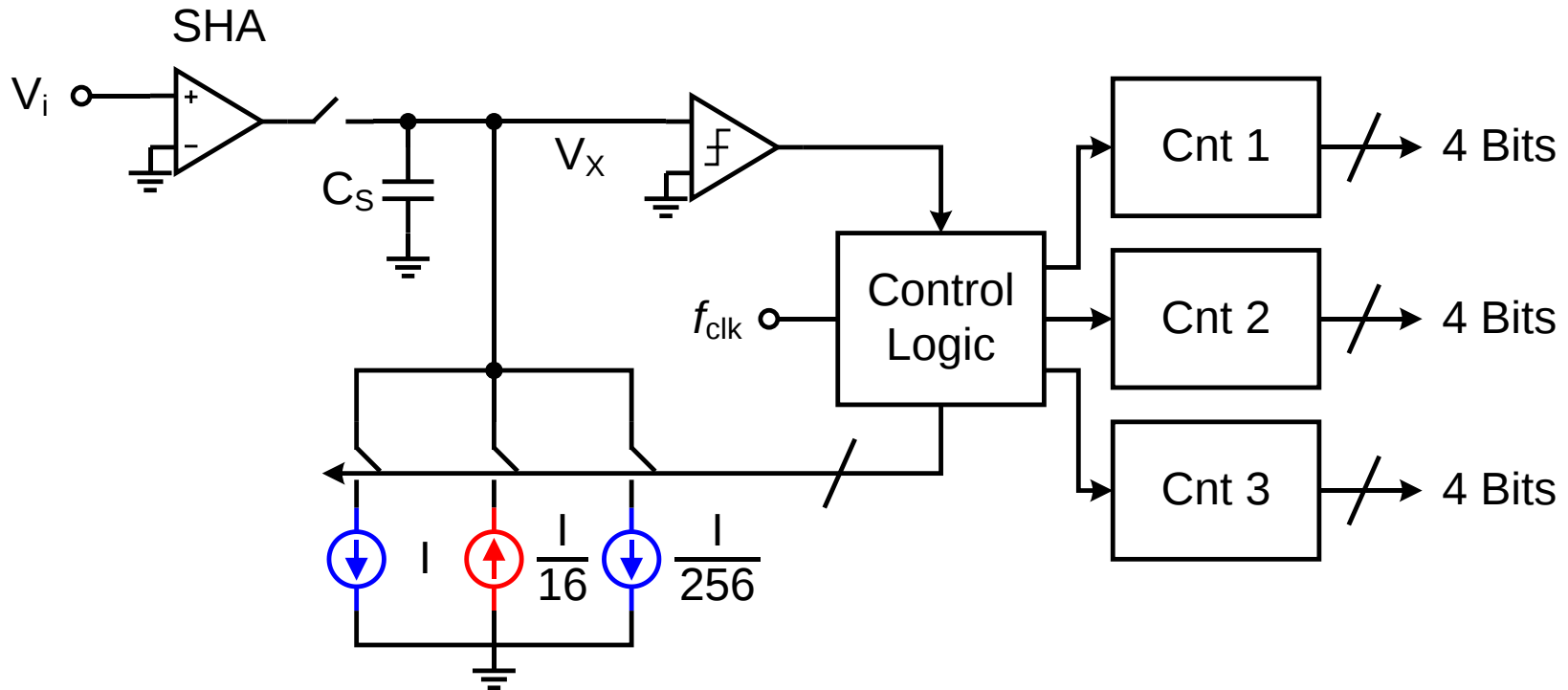
$$D_o = N_1 \cdot W + N_2$$

- Precise V_t is not required if carry is propagated
- Matching between the current sources is critical
→ if $I_1 = I$, $I_2 = (1+\delta) \cdot I/256$, then $|\delta| \leq 0.5/256$
- It'd be nice if CMP 1 can be eliminated → ZX detector!

Subranging Dual-Slope ADC

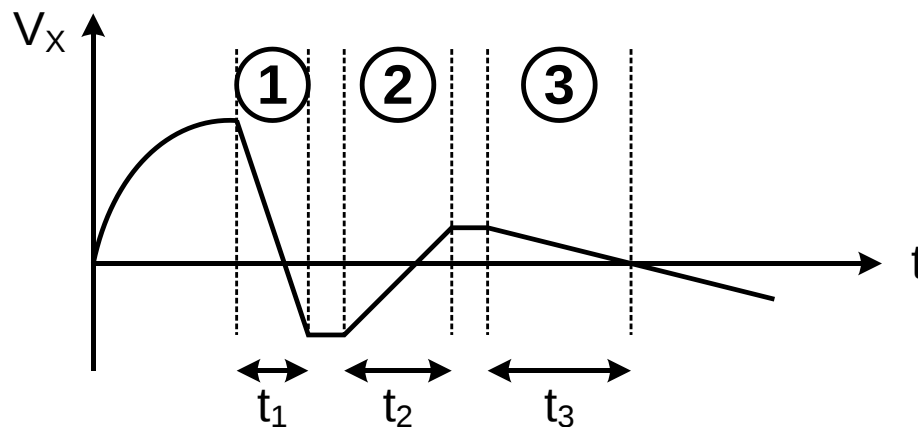
- CMP 1 response time is not critical
- Delay from CNT 1 to MSB current shut-off is not critical
→ constant delay results in an offset (why?)
- CMP 2 response time is critical, but relaxed due to subranging

Subranging Multi-Slope ADC



Ref: J.-G. Chern and A. A. Abidi, "An 11 bit, 50 kSample/s CMOS A/D converter cell using a multislope integration technique," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 1989, pp. 6.2/1-6.2/4.

Subranging Multi-Slope ADC



$$\frac{dV_x(1)}{dt} = \frac{I}{C},$$

$$\frac{dV_x(2)}{dt} = -\frac{I}{16C},$$

$$\frac{dV_x(3)}{dt} = \frac{I}{256C}$$

$$D_o = N_1 \cdot W_1 - N_2 \cdot W_2 + N_3$$

- Single comparator detects zero-crossing
- Comparator response time greatly relaxed
- Matching between the current sources still critical

Subranging Multi-Slope ADC

- Comparator response time is not critical except the last one
- Delays from CNTs to current sources shut-off are not critical
→ constant delays only result in offsets
- Last comparator response time is critical, but relaxed due to multi-step subranging

References

1. Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters," 2nd Ed., Springer, 2005..
2. Y. Chiu, *Data Converters Lecture Slides*, UT Dallas 2012.
3. B. Boser, *Analog-Digital Interface Circuits Lecture Slides*, UC Berkeley 2011.