CMOS Comparator Design

Extra Slides

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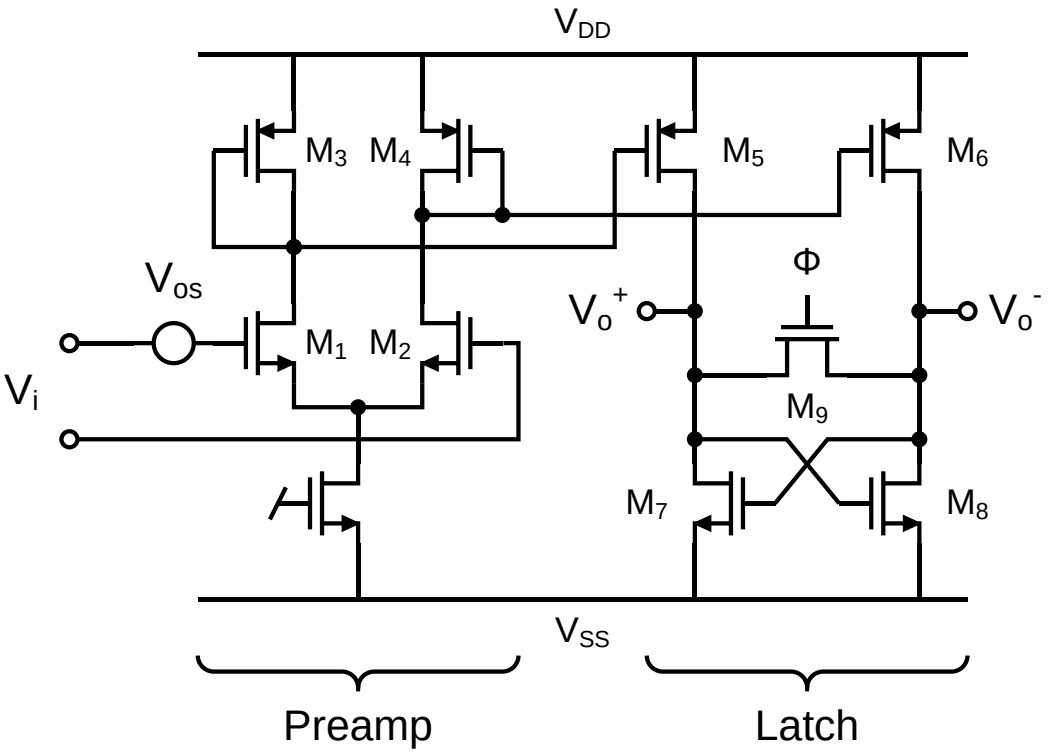
Comparator Design Considerations

- Comparator =
  - Preamp (optional)
  - + Reference Subtraction (optional for single-bit case)
  - + Regenerative Latch
  - +Static Latch to hold outputs (optional)
- Design Considerations
  - Accuracy (dynamic and static offset, noise, resolution)
  - Settling time (tracking BW, regeneration speed)
  - Sensitivity/resolution (gain)
  - Metastability (ability to make correct decisions)
  - Overdrive recovery (memory)
  - Power consumption

An Example CMOS Comparator



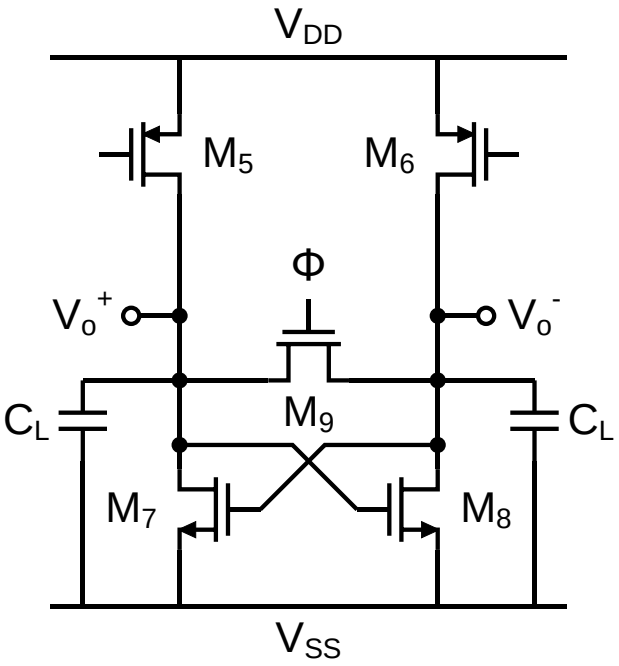
V_{os} orginiates from:

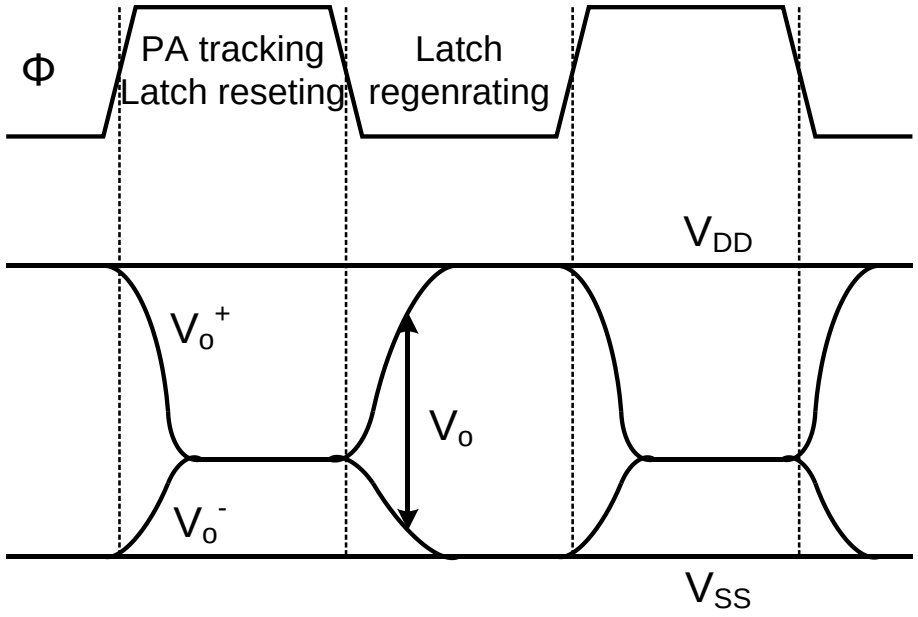
- Preamp input pair mismatch (V_{th},W/L)
- PMOS loads and current mirror
- Latch offset
- Charge-Injection

clock-feedthru imbalance of the reset switch (M9)

- Clock routing
- Parasitics

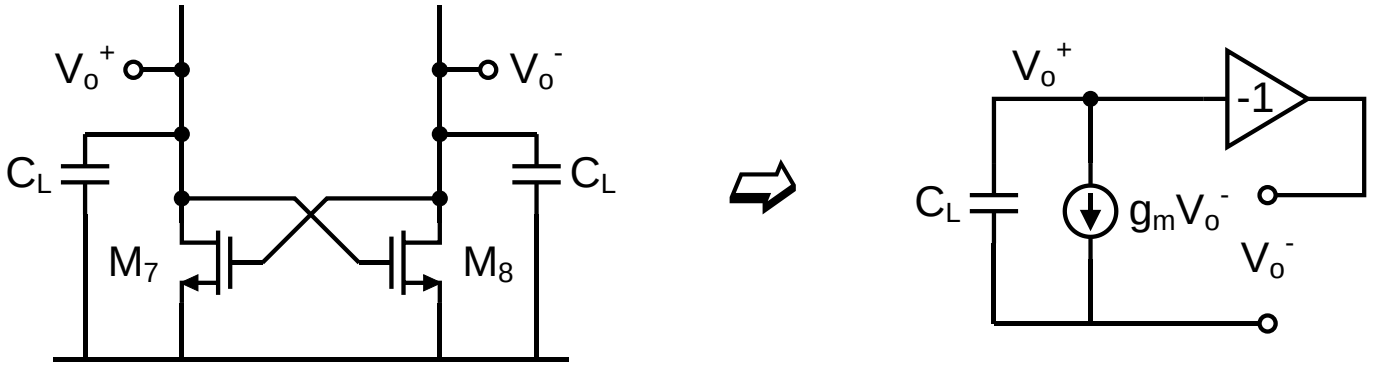
Latch Regeneration





- Exponential regeneration due to positive feedback of M_7 and M_8

Regeneration Speed – Linear Model

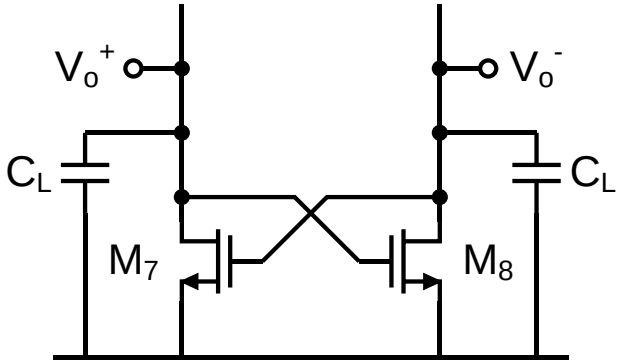


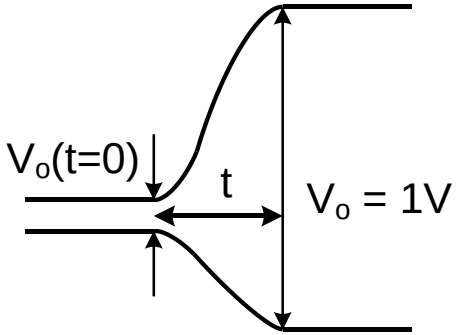
$$\begin{cases} V_o^+ = -V_o^- \\ V_o^+ = -g_m \cdot V_o^-/sC_L \end{cases} \Rightarrow \begin{pmatrix} 1 & 1 \\ 1 & g_m/sC_L \end{pmatrix} \begin{pmatrix} V_o^+ \\ V_o^- \end{pmatrix} = 0$$

$$\Delta(s) = g_m/sC_L - 1 = 0 \quad \Rightarrow \quad s_p = g_m/C_L, \quad \text{single RHP pole}$$

$$V_o(t>0) = V_o(t=0) \cdot \exp(t \cdot g_m/C_L)$$

Reg. Speed – Linear Model

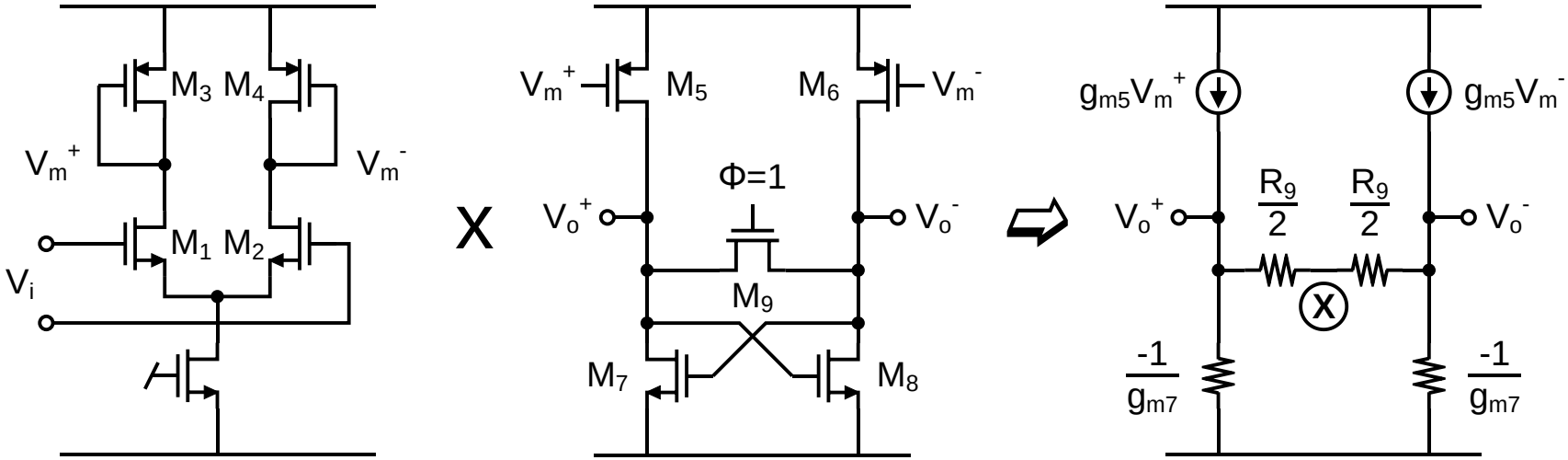




V_o	$V_o(t=0)$	$t/(C_L/g_m)$
1V	100mV	2.3
1V	10mV	4.6
1V	1mV	6.9
1V	100μV	9.2

$$t = \frac{C_L}{g_m} \cdot \ln\left[\frac{V_o(t)}{V_o(t=0)}\right]$$

Reg. Speed – Linear Model



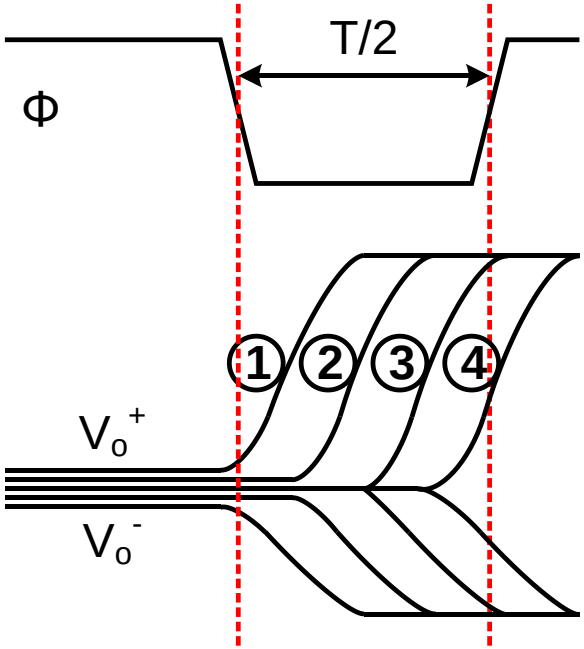
$$|A_{V1}| = \frac{g_{m1}}{g_{m3}}$$

$$|A_{V2}| = \frac{g_{m5}R_9}{2 - g_{m7}R_9}, \quad \frac{R_9}{2} < \frac{1}{g_{m7}} \text{ to be amplifier.}$$

$$V_o(0) = V_i(0) \cdot A_V = V_i(0) \cdot A_{V1}A_{V2}$$

$$V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

Comparator Metastability

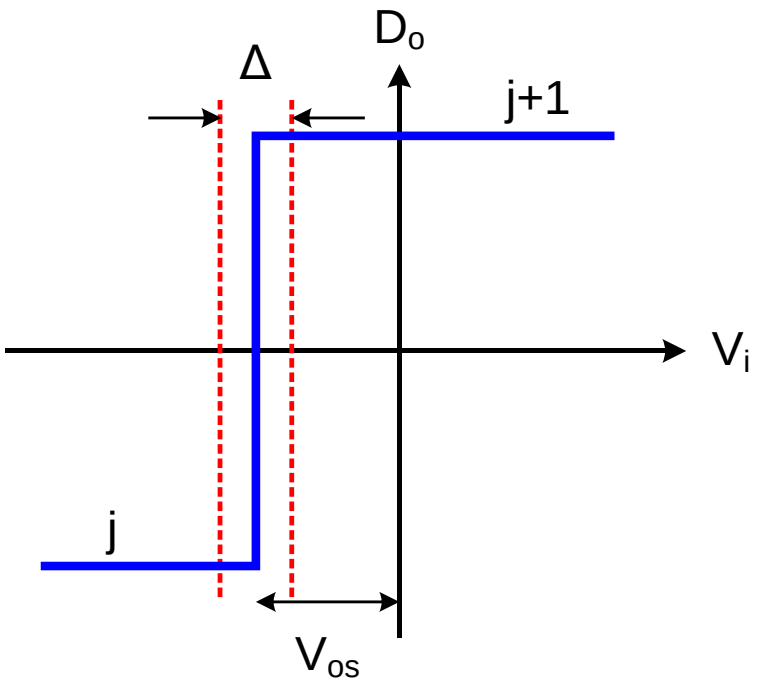


$$V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

Curve	$A_{V1}A_{V2}$	$V_i(t=0)$
①	10	10 mV
②	10	1 mV
③	10	100 μV
④	10	10 μV

Comparator fails to produce valid logic outputs within T/2 when input falls into a region that is sufficiently close to the comparator threshold

Comparator Metastability



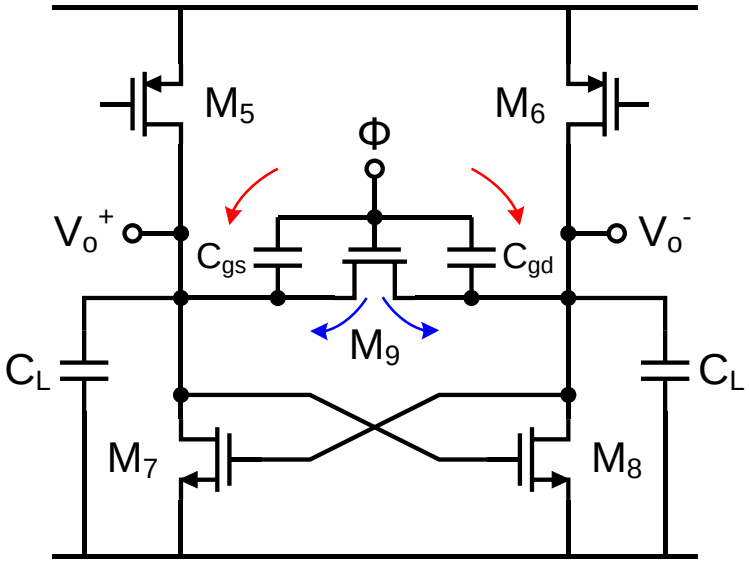
Assuming that the input is uniformly distributed over V_{FS}, then

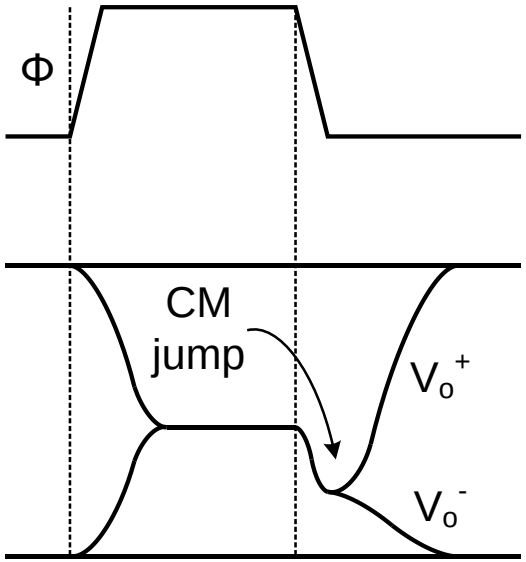
$$BER = \frac{\Delta}{1LSB}$$

$$V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

- Cascade preamp stages (typical flash comparator has 2-3 pre-amp stages)
- Use pipelined multi-stage latches; pre-amp can be pipelined too

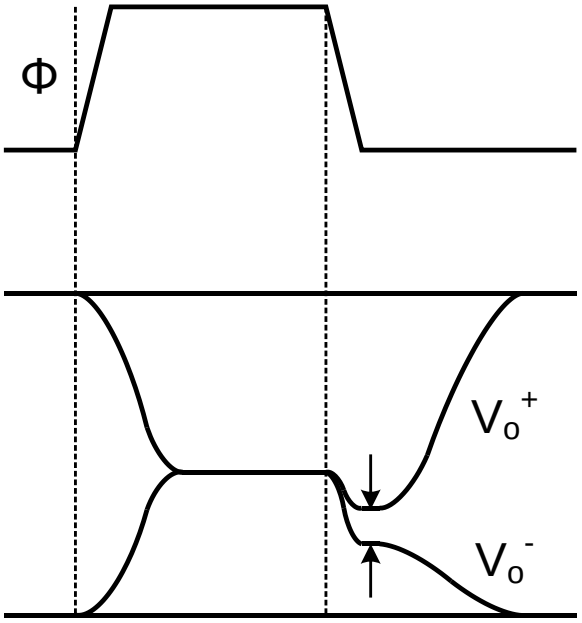
Charge-Injection and Clock-Feedthrough in Latch





- Charge injection (CI) and clock-feedthrough (CF) introduce CM jump in V_o^+ and V_o^-
- Dynamic latches are more susceptible to CI and CF errors

Dynamic Offset of a Latch



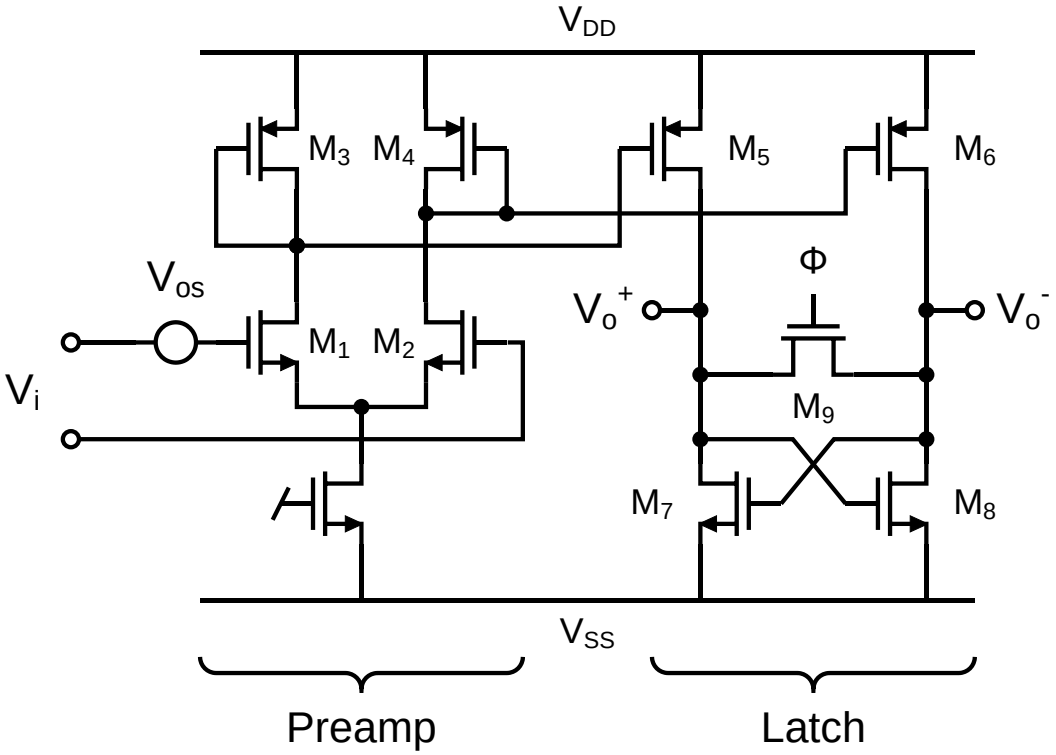
Dynamic offset derives from:

- Imbalanced CI and CF
- Imbalanced load capacitance
- Mismatch b/t M_7 and M_8
- Mismatch b/t M_5 and M_6
- Clock routing

$$\left.\begin{array}{l}0.5\text{V CM jump}\\ 10\%\text{imbalance}\end{array}\right\} \Rightarrow 50\text{mV offset}$$

Dynamic offset is usually the dominant offset error in latches

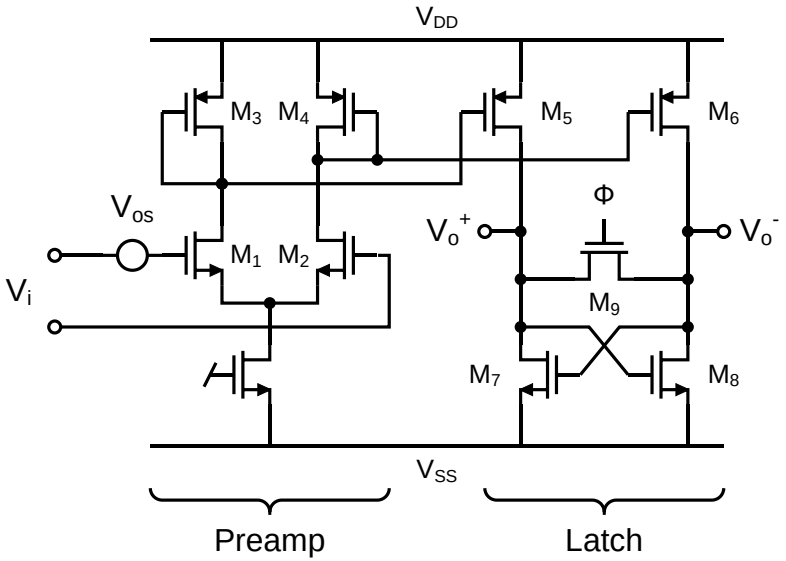
Typical CMOS Comparator



- Input-referred latch offset gets divided by the gain of PA
- Preamp introduces its own offset (mostly static due to V_{th}, W, and L mismatches)
- PA also reduces kickback noise

Kickback noise disturbs reference voltages, must settle before next sample

Comparator Offset



Differential pair mismatch:

$$V_{os}^2 = (\Delta V_{th})^2 + \frac{1}{4} V_{ov}^2 \left(\frac{\Delta \frac{W}{L}}{\frac{W}{L}} \right)^2$$

$$|A_{V1}| = \frac{g_{m1}}{g_{m3}} \qquad |A_{V2}| = \frac{g_{m5} R_9}{2 - g_{m7} R_9}$$

Total input-referred comparator offset:

$$V_{os}^2 = V_{os,12}^2 + \frac{V_{os,34}^2 + V_{os,56}^2}{A_{V1}^2} + \frac{V_{os,78}^2}{A_{V1}^2 A_{V2}^2} + \frac{V_{os,dyn}^2}{A_{V1}^2 A_{V2}^2}$$

Recall: Matching Properties

Suppose parameter P of two rectangular devices has a mismatch error of ΔP. The variance of parameter ΔP b/t the two devices is

$$\sigma^2(\Delta P) = \frac{A_P^{\,2}}{WL} + S_P^{\,2} D^2,$$

1st term dominates for small devices

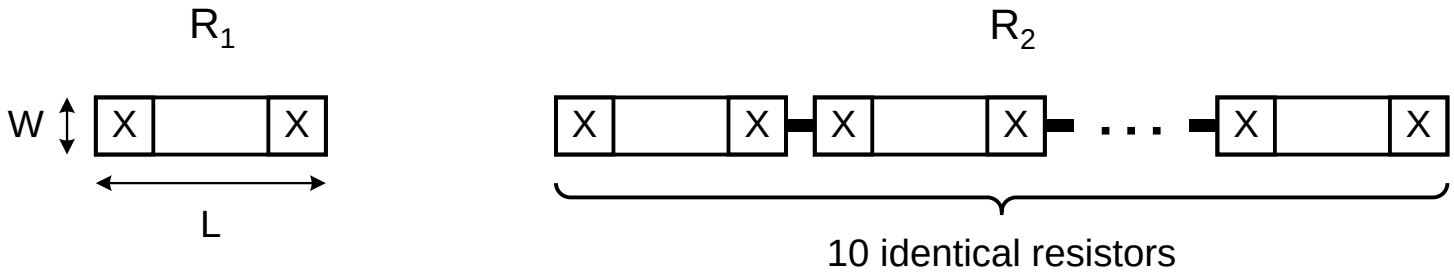
where, W and L are the effective width and length, D is the distance

$$\text{Threshold}: \ \sigma^2(V_{th}) = \frac{A_{Vth}^{\,2}}{WL} + S_{Vth}^{\,2} D^2$$

$$\text{Current factor}: \ \frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^{\,2}}{WL} + S_\beta^{\,2} D^2$$

Ref: M. J. M. Pelgrom, et al., "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 1433-1439, issue 5, 1989.

Recall: Device Sizing for Mismatch



$$R_1 = R_S \cdot \frac{L}{W} \quad \text{with std } \sigma_{R1}$$

$$R_2 = R_S \cdot 10\left(\frac{L}{W}\right) = 10R_1 \quad \text{with std } \sigma_{R2},$$

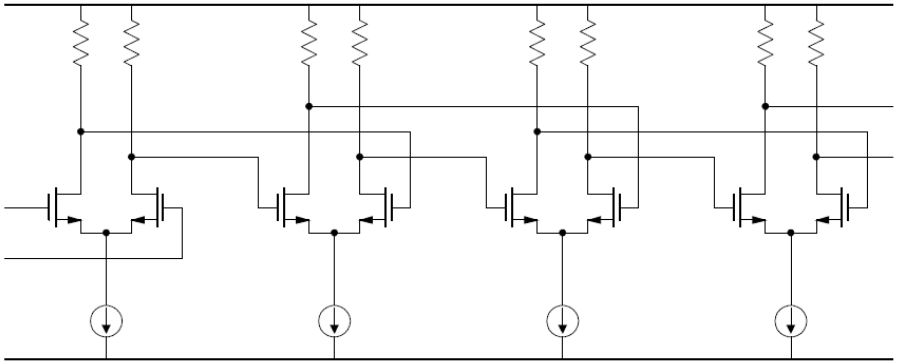
$$\sigma_{R2}^{\,2} = \sum_{j=1}^{10} \sigma_{R_j}^{\,2} = 10\sigma_{R1}^{\,2} \Rightarrow \sigma_{R2} = \sqrt{10}\sigma_{R1}$$

$$\frac{\sigma_{R2}}{R_2} = \frac{\sqrt{10}\sigma_{R1}}{10R_1} = \frac{1}{\sqrt{10}}\left(\frac{\sigma_{R1}}{R_1}\right) \Rightarrow \frac{\sigma_R}{R} \propto \frac{1}{\sqrt{A}} = \frac{1}{\sqrt{WL}}$$

"Spatial averaging"

Pre-amp Design

- A fully-differential gain-stage
  - Avoid or use simple CMFB
  - Pre-amp gain reduces input referred offset due to the latch
  - Autozeroing techniques for offset storage and reduction
- Pre-amp open-loop gain vs tracking bandwidth trade-off
  - Multiple stages of pre-amp limit bandwidth
    - Optimum value of stages 2-4

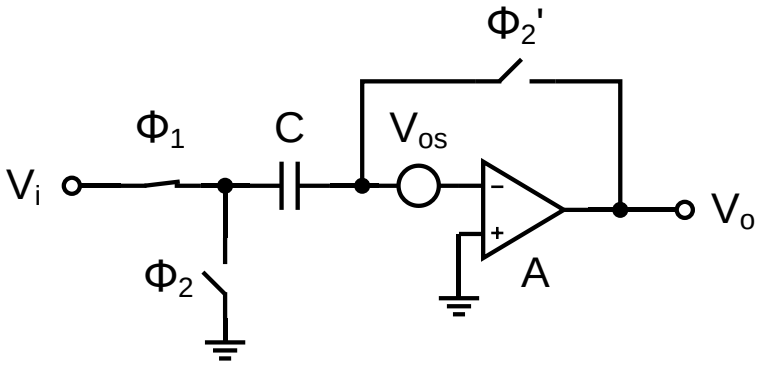


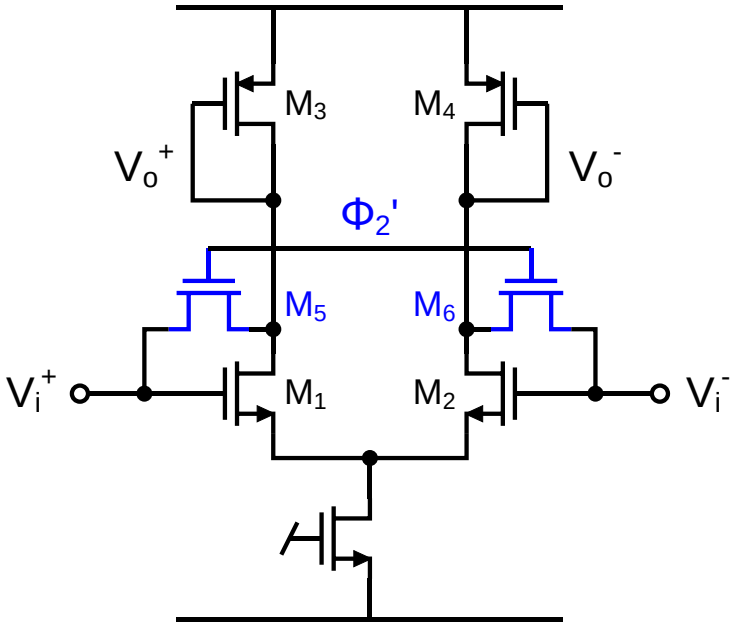
N stages:

$$\left|A_N(\omega)\right| = \left|\left(\frac{A_0}{1+j\cdot\omega/\omega_0}\right)^N\right| = \left(\frac{A_0}{\sqrt{1+(\omega/\omega_0)^2}}\right)^N$$

$$\left|A_N(\omega=\omega_{-3dB})\right| = \frac{A_0{}^N}{\sqrt{2}}, \quad \omega_{-3dB} = \omega_0\sqrt{2^{\frac{1}{N}}-1}$$

Pre-amp (PA) Autozeroing





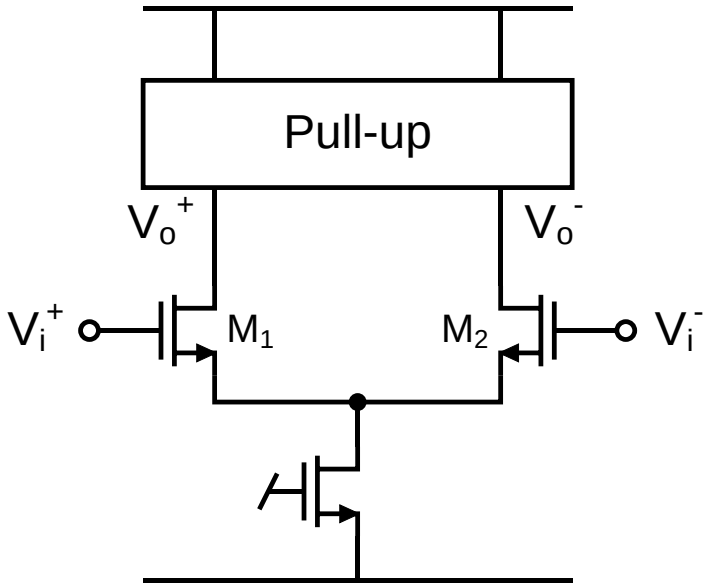
- Finite preamp gain :

$$V_{OS,in} \approx \frac{V_{OS,pre-amp}}{A}$$

- For the overall comparator :

$$\sigma^2_{V_{OS,in}} \approx \frac{\sigma^2_{V_{OS,pre}}}{A^2_{pre}} + \frac{\sigma^2_{V_{OS,latch}}}{A^2_{pre}}$$

Pre-amp Design: Pull-up load



- NMOS diode pull-up:

$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{(W/L)_1}{(W/L)_L}}$$

- PMOS diode pull-up:

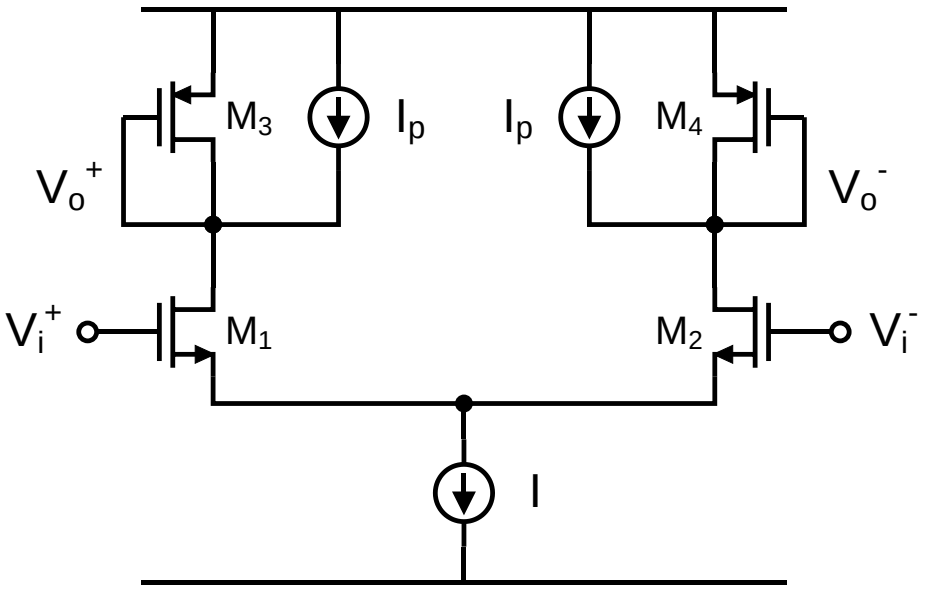
$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{\mu_n}{\mu_p}\frac{(W/L)_1}{(W/L)_L}}$$

- Resistor pull-up:

$$A_V = -g_{m1} \cdot R_L$$

- NMOS pull-up suffers from body effect, affecting gain accuracy
- PMOS pull-up is free from body effect, but subject to P/N mismatch
- Gain accuracy is the worst for resistive pull-up as resistors (poly, diffusion, well, etc.) don't track transistors; but it is fast!

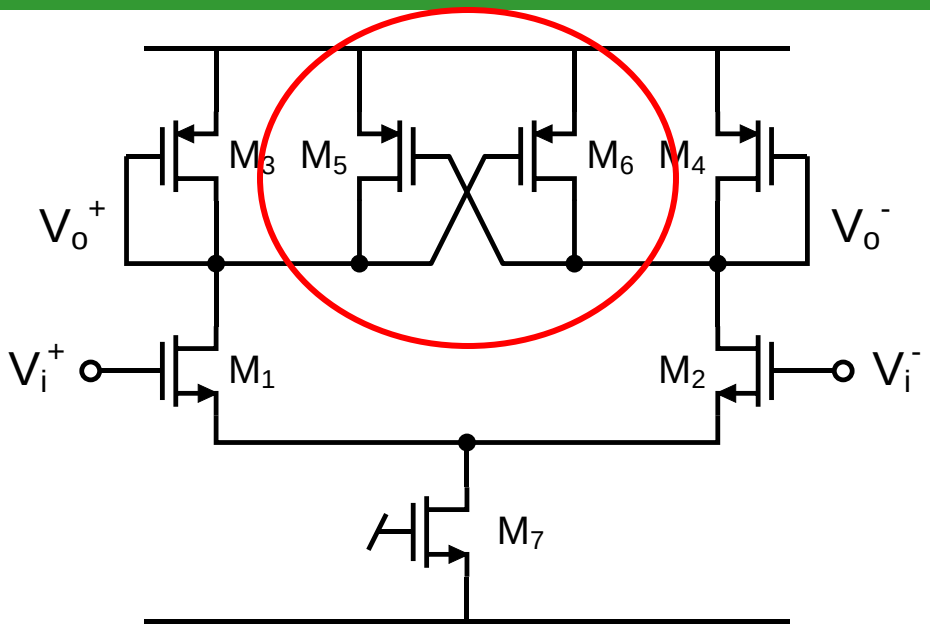
Pre-amp Design: More Gain

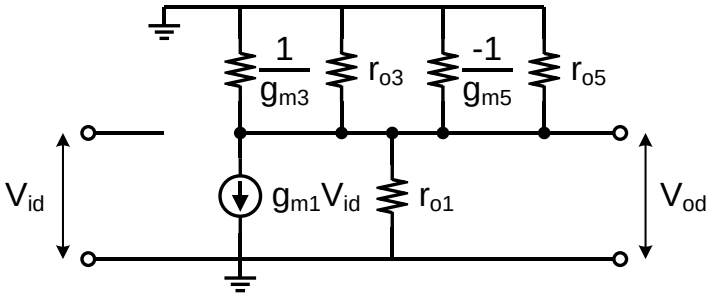


$$A_V = -\frac{g_{m1}}{g_{m3}} \approx -\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{I/2}{I/2 - I_p}\right)\frac{(W/L)_1}{(W/L)_3}}$$

- I_p diverts current away from PMOS diodes (M_3 & M_4), reducing $(W/L)_3$
- Higher gain without CMFB
- Needs biasing for I_p
- M_3 & M_4 may cut off for large V_{in}, resulting in a slow recovery

Faster Settling Pre-amp

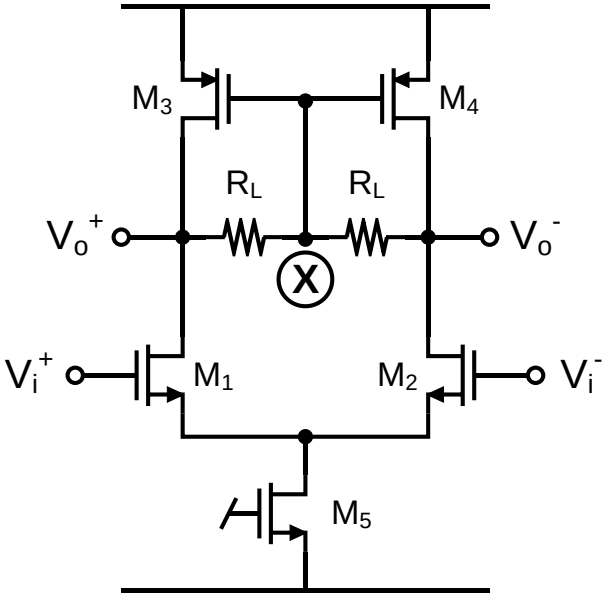




$$\text{DM gain: } A_V^{dm} = -g_{m1}\cdot\left[\frac{1}{g_{m3}} // \left(-\frac{1}{g_{m5}}\right) // r_{o1} // r_{o3} // r_{o5}\right] \approx -\frac{g_{m1}r_{o1}}{3}$$

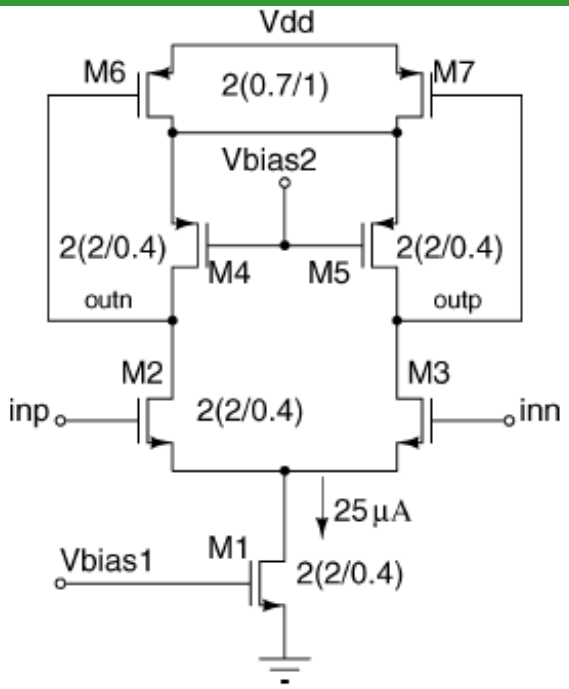
- NMOS diff-pair loaded with PMOS diodes and a PMOS cross-coupled latch
- High DM gain, low CM gain, good CMRR
- Simple, no CMFB required
- $(W/L)_{34} > (W/L)_{56}$ needs to be ensured for stability
- Ref: K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," *JSSC*, vol. 32, pp. 1887-1895, issue 12, 1997.

Pre-amp Example



- NMOS diff. pair loaded with PMOS diodes and resistors
- High DM gain, low CM gain, good CMRR
- Simple, no CMFB required
- Gain not well-defined
- Ref: B.-S. Song et al., “A 1 V 6 b 50 MHz current-interpolating CMOS ADC,” in *Symp. VLSI Circuits*, 1999, pp. 79-80.

Pre-amp Example

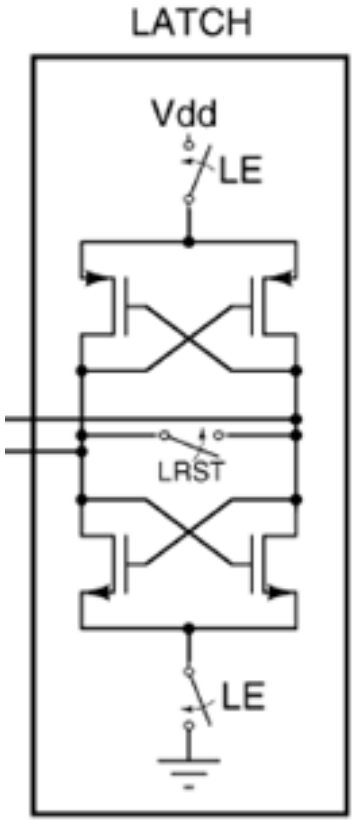


- NMOS diff. pair loaded with PMOS Current mirror
  - Simple CMFB circuit
- Gain is well-defined

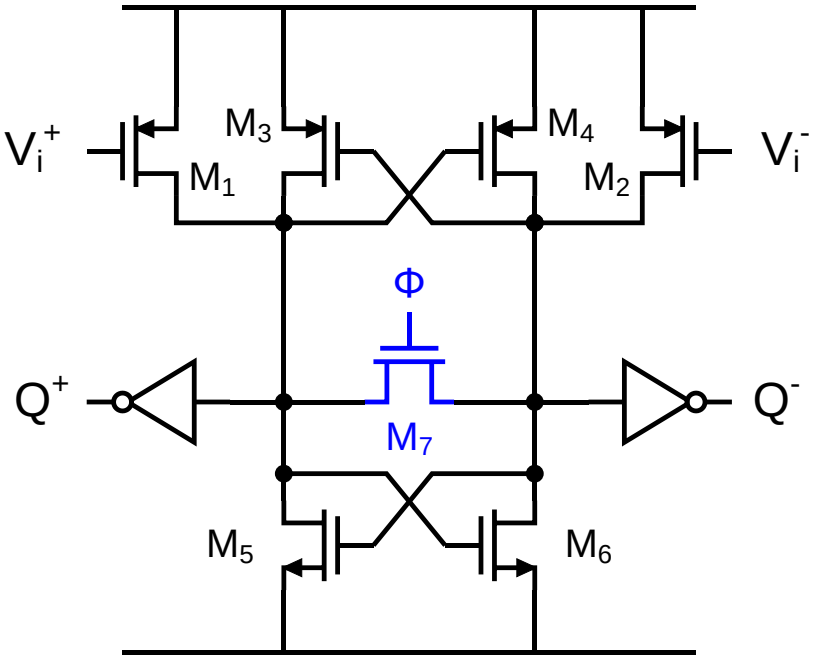
Ref: V. Srinivas, S. Pavan, A. Lachhwani, and N. Sasidhar, “A Distortion Compensating Flash Analog-to-Digital Conversion Technique," IEEE JSSC, vol. 41, no. 9, pp. 1959-1969, Sep. 2006.

Latch Design

- Regenerative latches for faster settling
  - See lecture notes
- At least one cross-coupled regenerative core
  - Local positive feedback
  - Numerous methods for applying the input initial signal to regenerate upon
  - Latches can have large static and dynamic offsets
- Large Regenerative gain for resolving small inputs
  - Metastability (wrong or incomplete decisions) when latch can't make decision
  - Pre-amp can be used for amplifying the inputs (slower tracking BW)
- One size doesn't fit all applications
  - Speed vs power consumption trade-off

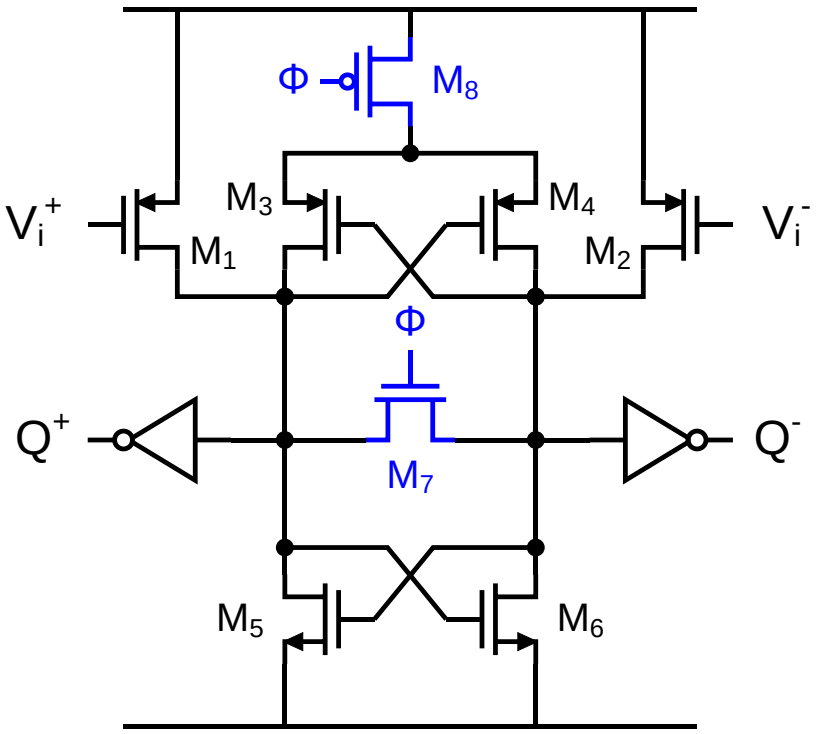


Static Latch



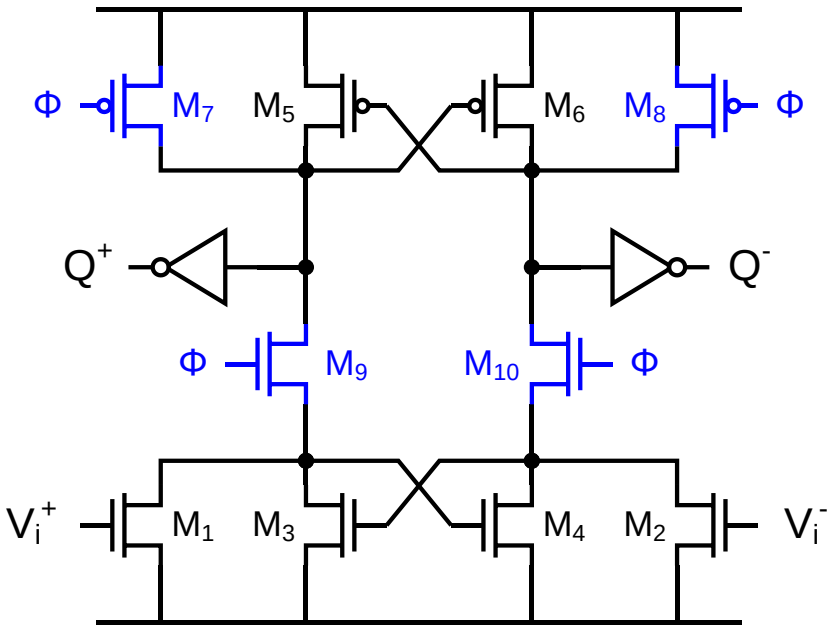
- Active pull-up and pull-down → full CMOS logic levels
- Very fast!
- Q^+ and Q^- are not well defined in reset mode ($\Phi = 1$)
- Large short-circuit current in reset mode
- Zero DC current after full regeneration
- Supply is very noisy

Semi-Dynamic Latch



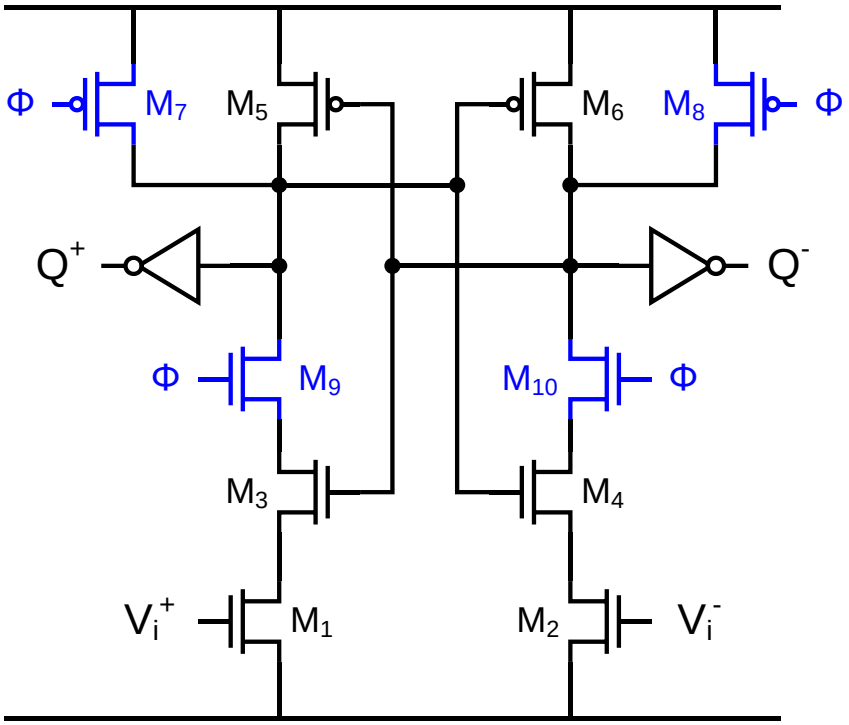
- Diode divider disabled in reset mode → less short-circuit current
- Pull-up not as fast
- Q^+ and Q^- are still not well defined in reset mode ($\Phi = 1$)
- Zero DC current after full regeneration
- Supply still very noisy

Dynamic Latch



- Zero DC current in reset mode
- Q^+ and Q^- are both reset to “0”
- Full logic level after regeneration
- Slow

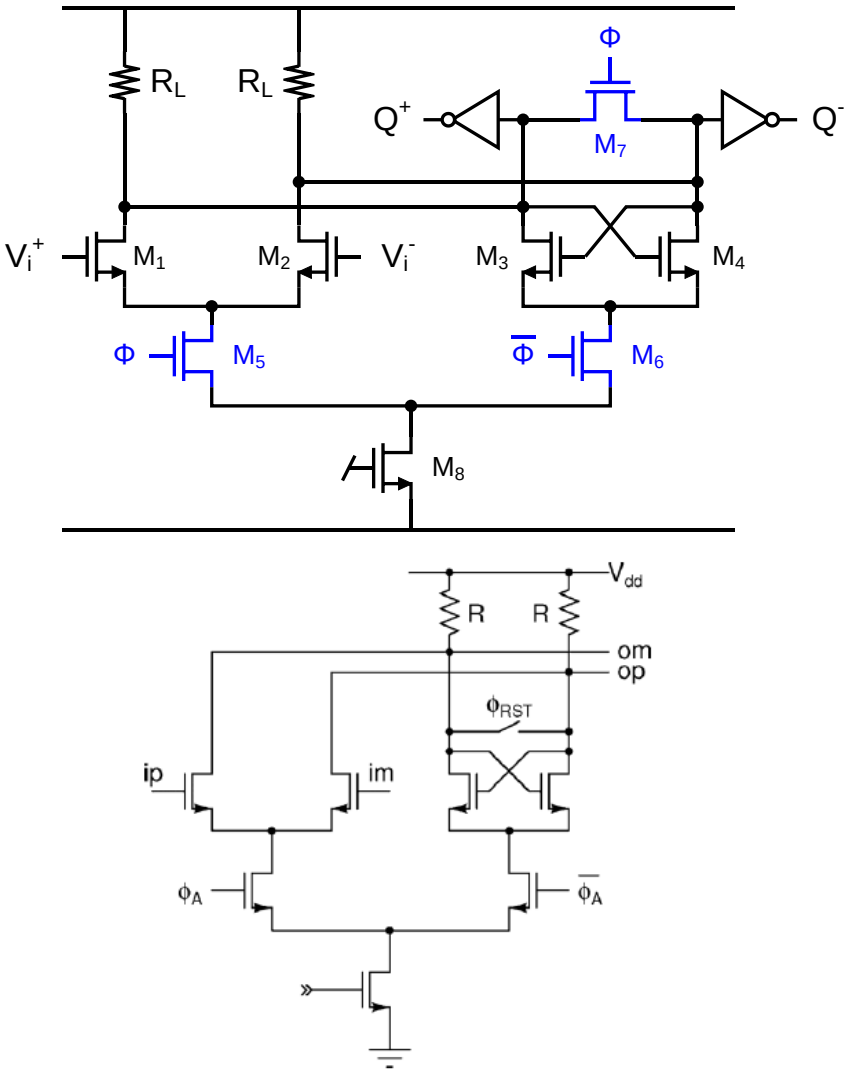
Dynamic Latch 2



- Zero DC current in reset mode
- Q^+ and Q^- are both reset to "0"
- Full logic level after regeneration
- Slow

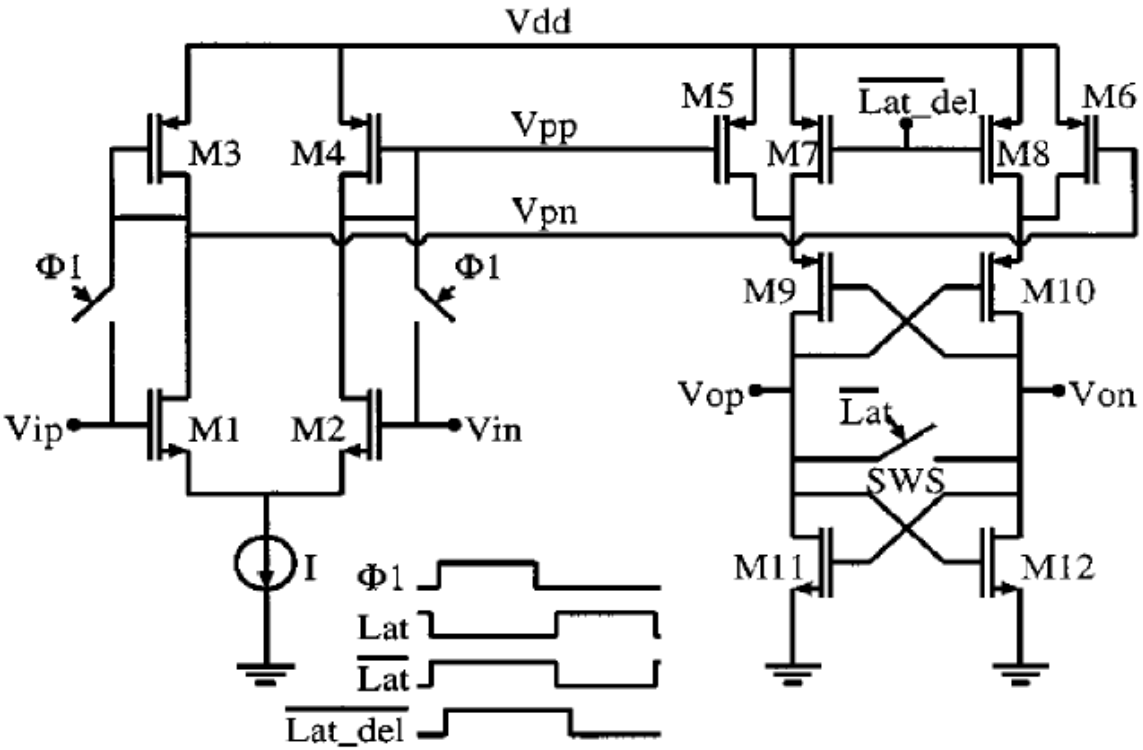
Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *JSSC*, vol. 30, pp. 166-172, issue 3, 1995.

Current-Steering/CML Latch



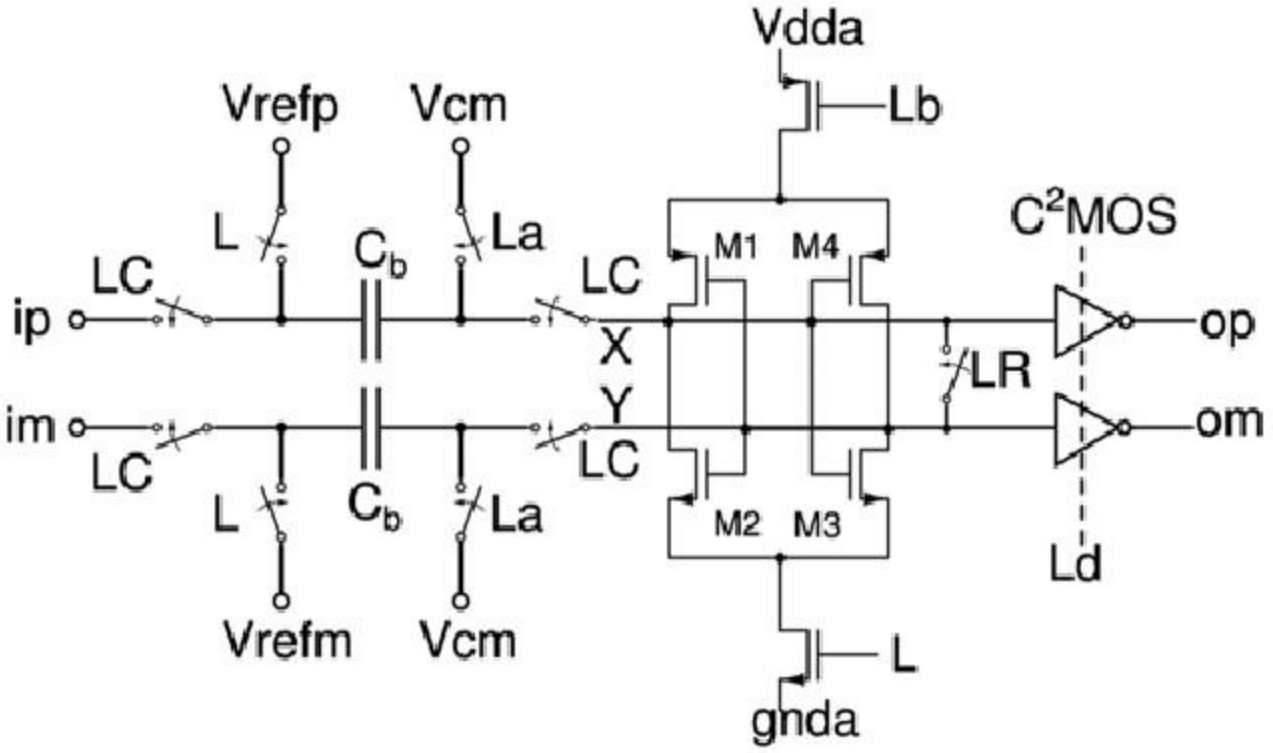
- Current mode logic (CML) latch
- Constant current → supply very quite
- Higher gain in tracking mode
- Cannot produce full logic levels
- Fast
  - Popular for high-speed designs
- Trip point of the inverters

PA Autozeroing Example



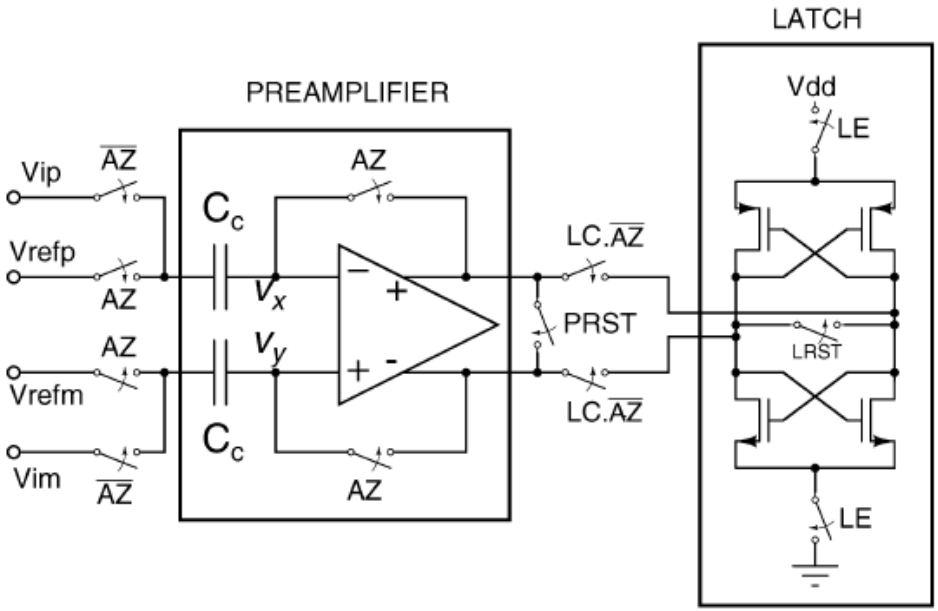
I. Mehr and L. Singer, “A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC,” IEEE JSSC March 2000, pp. 318-25.

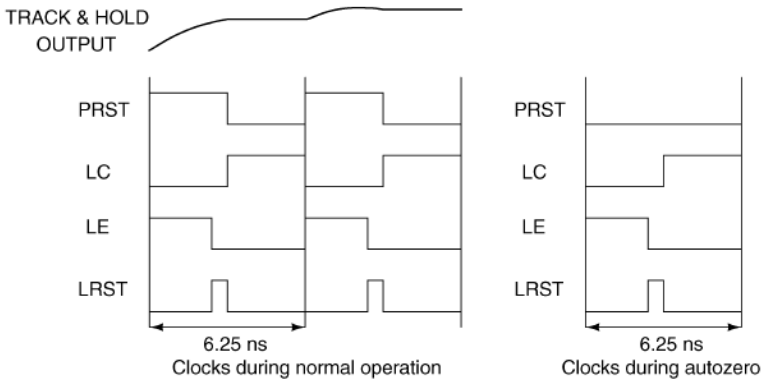
Reference Subtraction

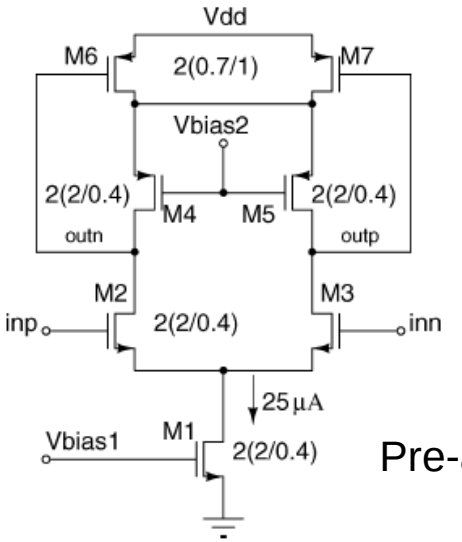


S. Pavan, N. Krishnapura, R. Pandarinathan, P. Sankar, "A Power Optimized Continuous-time Delta-Sigma Modulator for Audio Applications," IEEE JSSC, vol. 43, no. 2, pp. 351-360, Feb. 2008.

Autozeroing and Reference Subtraction



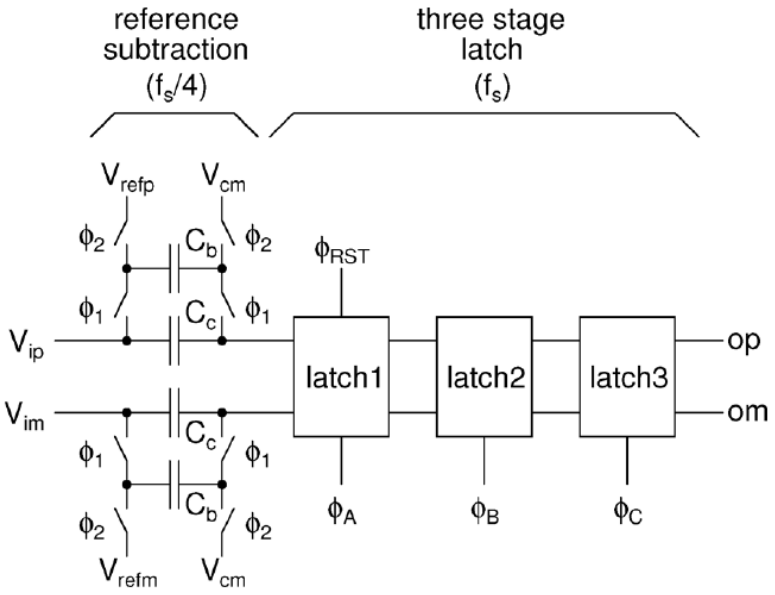


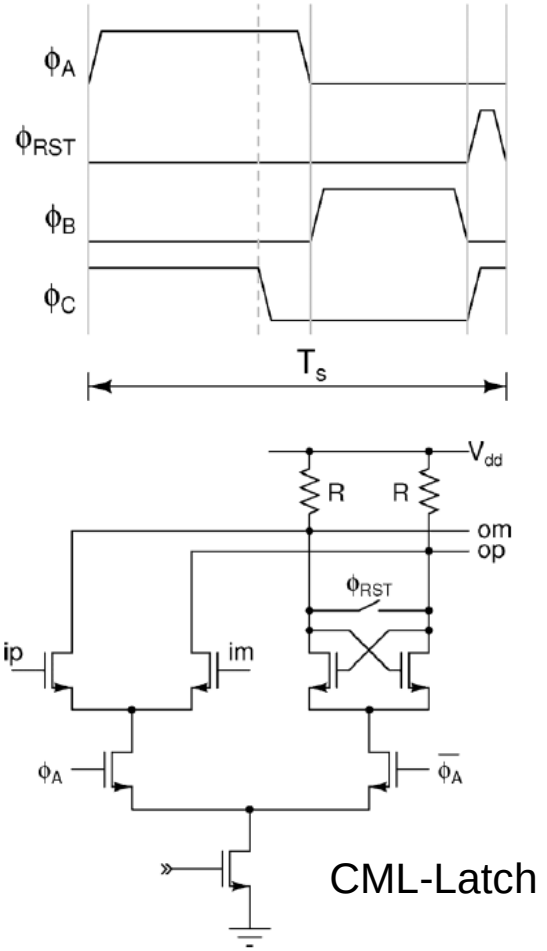


Pre-amp

V. Srinivas, S. Pavan, A. Lachhwani, and N. Sasidhar, “A Distortion Compensating Flash Analog-to-Digital Conversion Technique," IEEE JSSC, vol. 41, no. 9, pp. 1959-1969, Sep. 2006.

CML based Comparator





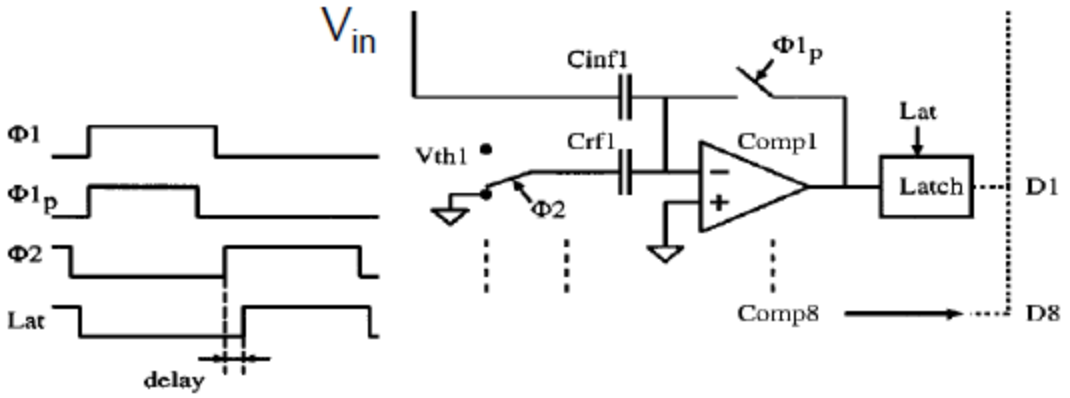
CML-Latch

V. Singh, N. Krishnapura, S. Pavan, B. Vigraham, D. Behera, and N. Nigania, “A 16MHz BW 75 dB DR CT ΔΣ ADC Compensated for More Than One Cycle Excess Loop Delay," IEEE JSSC, vol. 47, no. 8, Aug. 2012.

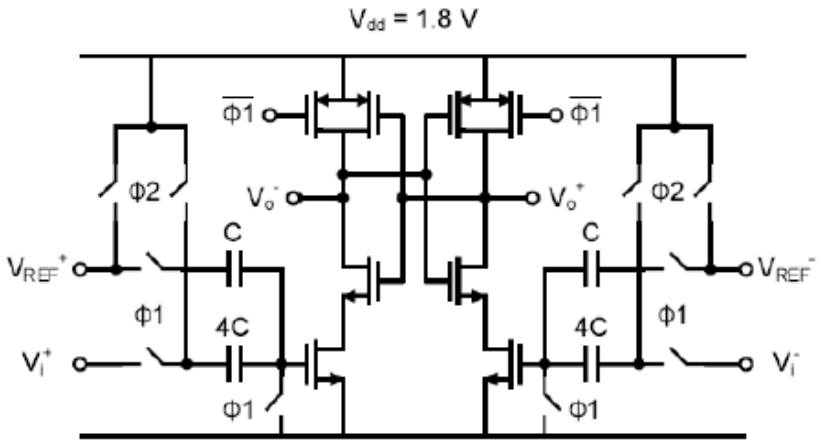
Comparators for Pipelined ADCs

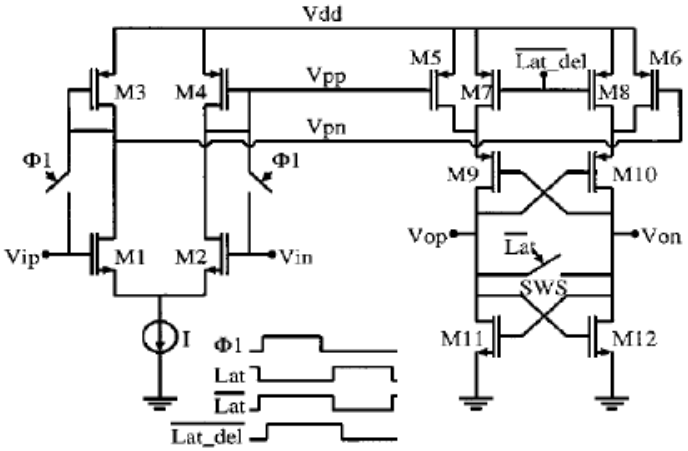
- Pipelined ADCs employ at least 0.5 bit/stage redundancy
  - Can tolerate large offsets and large noise with appropriate redundancy
- Should consume negligible power in a good design
  - 50-100 mW or less per comparator
- Lots of implementation options
  - Resistive/capacitive reference generation
  - Different pre-amp/latch topologies

Comparators for Pipelined ADCs



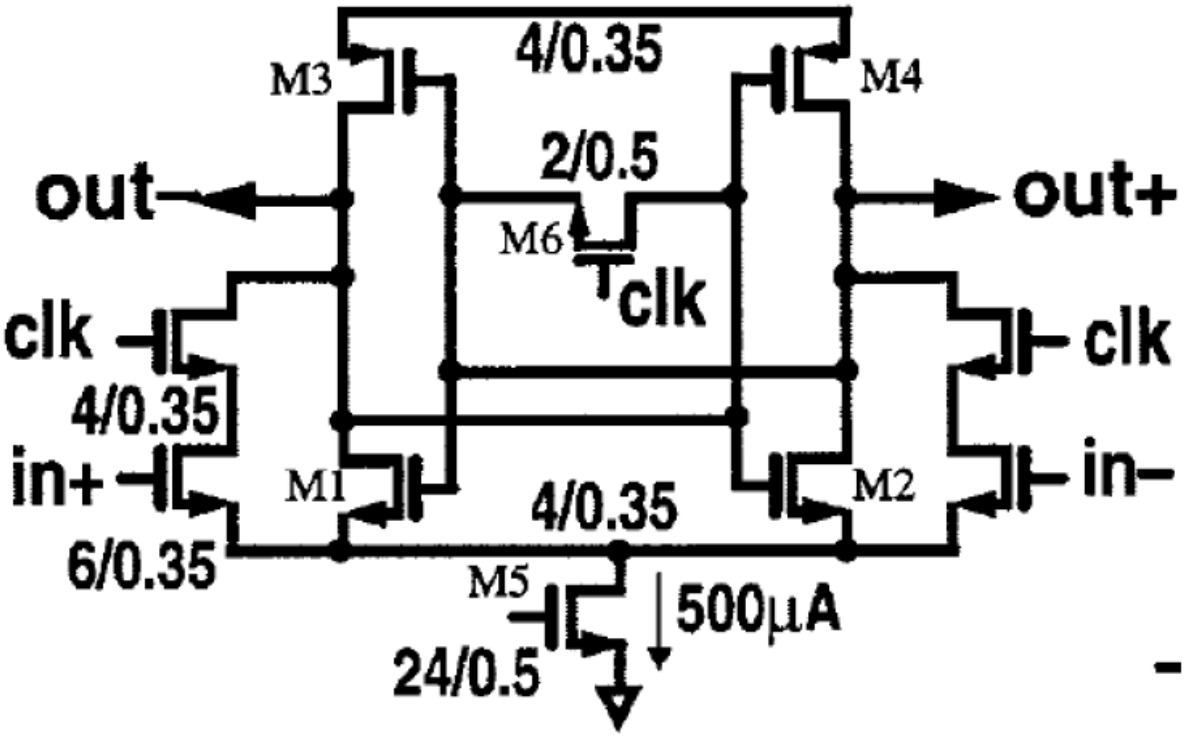
[Chiu 2004]





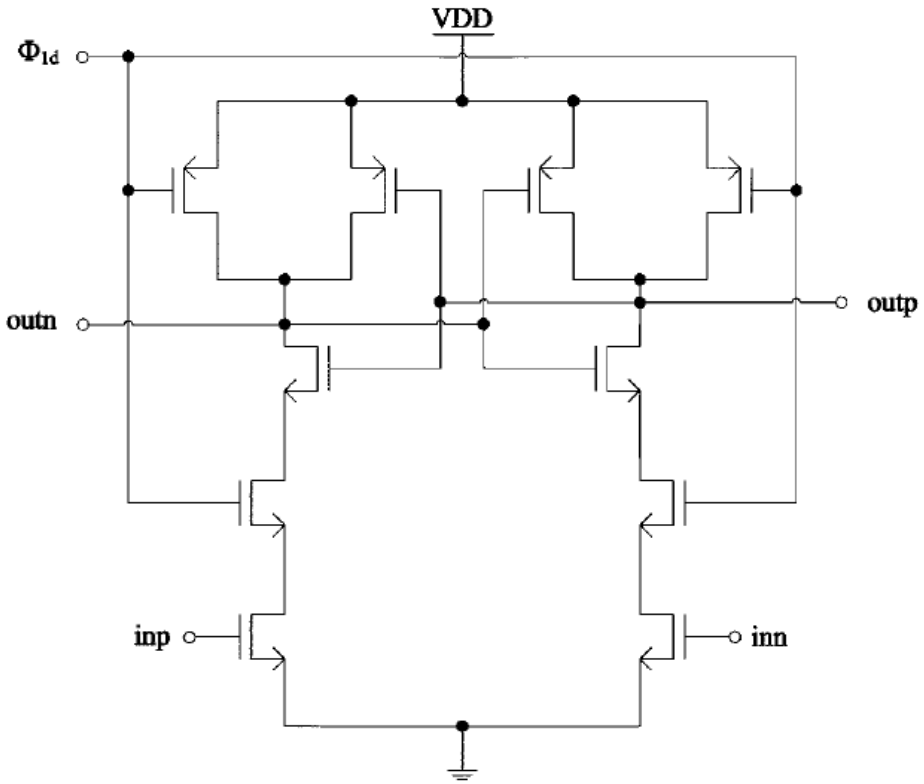
[Mehr 2000]

Comparator Example



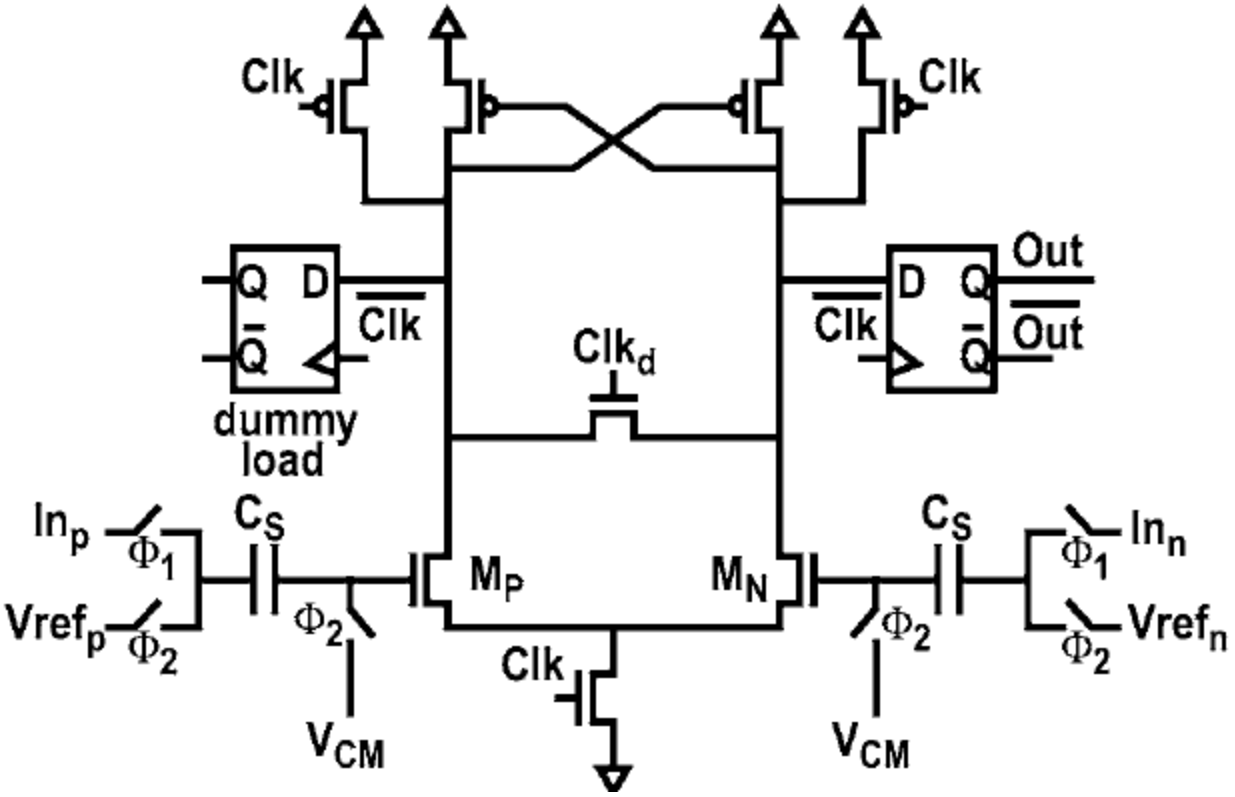
A 6-b 1.3-Gsample/s A/D Converter in 0.35-m CMOS
IEEE JSSC, vol. 36, no. 12, Dec 2001.

Latch Example



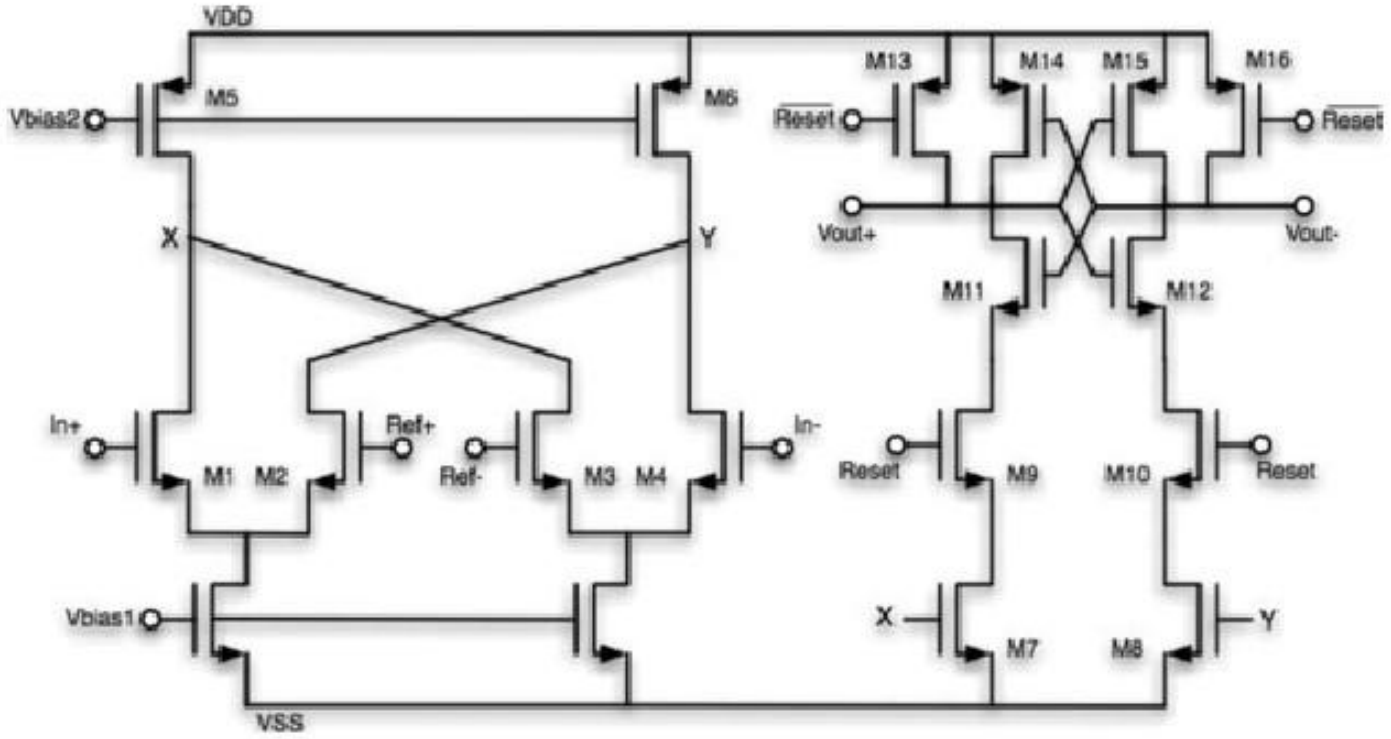
A 0.9-V 60-W 1-Bit Fourth-Order Delta-Sigma Modulator With 83-dB Dynamic Range
IEEE JSSC, vol. 43, no. 2, Feb. 2008

Comparator Example



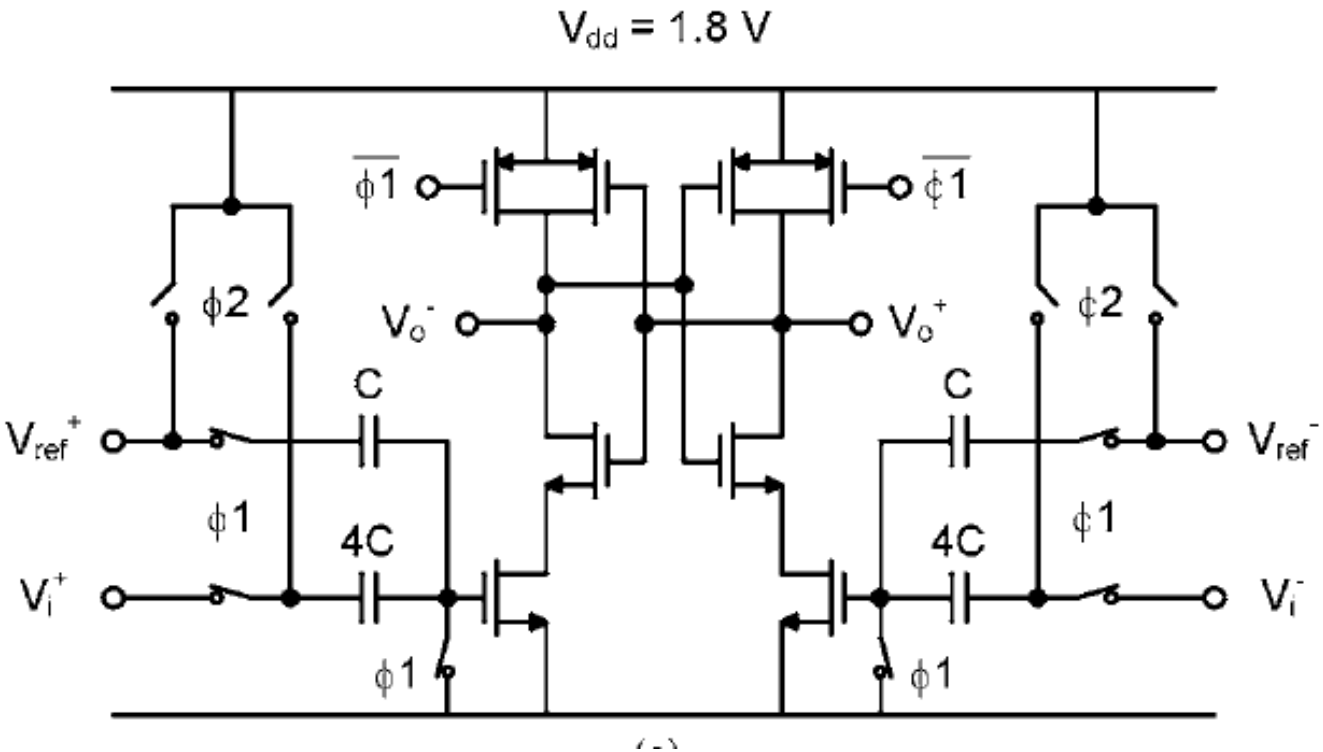
A 77-dB Dynamic Range, 7.5-MHz Hybrid Continuous-Time/Discrete-Time Cascaded ΔΣ Modulator, IEEE JSSC, vol. 43, no. 4, Apr 2008

Comparator Example



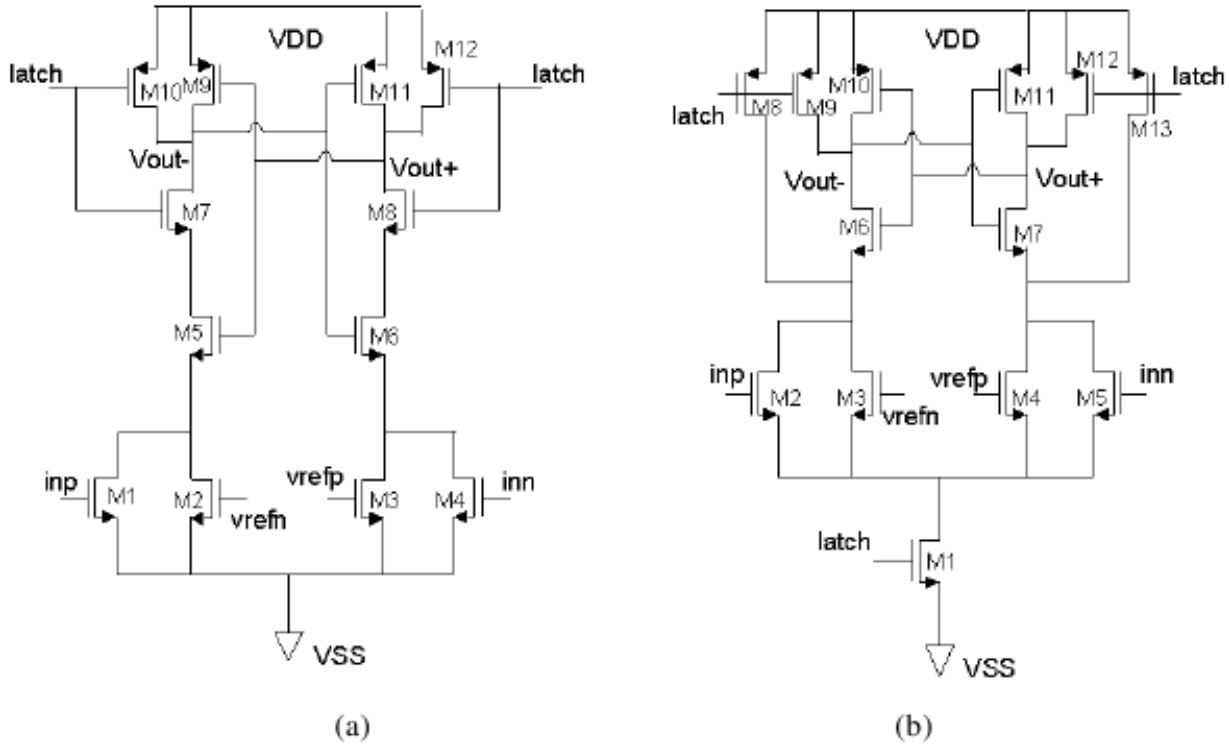
I. Galdi, 40 MHz IF 1 MHz Bandwidth Two-Path Bandpass ΣΔ Modulator With 72 dB DR Consuming 16 mW, IEEE JSSC, vol. 39, no. 8, pp. 1341–1346, Aug. 2004.

Comparator Example



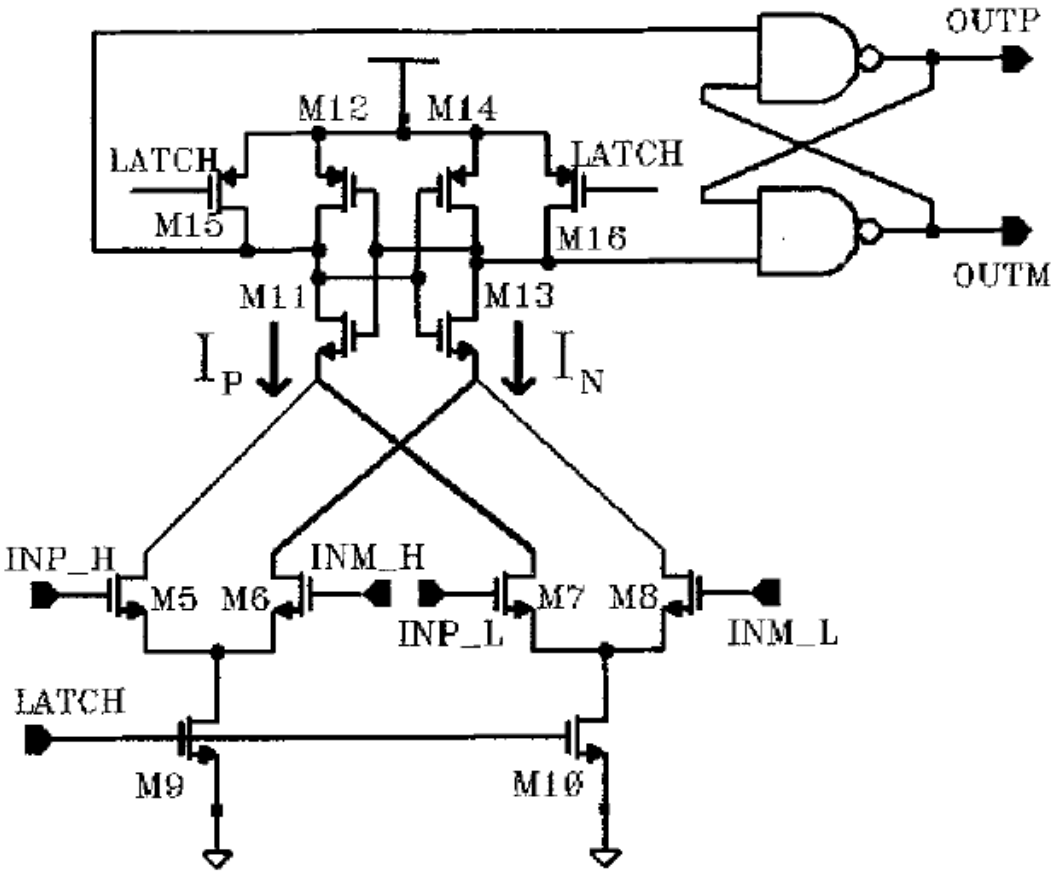
Y. Chiu, P. R. Gray, and B. Nikolic, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," IEEE JSSC, vol. 39, pp. 2139 - 2151, December 2004.

Comparator Example



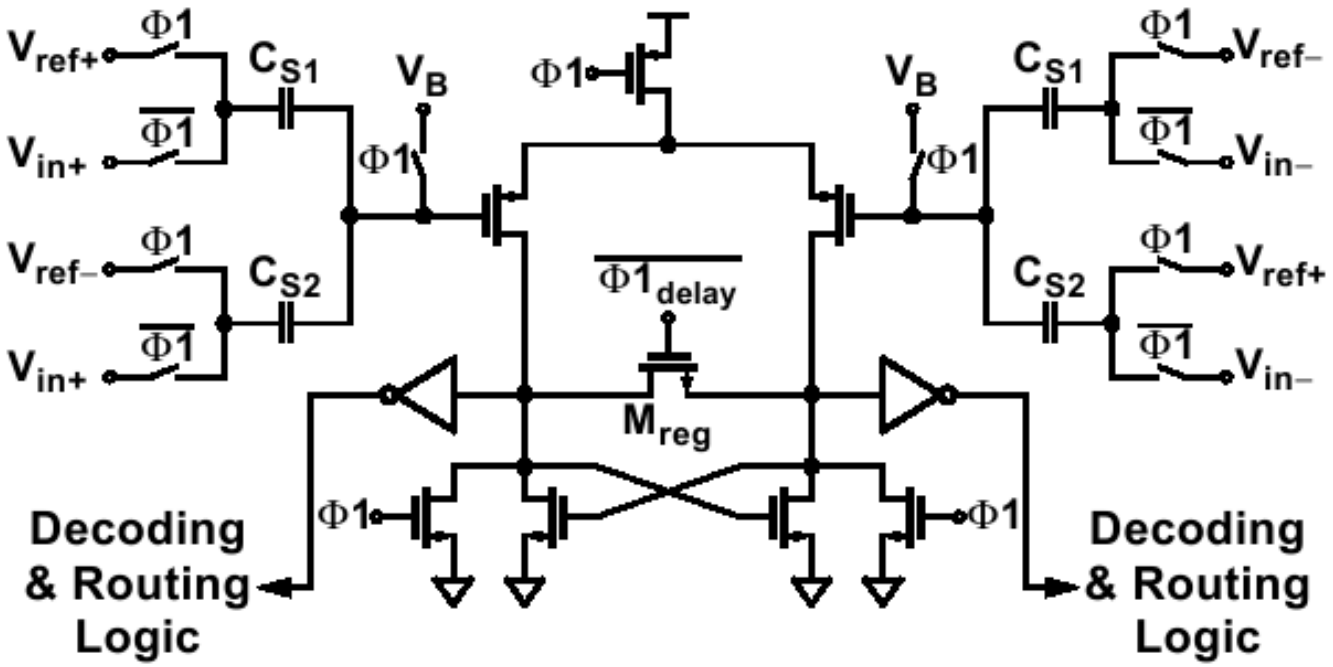
B. Min, P. Kim, F. W. Bowman, D. M. Boisvert, and A. J. Aude, "A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC," IEEE JSSC, vol. 38, pp. 2031 - 2039, Dec. 2003.

Comparator Example



J. Lin and B. Haroun, "An embedded 0.8 V/480 µW 6B/22 MHz flash ADC in 0.13 µm digital CMOS Process using a nonlinear double interpolation technique," IEEE JSSC, vol. 37, pp. 1610 - 1617, Dec. 2002.

Comparator Example



S . Limotyrakis, S. D. Kulchycki, D. Su, and B. A. Wooley, "A 150MS/s 8b 71mW time-interleaved ADC in 0.18µm CMOS," proc. IEEE ISSCC, pp. 258 - 259, Feb 2004.

Exercise

- Compare the latches with respect to
  - Static power dissipation
  - Dynamic and static Offsets
  - Kickback noise at the input
  - Number of clock phases
  - Maximum achievable clock speed

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4. B. Boser, *Analog-Digital Interface Circuits Lecture Slides,* UC Berkeley 2011*.*