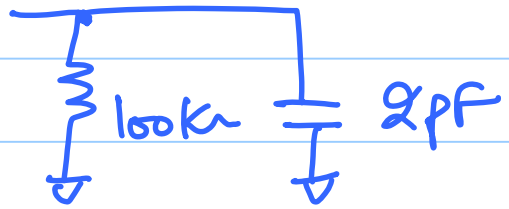
ECE 511 – Project Help

Note Title 4/18/2015

Table 1: Opamp design specifications.

Parameter	Specified Value
Technology	TSMC 180n CMOS
Supply voltage, V_{DD}	1.8 V
Typical load	$100k\Omega \| \| 2pF$
Unit gain frequency (f_{un})	$> 50\,MHz$ *for ECE 411*
	$> 200\,MHz$ *for ECE 511*
Open-loop gain (A_{OL})	$> 75\,dB$
Slew-rate (SR)	$> 500\frac{V}{\mu s}$
Phase margin (ϕ_M)	$\gtrsim 63^\circ$
Power consumption	Minimum possible



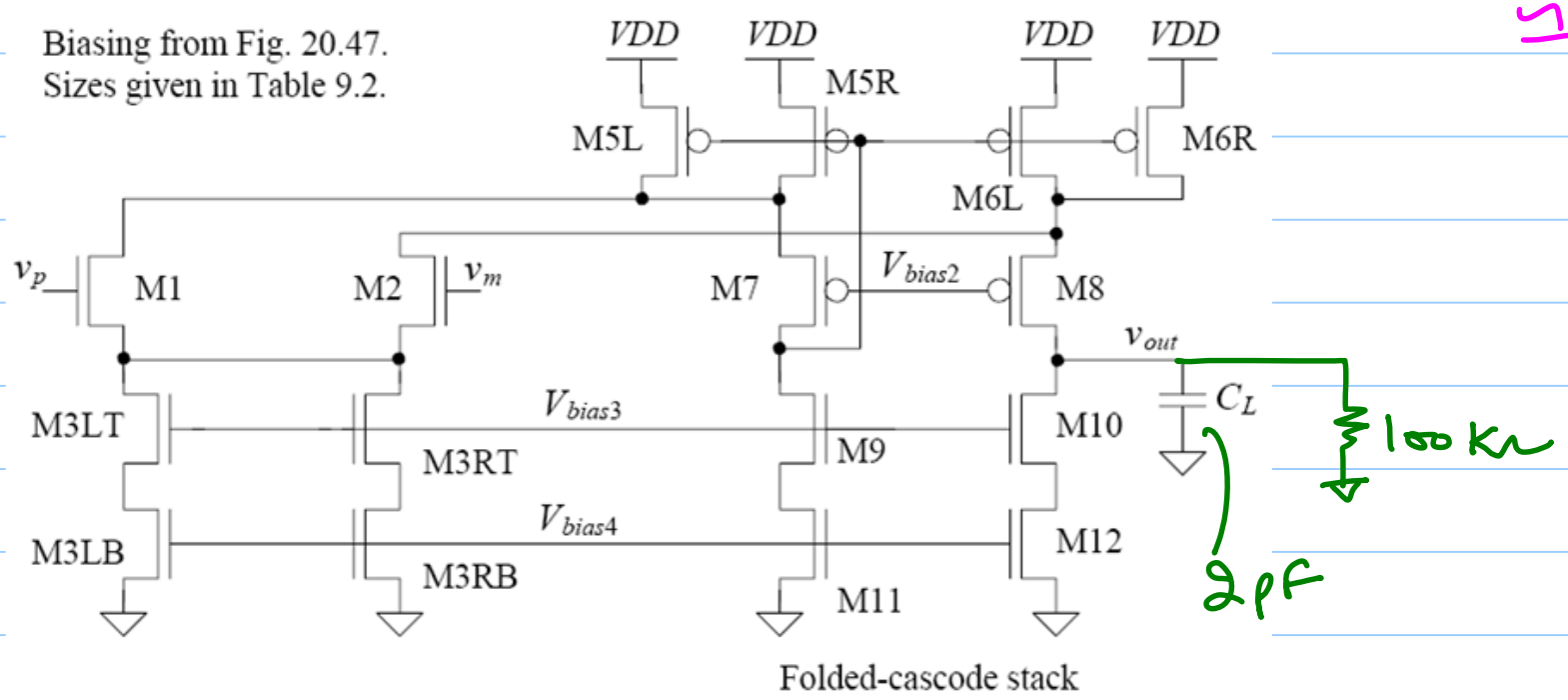


Figure 24.42 A folded-cascode OTA.

$R_{oamp} \| R_{ocasn} \approx 10\,M\Omega$

$100\,k\Omega$

$2\,pF$

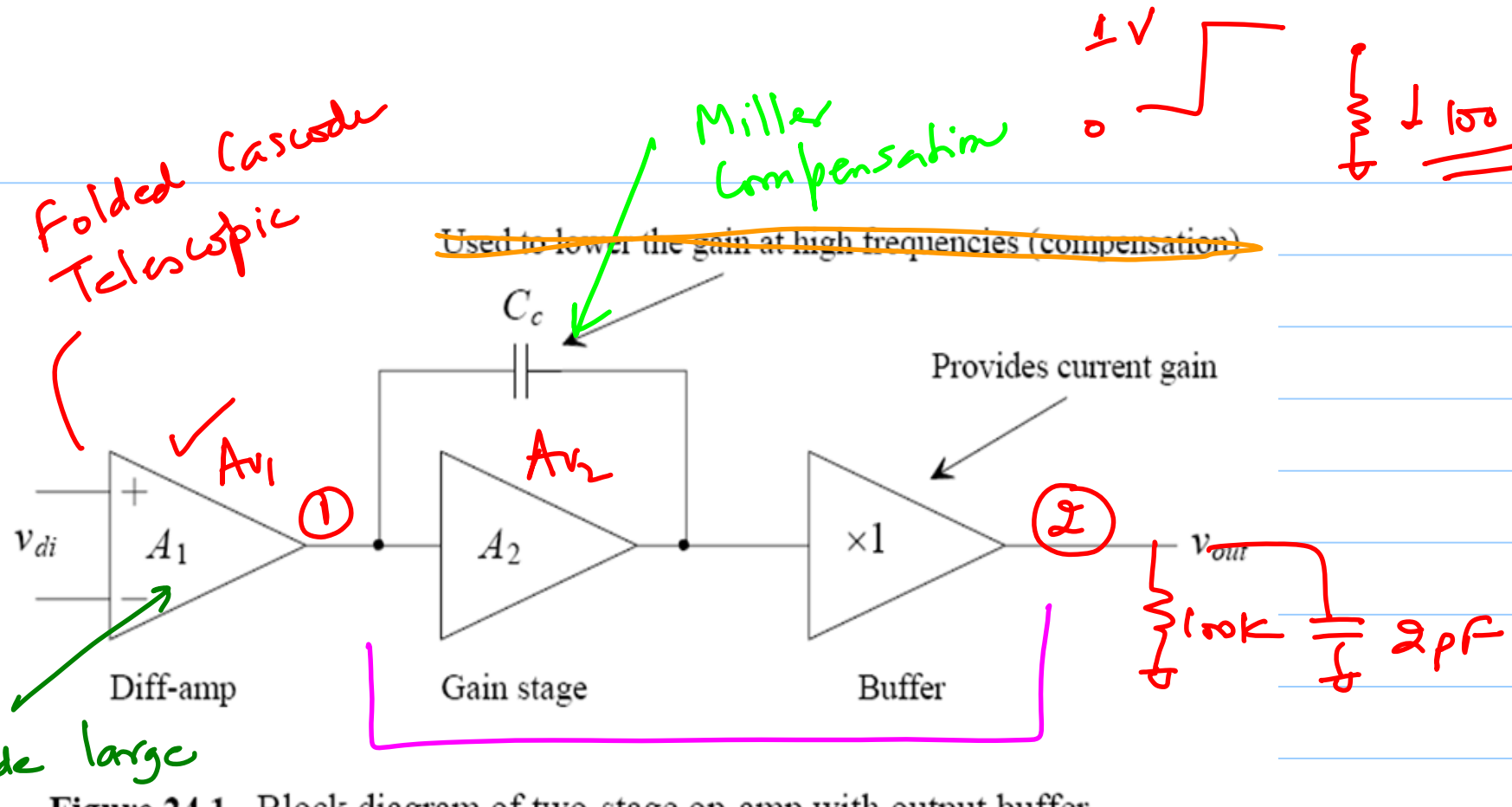
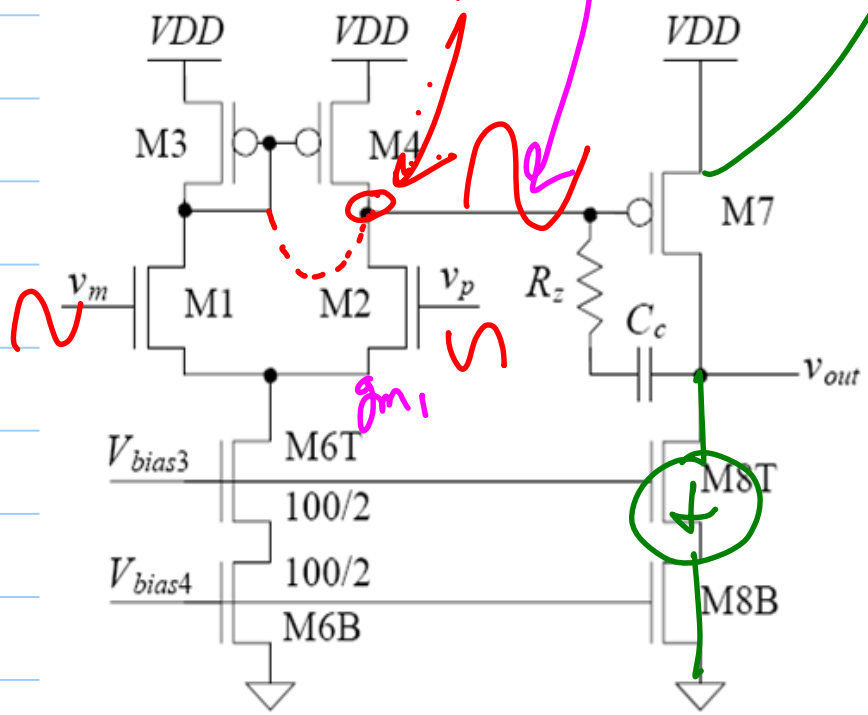
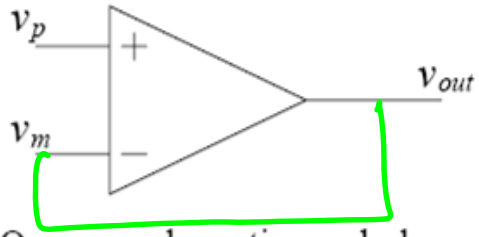


Figure 24.1 Block diagram of two-stage op-amp with output buffer.



Parameters from Table 9.2 with biasing circuit from Fig. 20.47. Unlabeled NMOS are 50/2 and PMOS are 100/2. Scale factor is 50 nm.



Op-amp schematic symbol

Figure 24.2 Basic two-stage op-amp.

Diffamp

Vbias

DC-level should be well defined

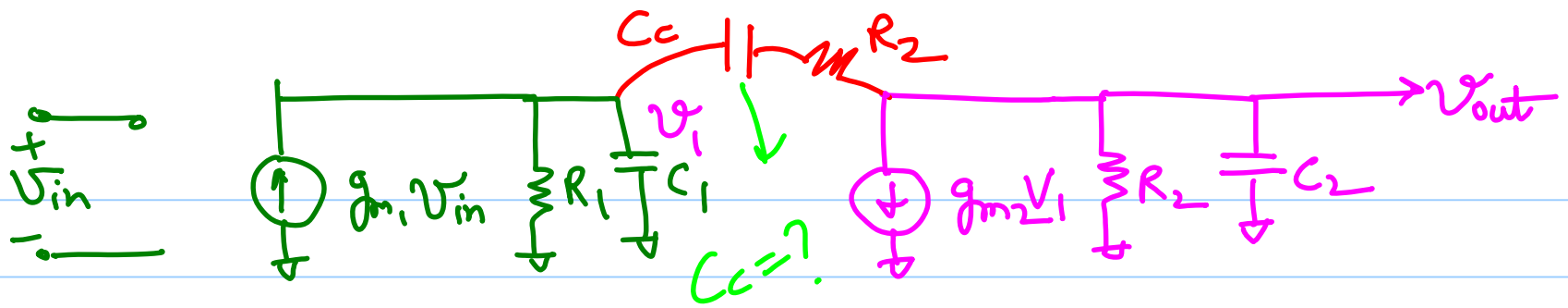
CS Amplifier

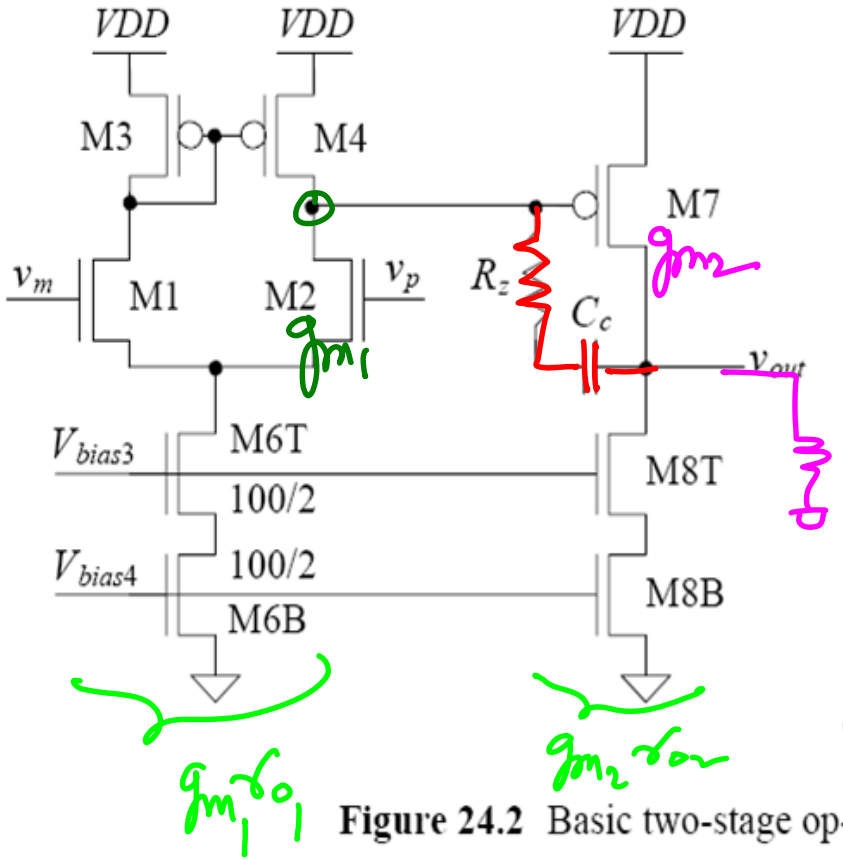
DC bias

g_{m_2}

g_{m_1}

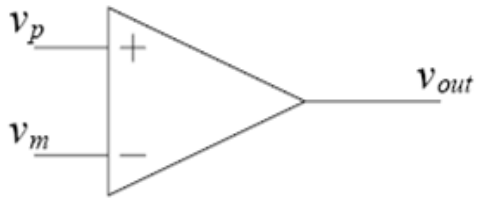
Diffamp output biases the 2nd-stage (CS stage) & transfers the signal





Parameters from Table 9.2 with biasing circuit from Fig. 20.47. Unlabeled NMOS are 50/2 and PMOS are 100/2. Scale factor is 50 nm.

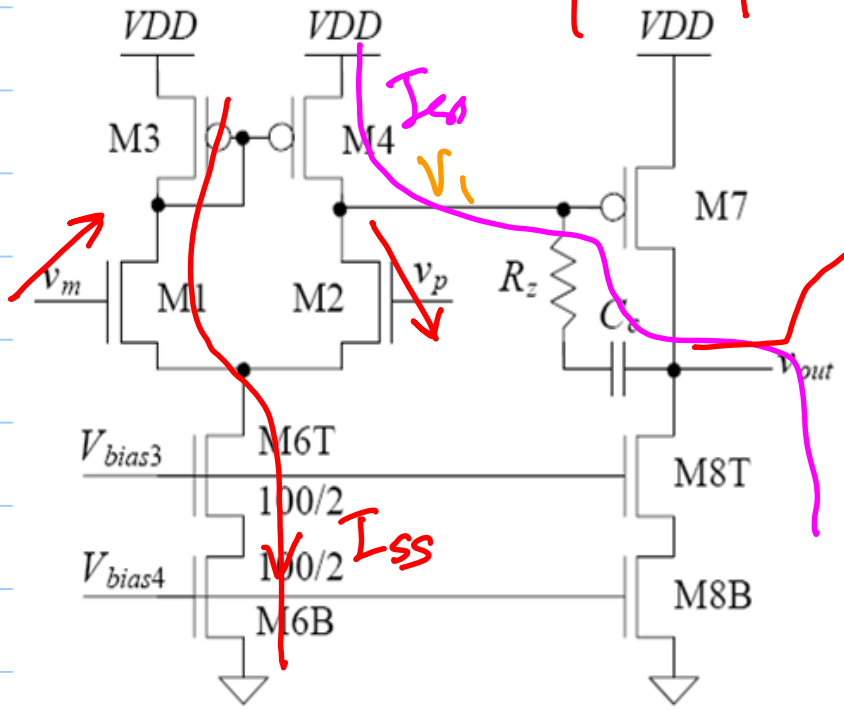
$f_{un} = \frac{1}{2\pi}\frac{g_{m1}}{C_c}$ ↑ g_m



Op-amp schematic symbol

Figure 24.2 Basic two-stage op-amp.

Class-A stage



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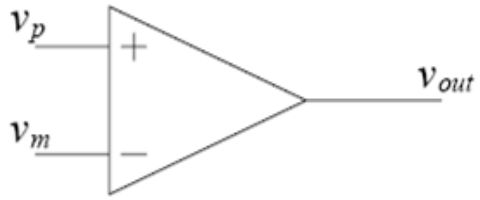
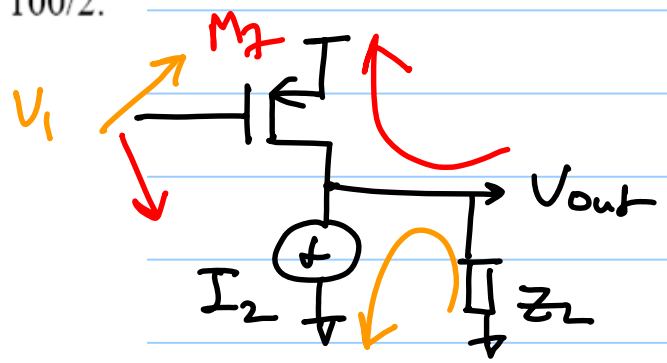


Op-amp schematic symbol



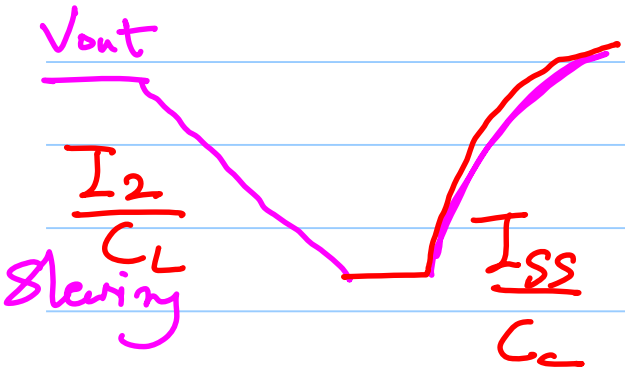
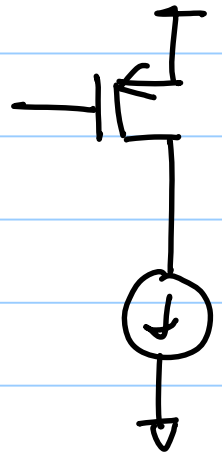
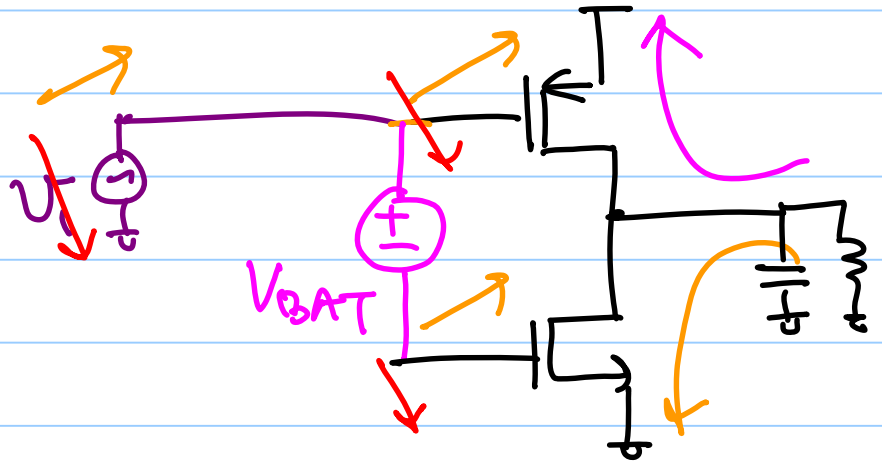


Figure 24.2 Basic two-stage op-amp.

Class-A



Class-AB

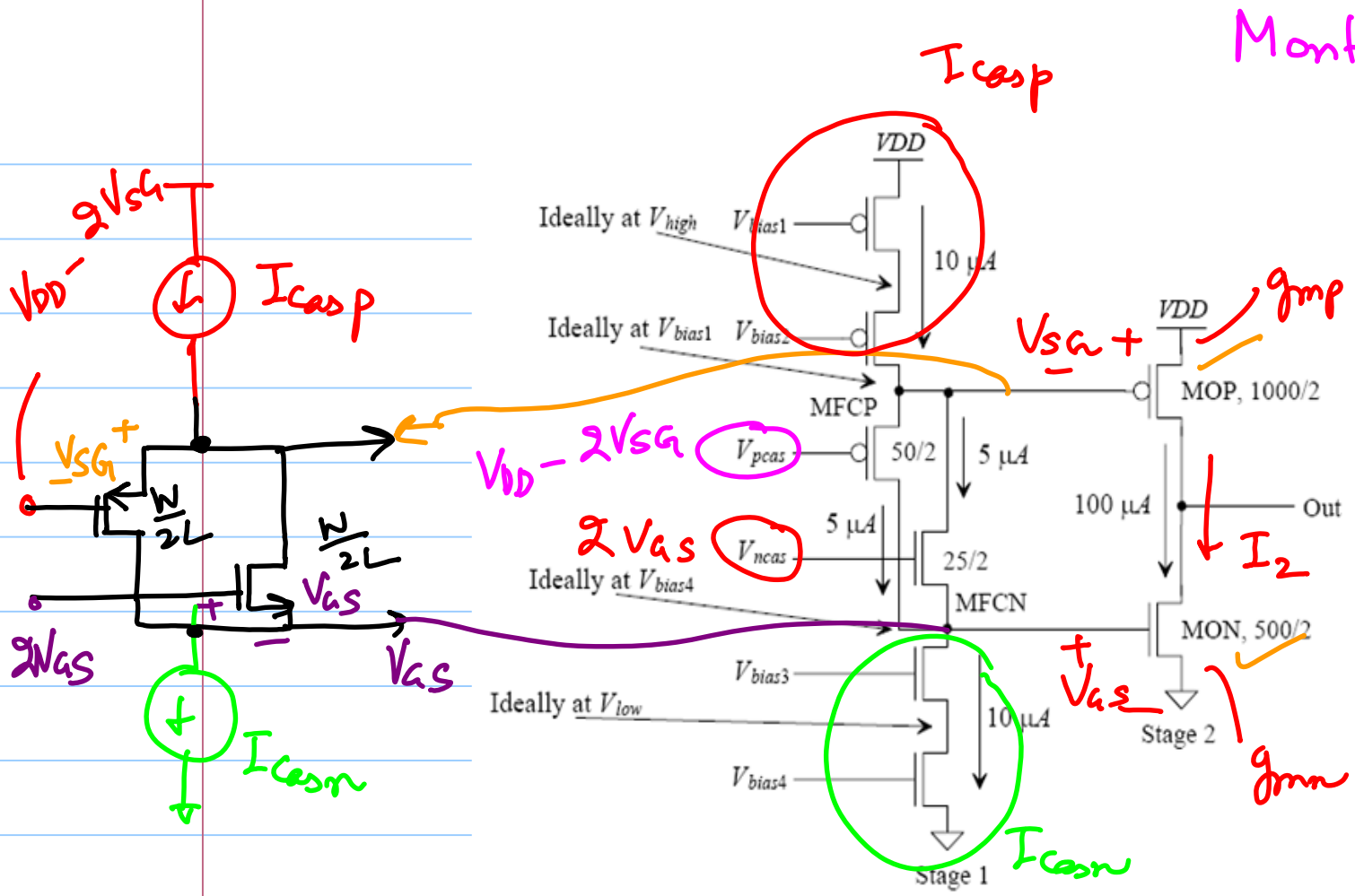


Either PMOS or NMOS drive the load

* transition should be smooth

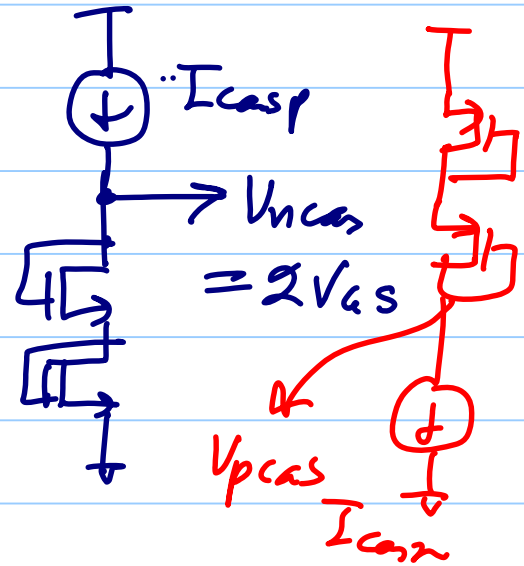
* No slewing

Monticelli Output stage (class-AB)



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2). Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 20.49 Biasing with a floating current source.



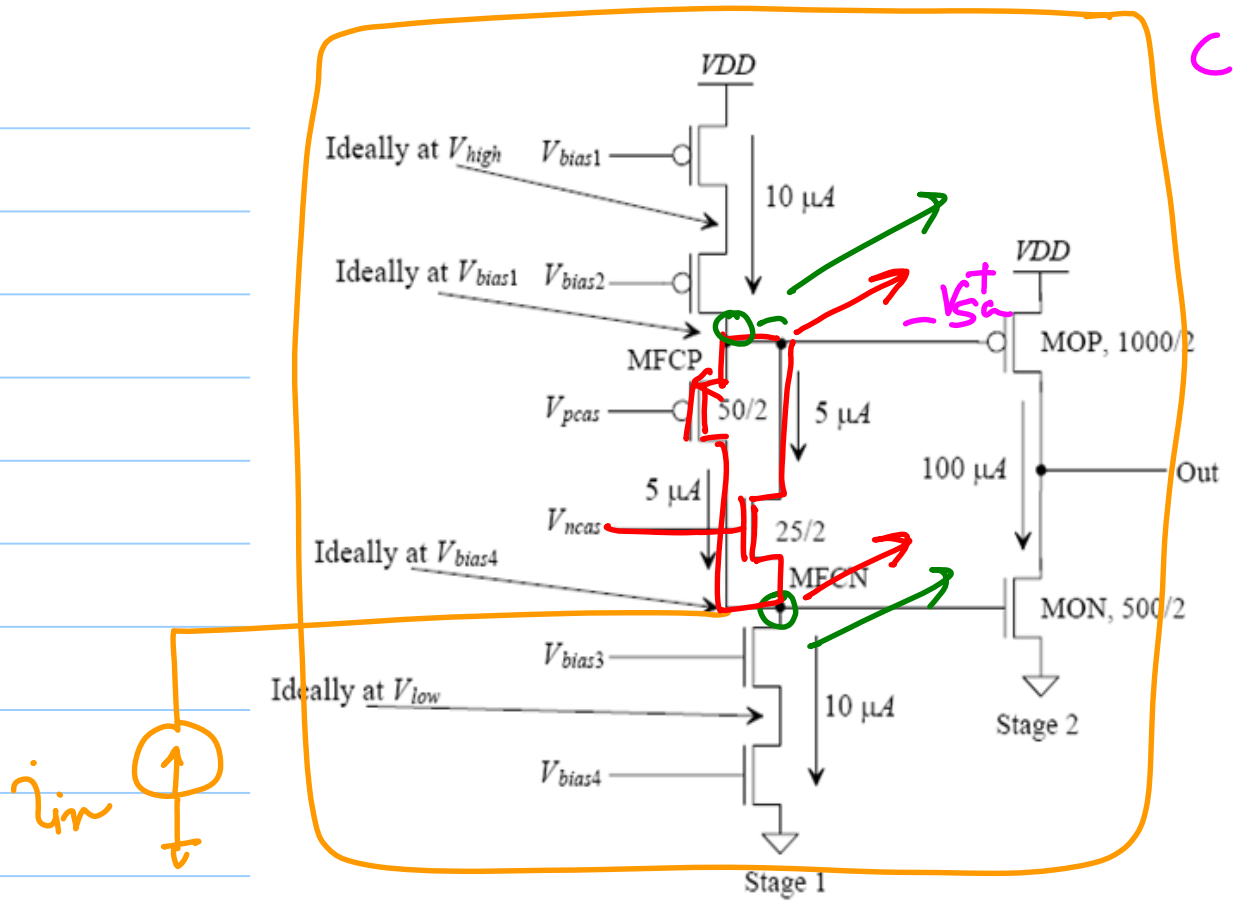


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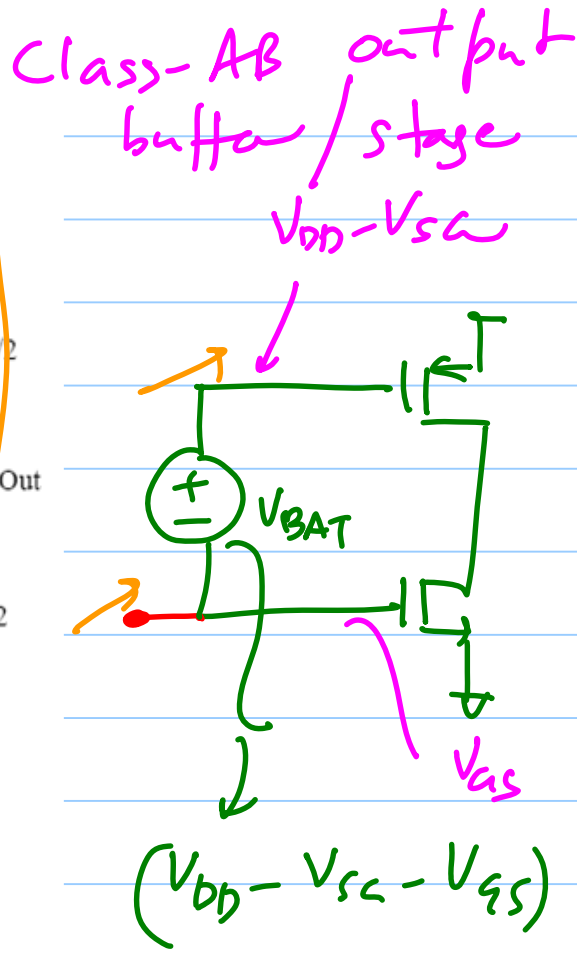
Figure 20.49 Biasing with a floating current source.



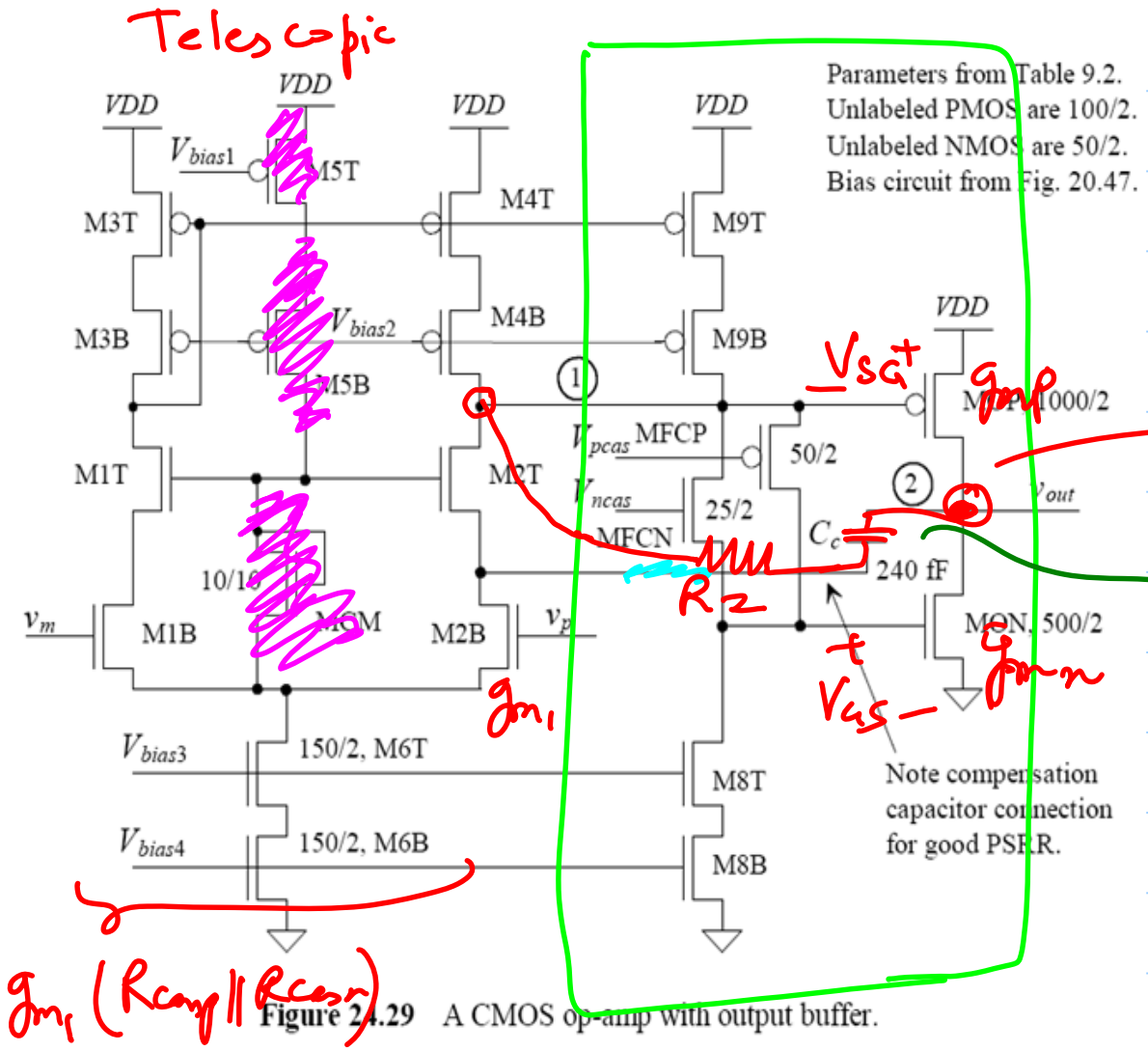


Figure 24.29 A CMOS op-amp with output buffer.

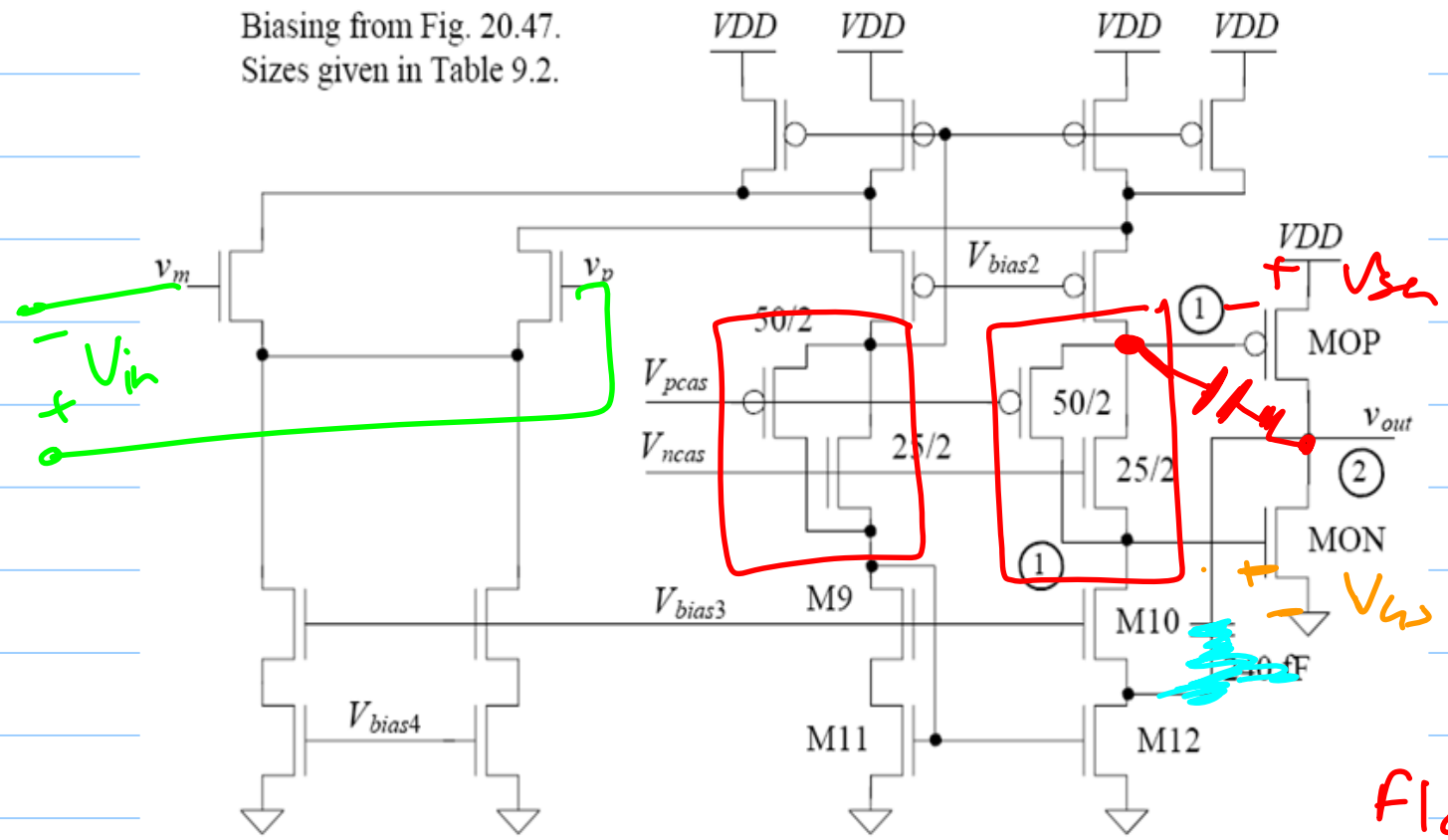
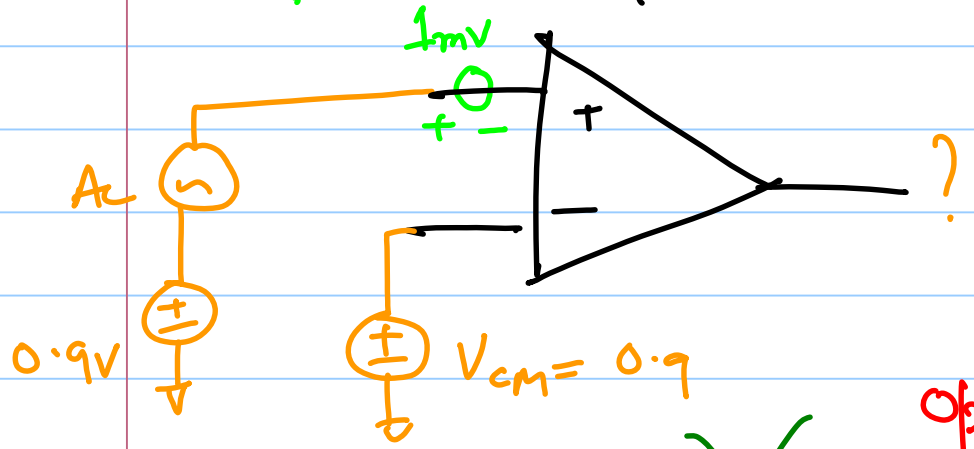


Figure 24.44 Folded-cascode op-amp with class AB output buffer.

Floating CM is merged with folded Cascode stage

DC offset

$A_V = 1000$ 60dB

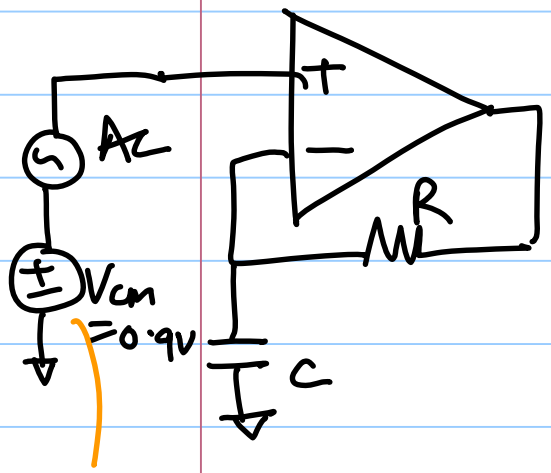


Open-loop Bode plot

↳ check phase margin

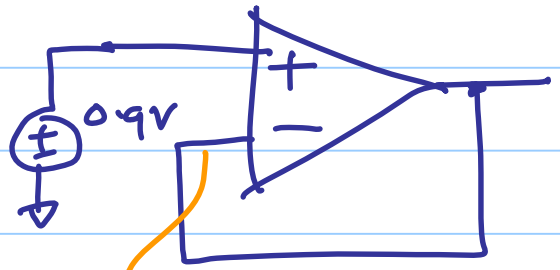
Open loop simulation

* I want to DC bias the opamp first & then run AC analysis



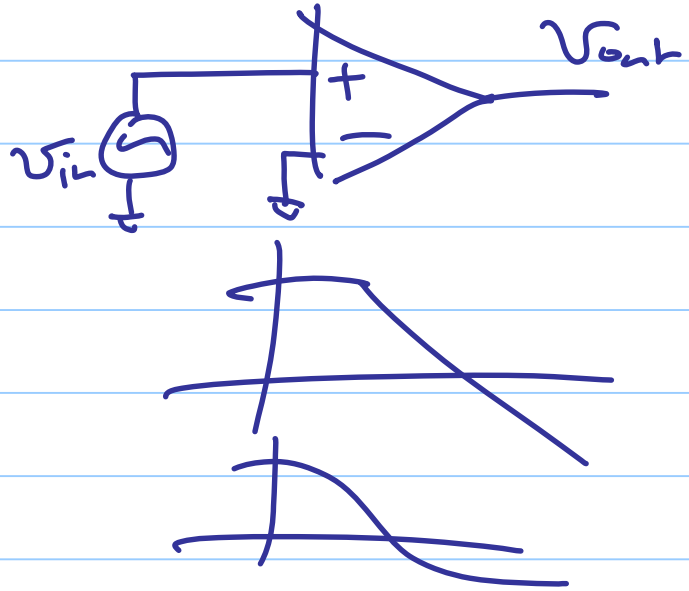
Should fall within the input CM-range

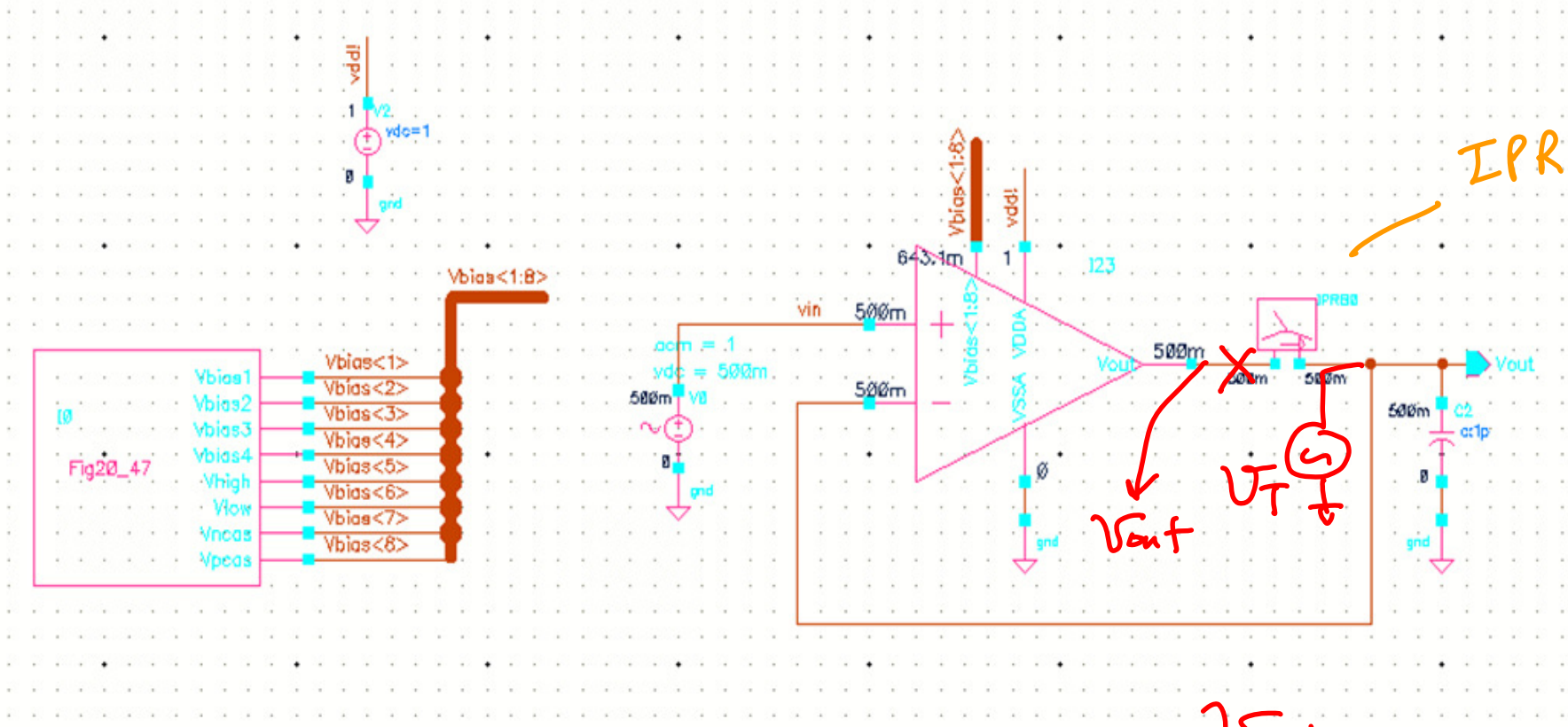
DC



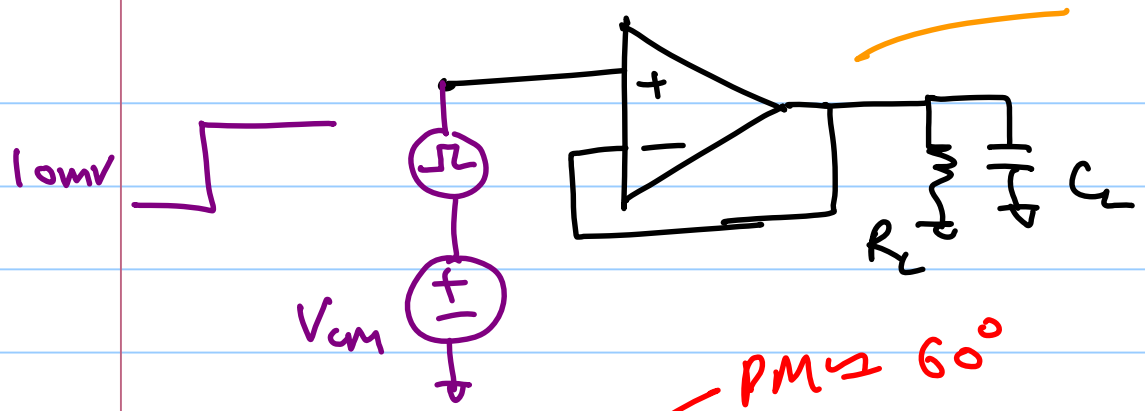
0.899 (due to finite Jain)

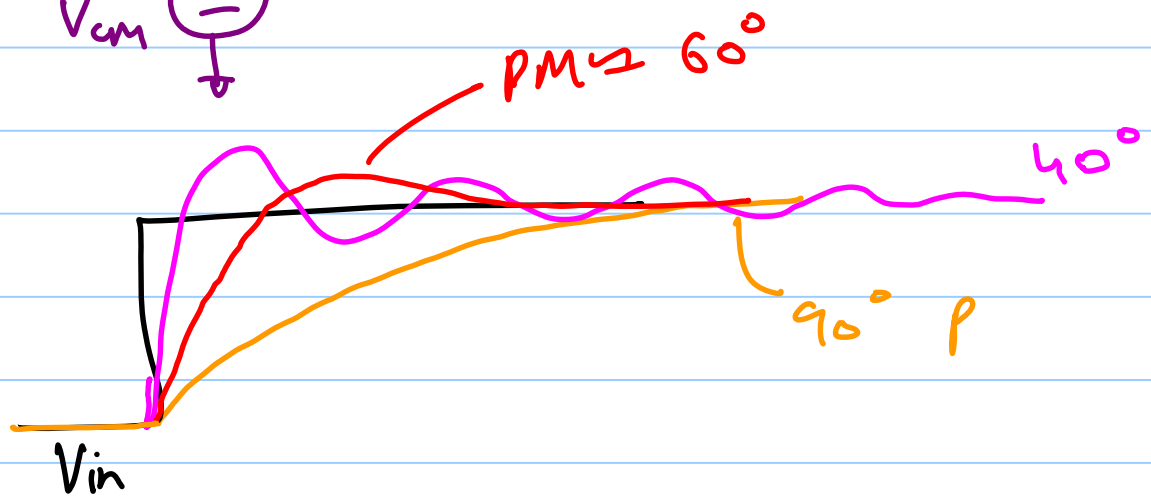
AC

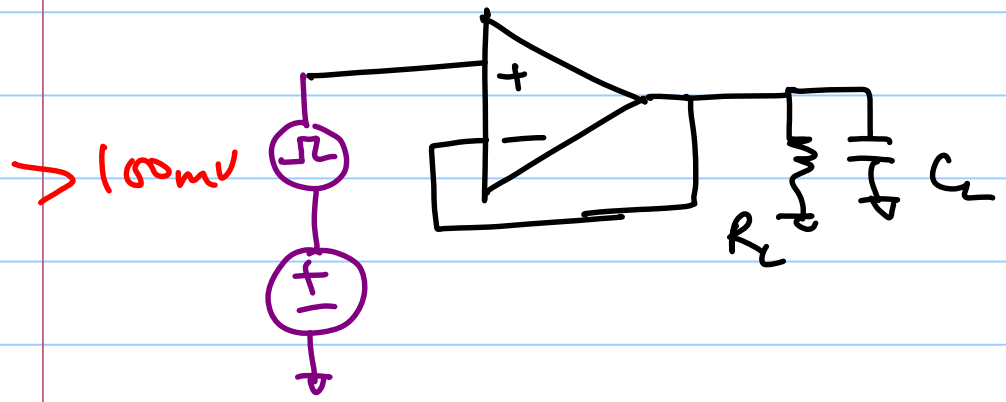



vdd!
V2
vdc=1
gnd
Vbias<1:8>
Fig20_47
Vbias1
Vbias2
Vbias3
Vbias4
Vhigh
Vlow
Vncas
Vpcas
Vbias<1>
Vbias<2>
Vbias<3>
Vbias<4>
Vbias<5>
Vbias<6>
Vbias<7>
Vbias<8>
643.1m
I23
vin
500m
acm = .1
vdc = 500m
V0
VDDA
VSSA
Vout
IPRB0
C2
c:1p
IPROBE
Vout
VT
Vout/VT(jω)

Transient response



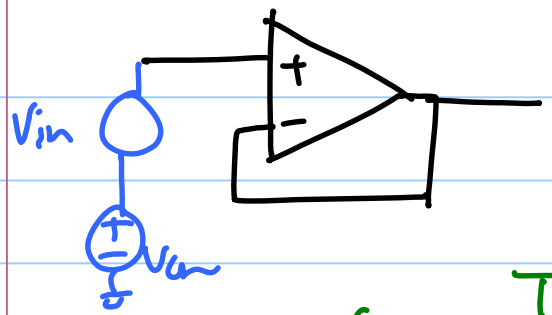




$$SR = \frac{\Delta V_{out}}{\Delta t} > \frac{500V}{\mu s}$$

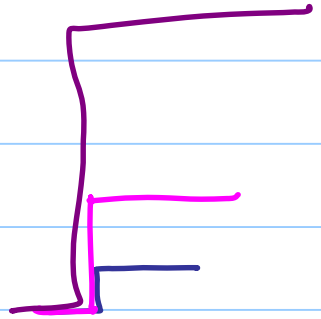
$$= 0.5 \frac{V}{ns}$$

With class AB $SR = \frac{I_{SS}}{C_L}$ ← first stage diff amp Tail Current



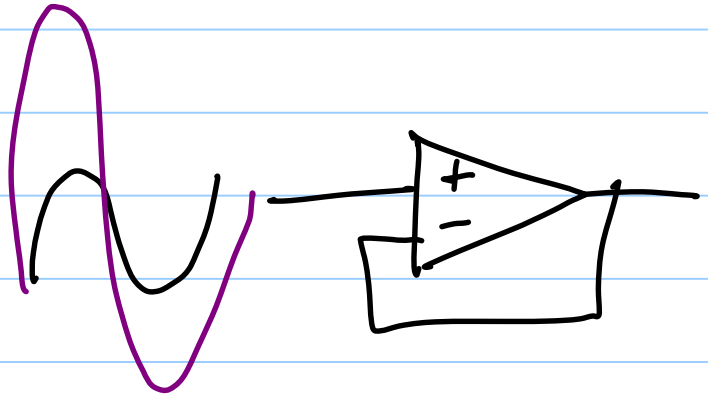
$$V_{out} = V_0 \left(1 - e^{-T/\tau}\right)$$

Ideal settling
(linear behavior)



not really proportional

non-linearity


+
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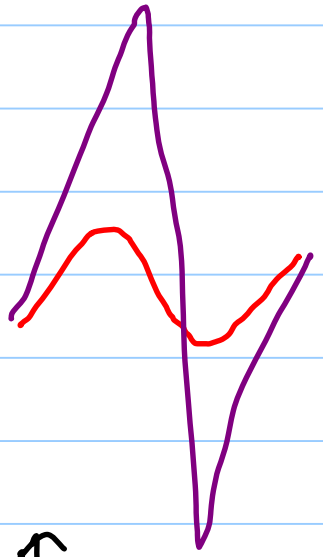
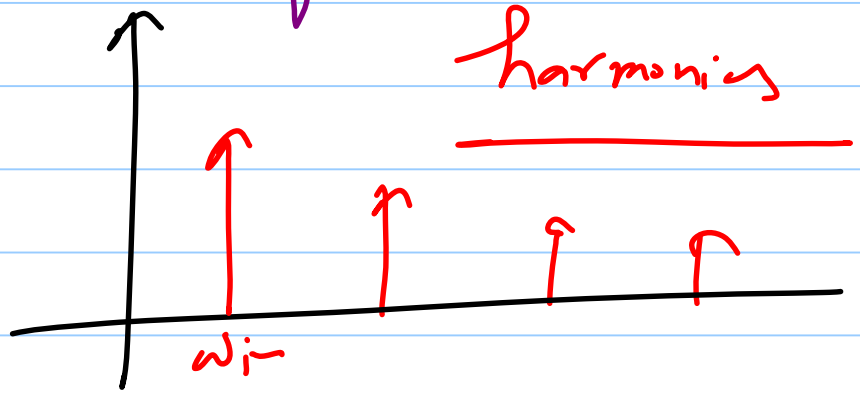



ω_{in}
f


harmonics
ω_{in}