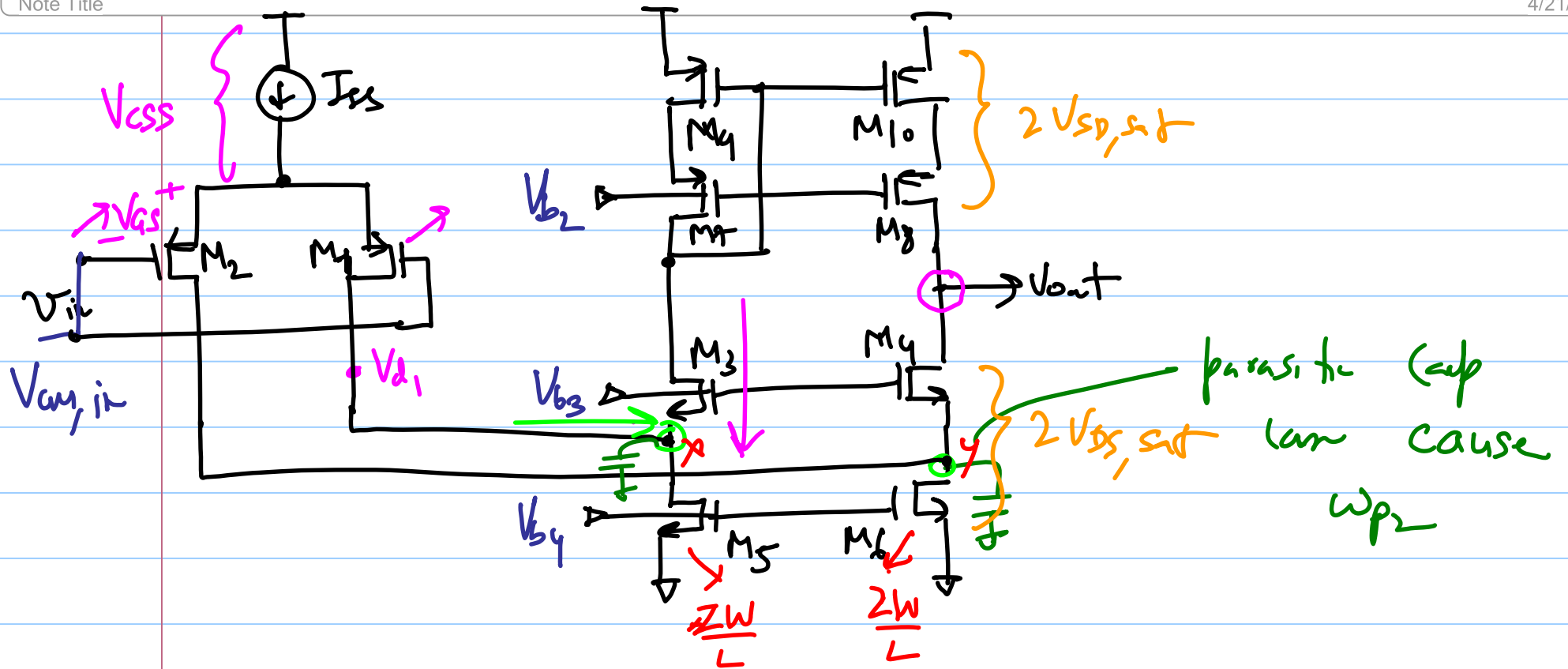


ECE 511 - Lecture 24

Note Title

4/21/2015

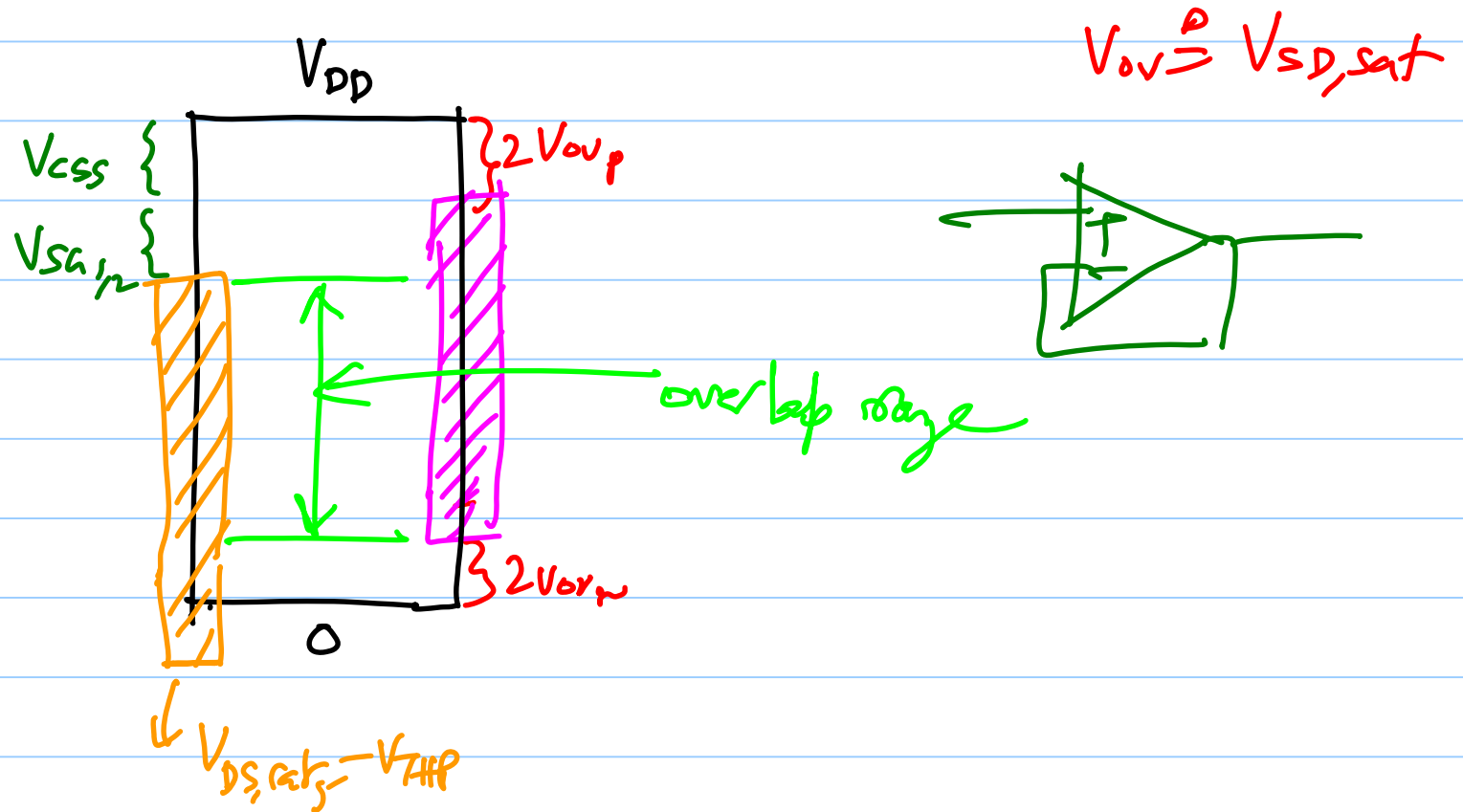


$$V_{cm,in} = V_{G1} > V_{D1} - V_{THP} \quad \& \quad V_{D1} \geq V_{DS,sat5}$$

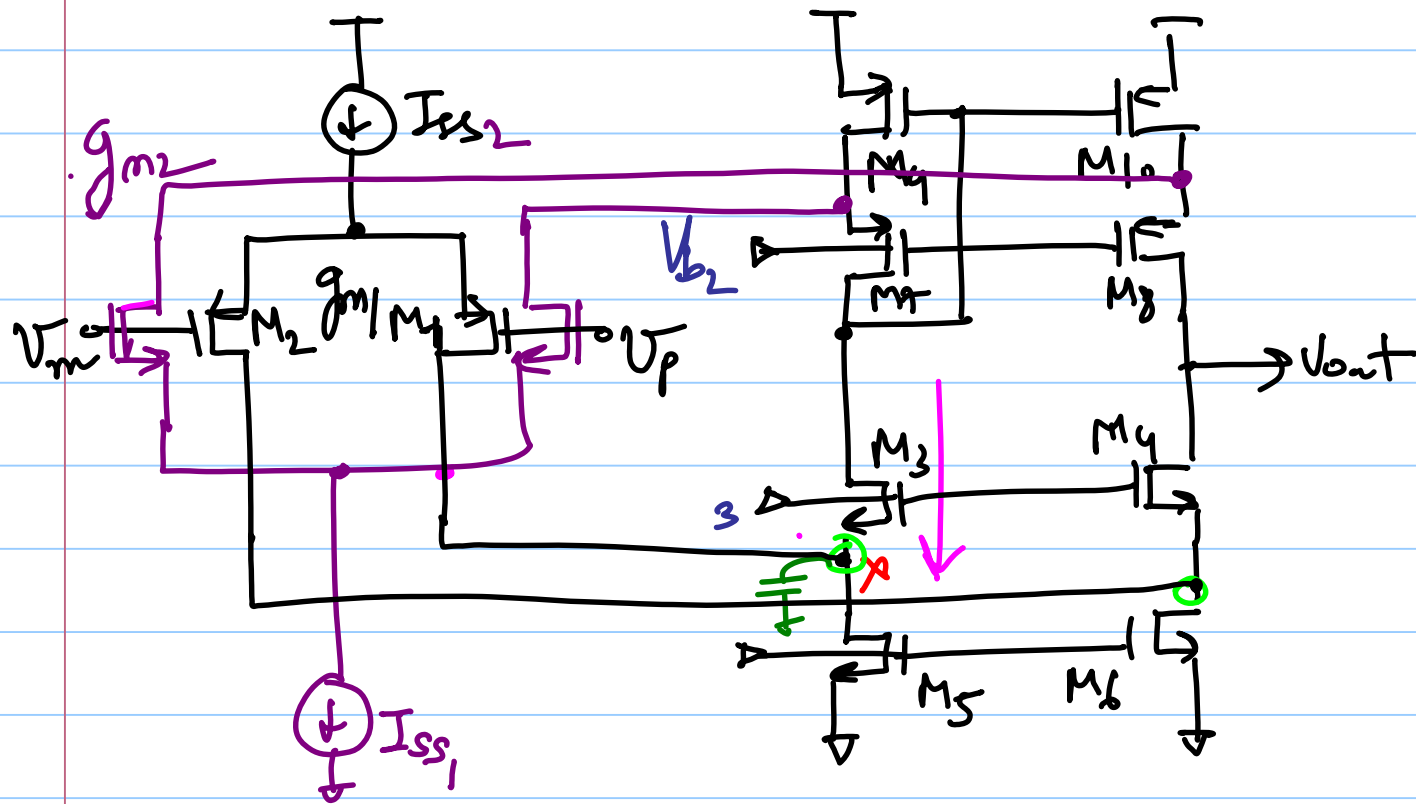
$$\boxed{V_{cm,in} \geq V_{DS,sat5} - V_{THP} < 0}$$

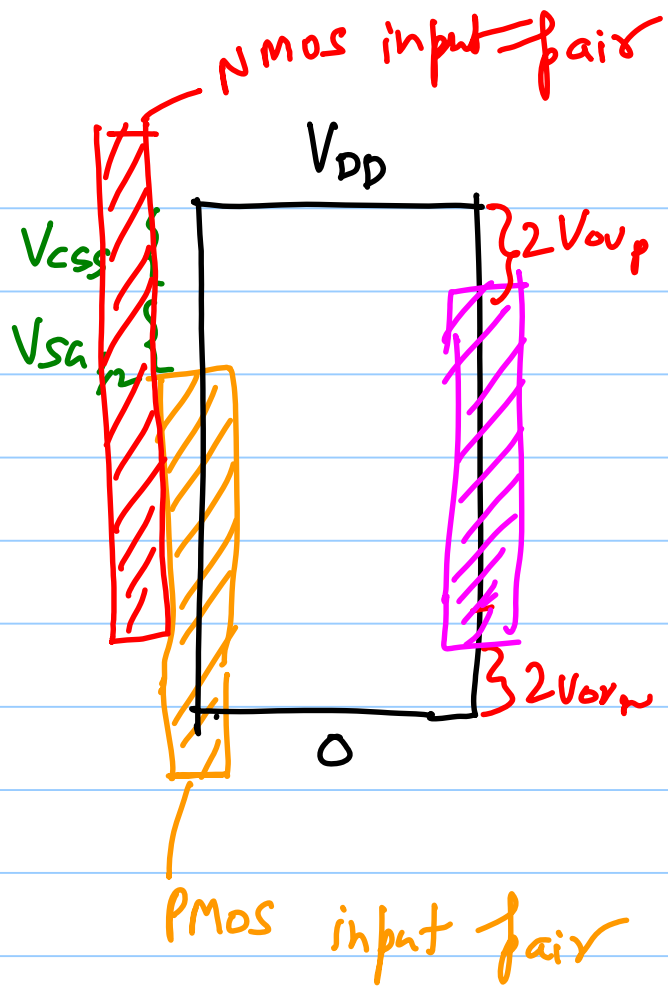
can go below the GND rail

$$V_{in,min} \leq V_{DD} - V_{CSS} - V_{SG,1/2}$$



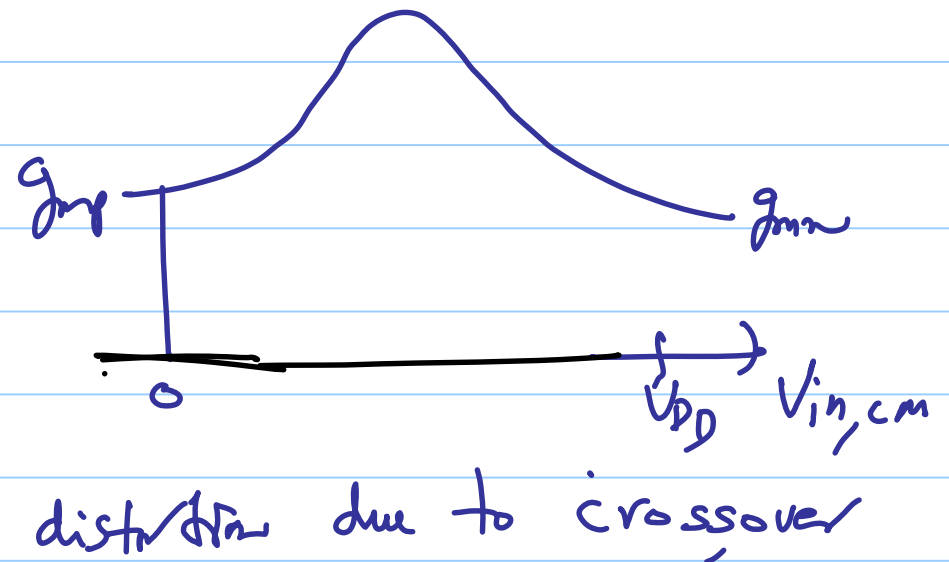
(-) consumes more (2x) bias current

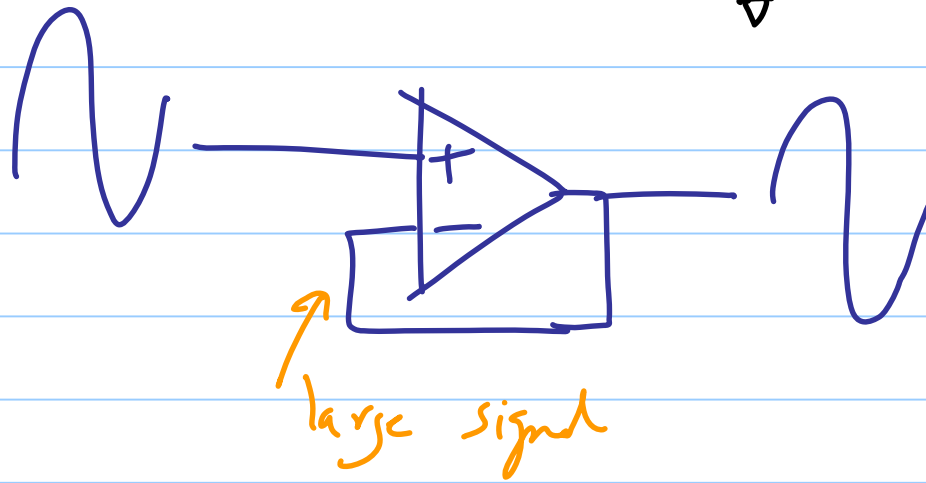
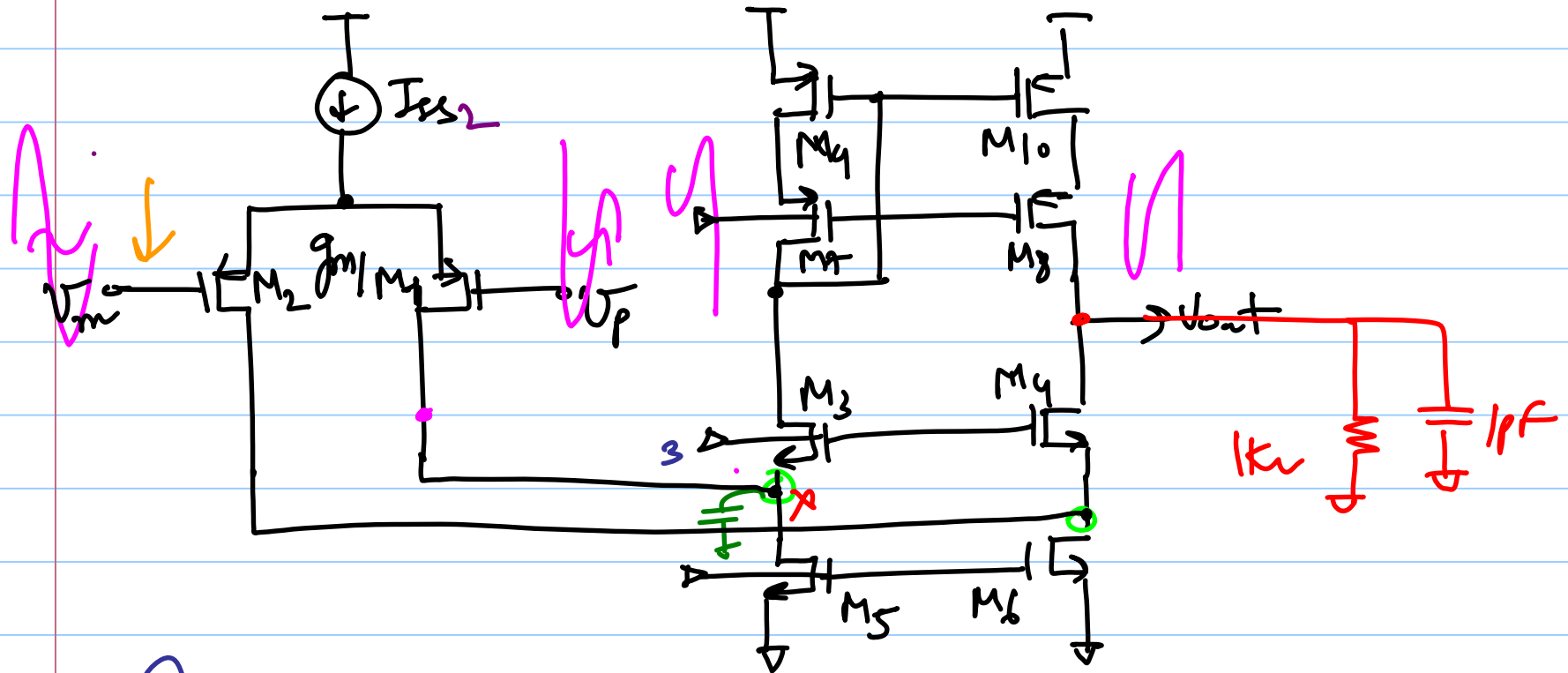




rail-to-rail
input swing

$$G_{m,tot} = g_{m,n} + g_{m,p}$$

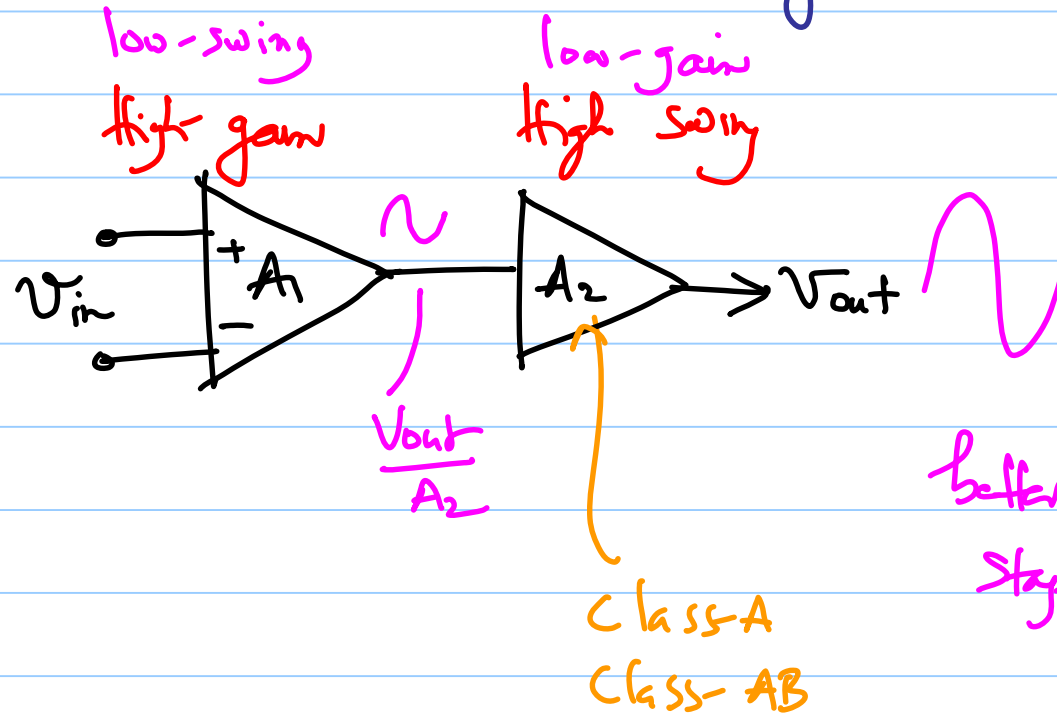




more non linear
behavior

Two-stage Opamp:

2nd stage isolates gain & swing requirements



better linearity as first stage output swing is small.

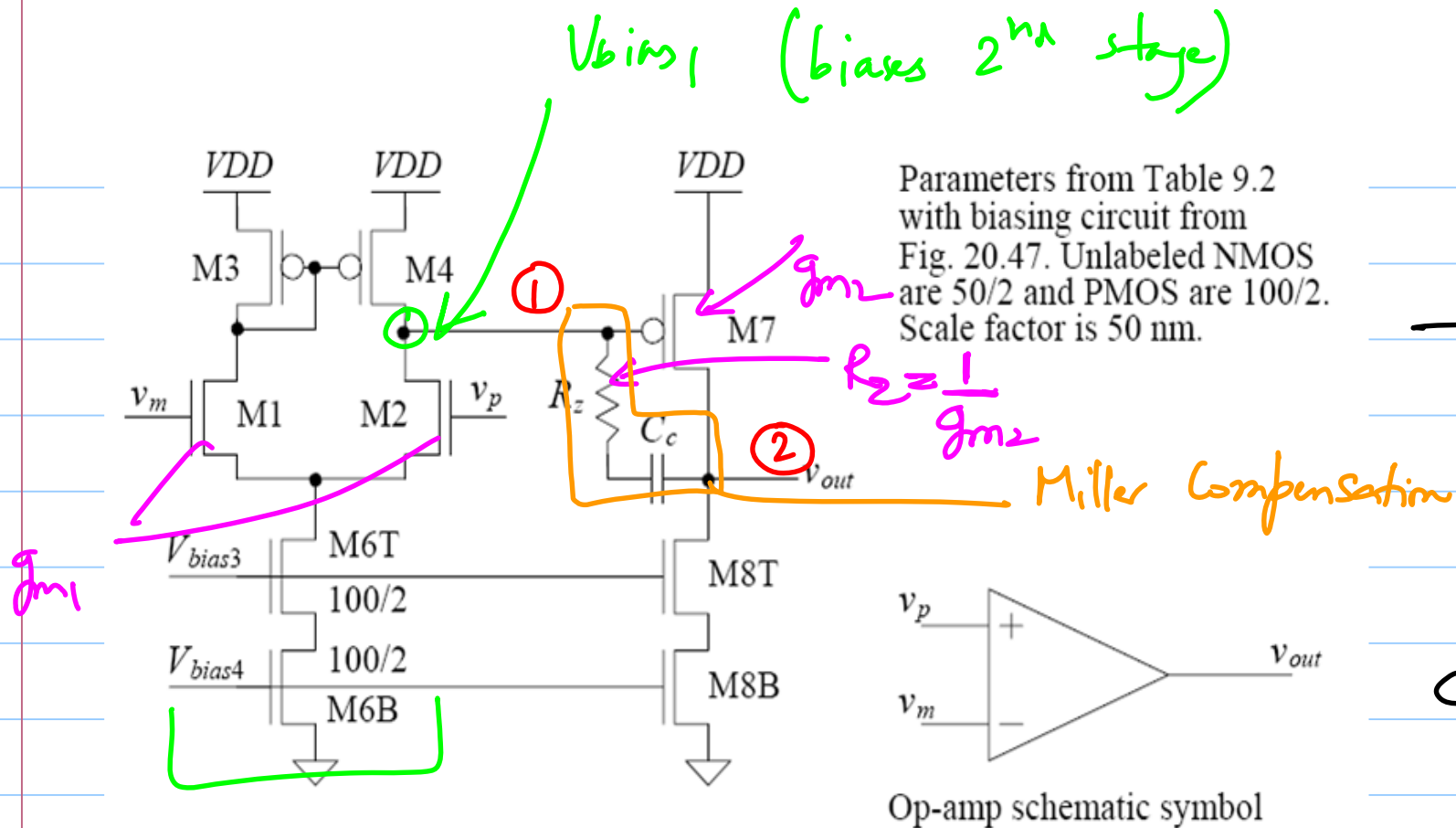
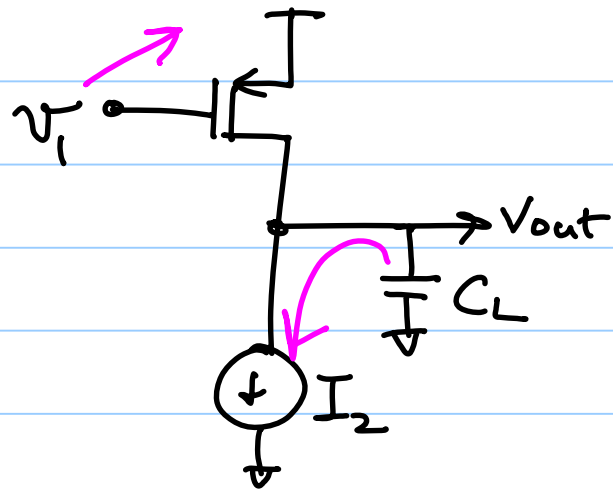
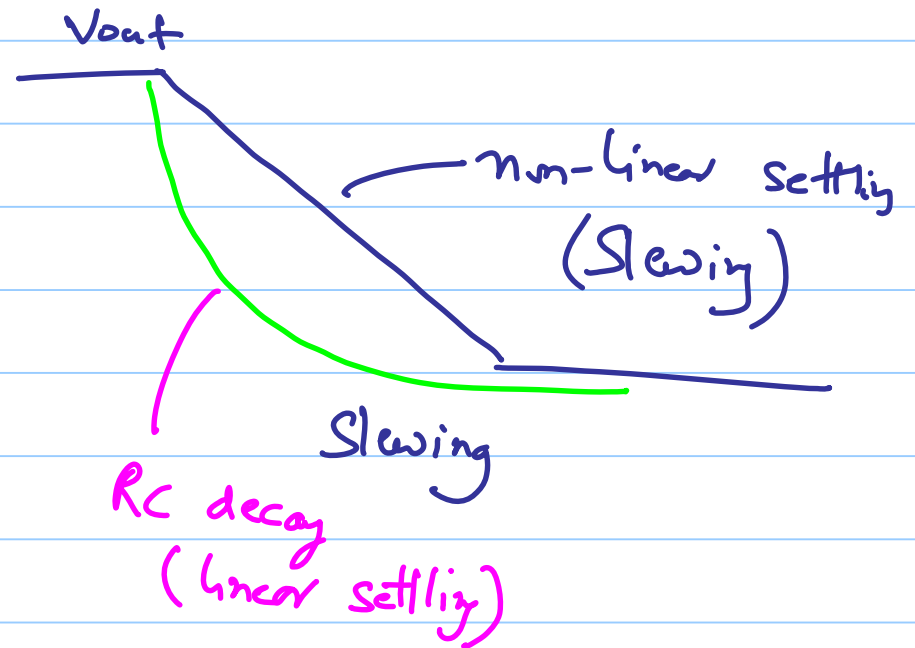


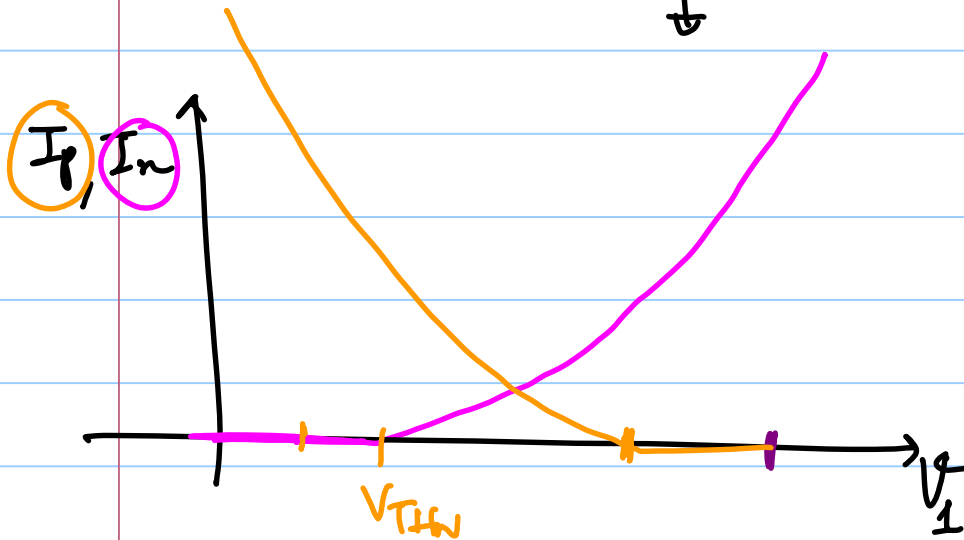
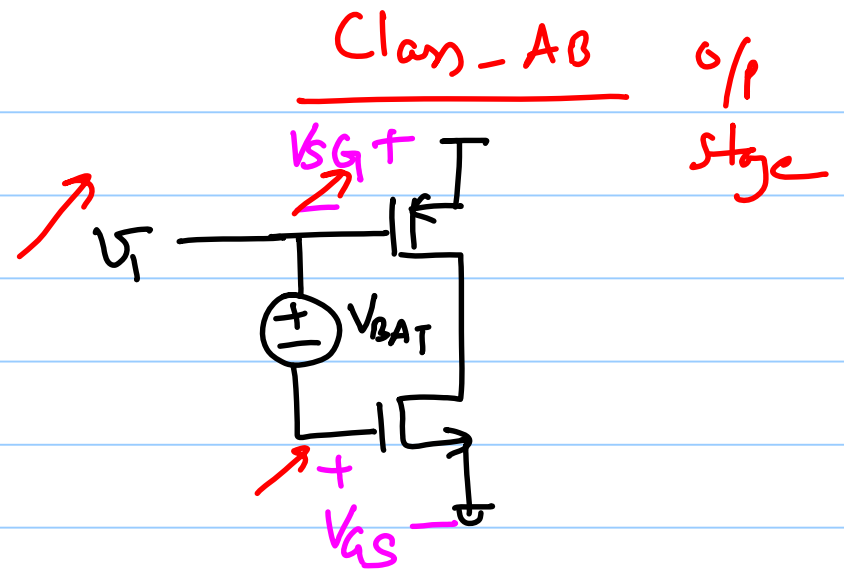
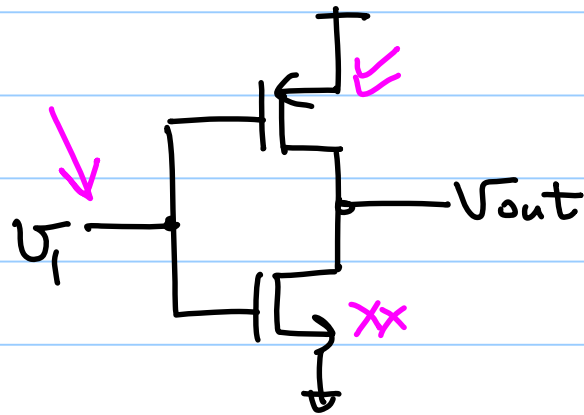
Figure 24.2 Basic two-stage op-amp.

Class-A stage

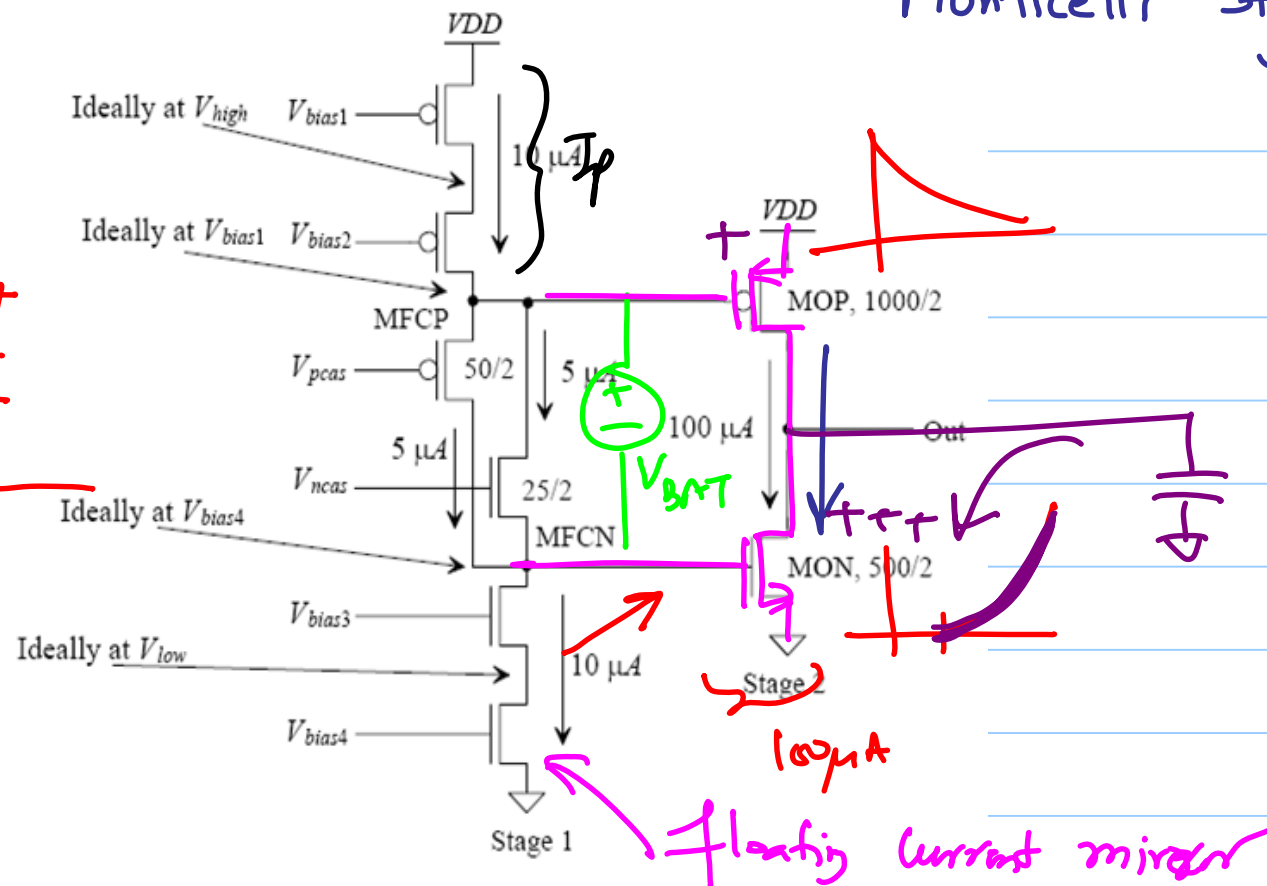
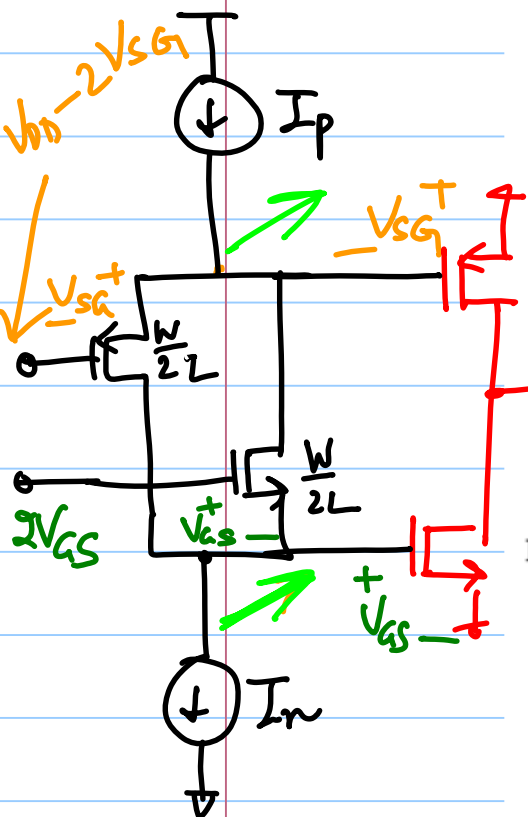


$$\frac{dV_{out}}{dt} = \frac{I_2}{C_L}$$





"Monticelli Stage"



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2). Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 20.49 Biasing with a floating current source.

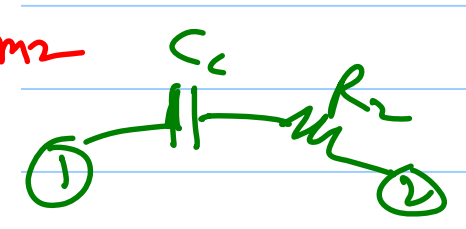
Biasing from Fig. 20.47.
 Sizes given in Table 9.2.

The diagram shows a differential amplifier with cascode stages. The PMOS network consists of M1, M2, M9, and M10. The NMOS network consists of M3, M4, M11, and M12. Biasing is provided by V_{bias1} , V_{bias2} , V_{bias3} , and V_{bias4} . Cascode stages are formed by M5, M6, M7, and M8. Handwritten annotations include red circles around M1 and M2, a red 'In' at the bottom, and green and red annotations on the right side including a green line, a red line, and a green 'C' with a red 'R'.

Folded Cascode

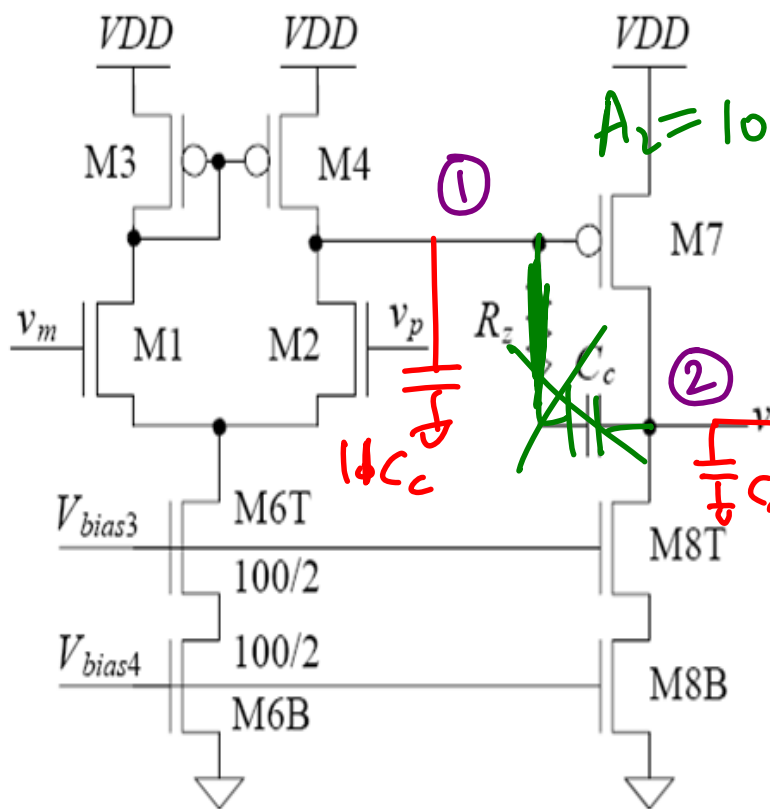
Embedded Current mirrors

Clam-AB o/p style
Buffer



$$W_{P2} \propto \frac{g_{m2}}{C_L}$$

Figure 24.44 Folded-cascode op-amp with class AB output buffer.



Parameters from Table 9.2
with biasing circuit from
Fig. 20.47. Unlabeled NMOS
are 50/2 and PMOS are 100/2.
Scale factor is 50 nm.

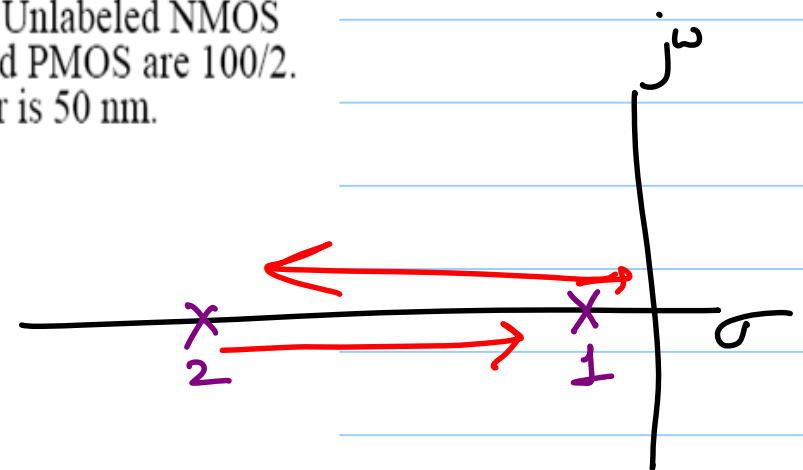
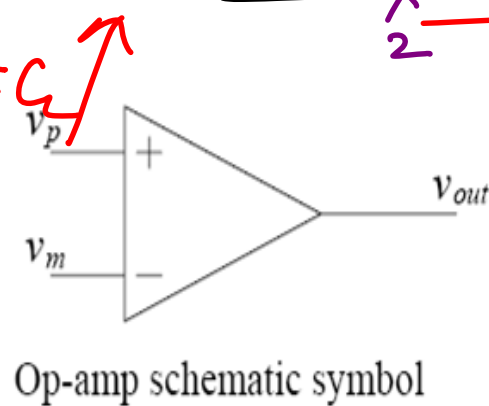
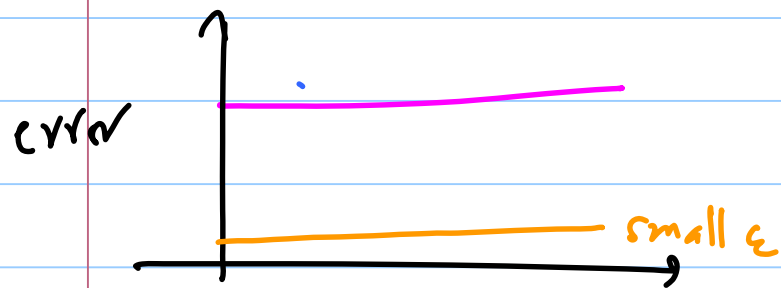
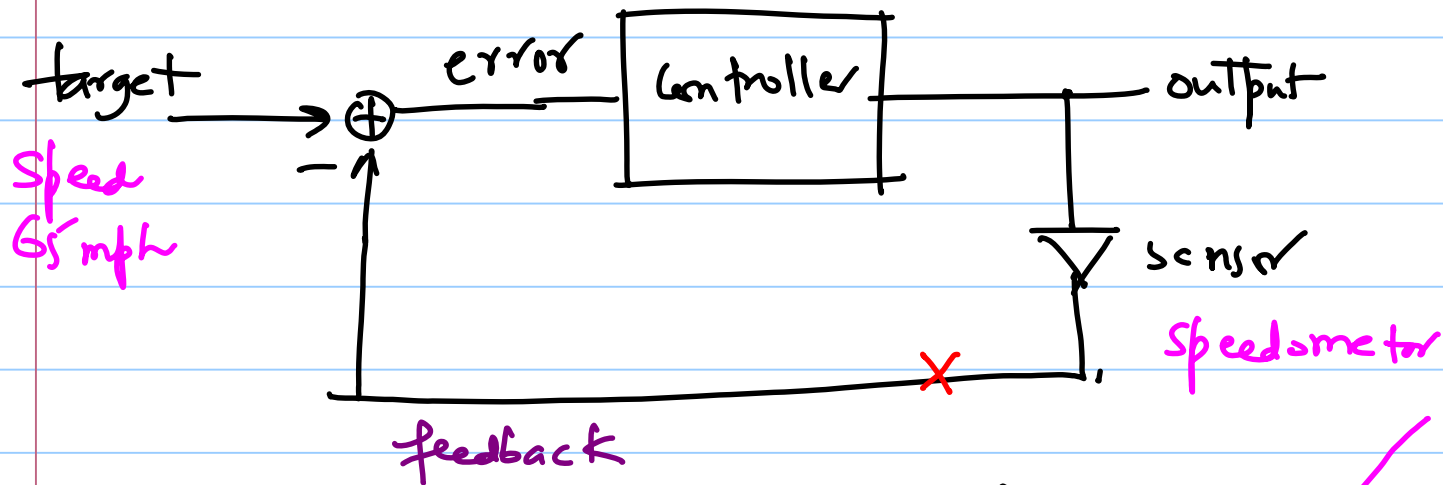


Figure 24.2 Basic two-stage op-amp.

Negative feedback loops :



an integrator as the controller

