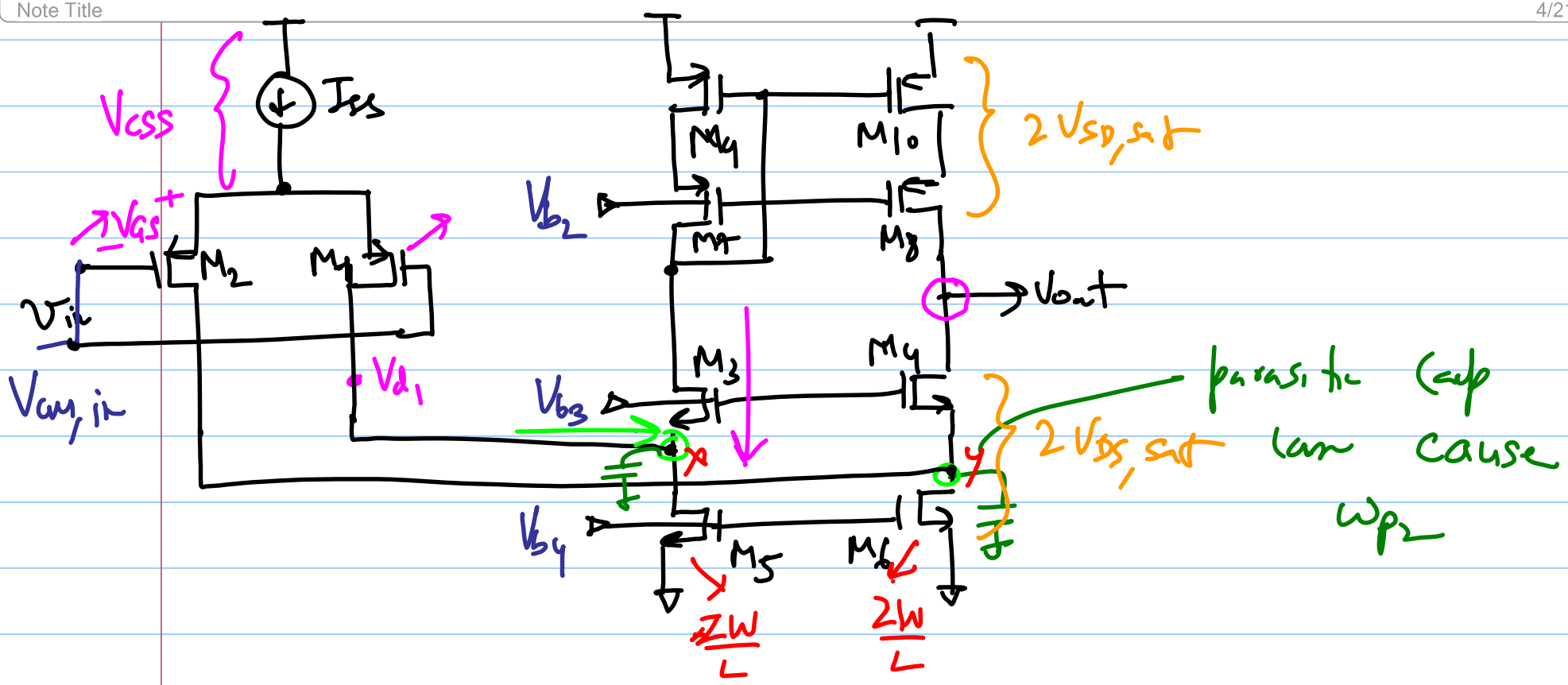
ECE 511 – Lecture 24

Note Title 4/21/2015

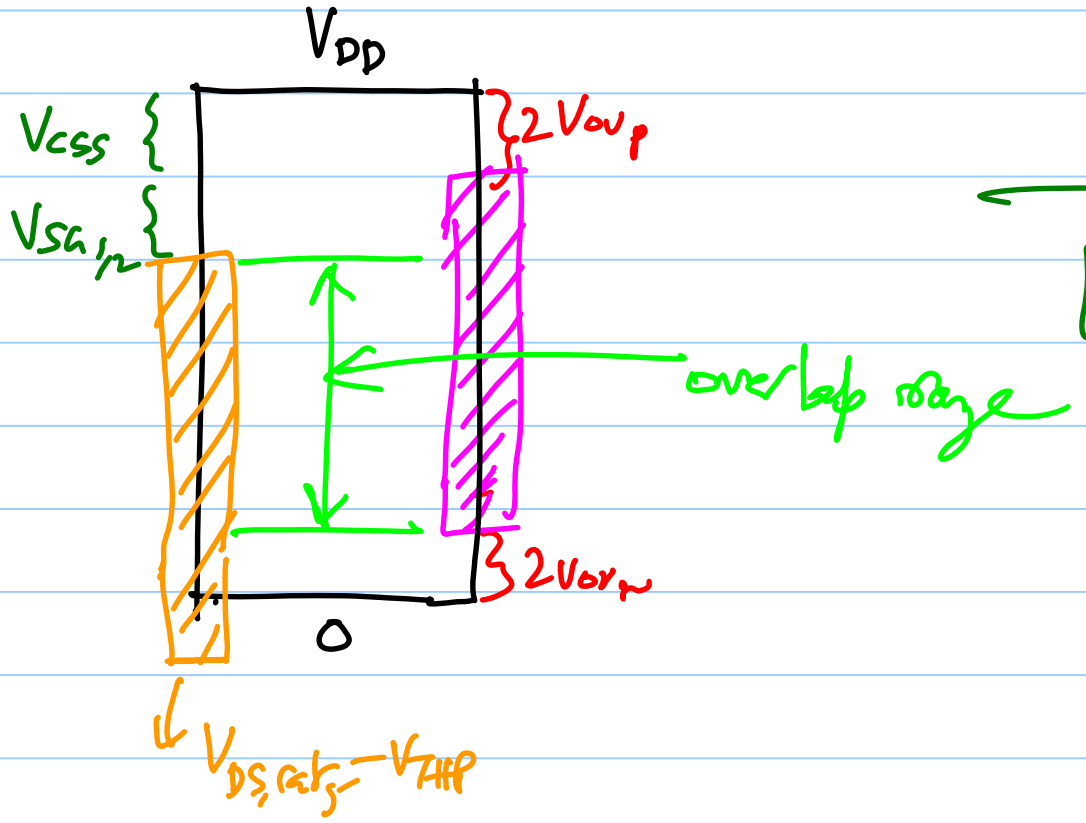


$V_{CM,in} = V_{G1} > V_{D1} - V_{THP}$ & $V_{D1} \geq V_{DS,sat5}$

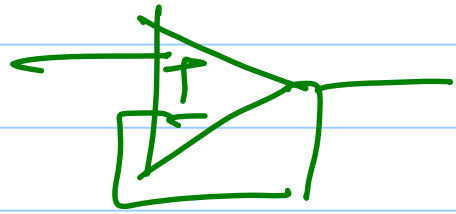
$$\boxed{V_{CM,in} \geq V_{DS,sat5} - V_{THP}} < 0$$

Can go below the GND rail

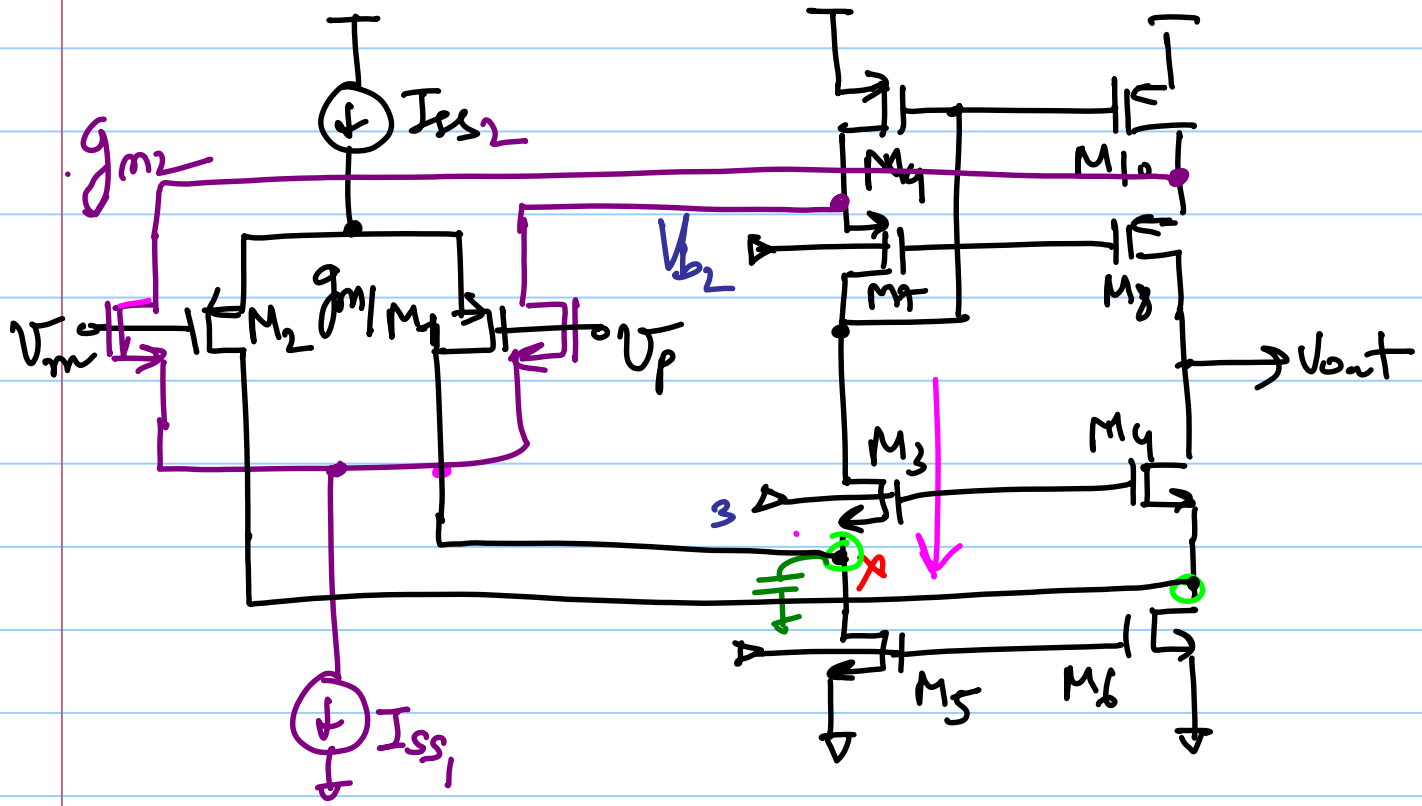
$$V_{CM,in} \leq V_{DD} - V_{CSS} - V_{SG1,2}$$

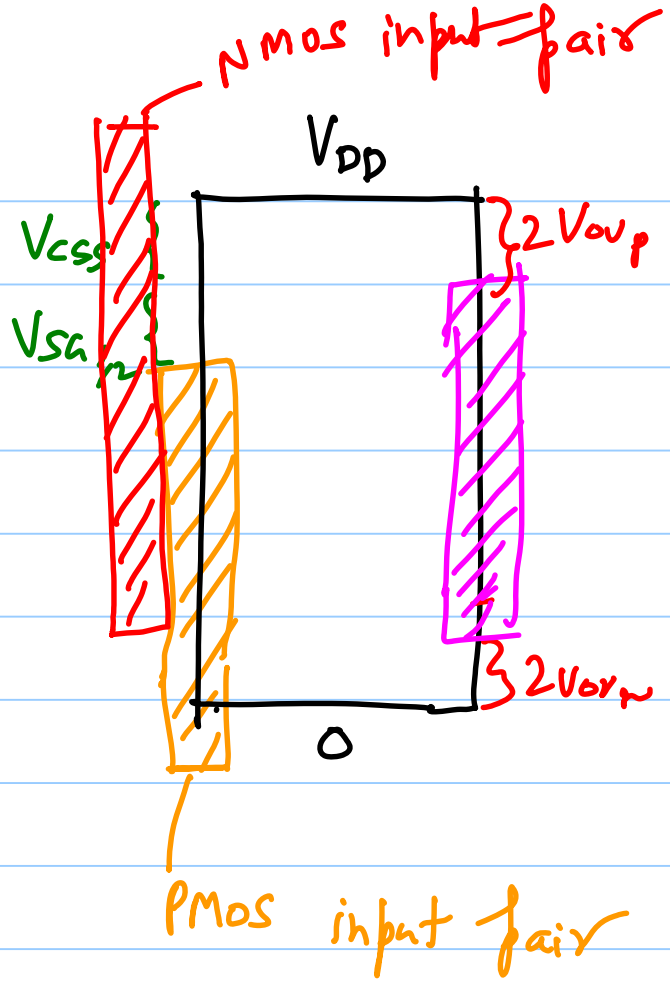


$V_{ov} \triangleq V_{SD,sat}$



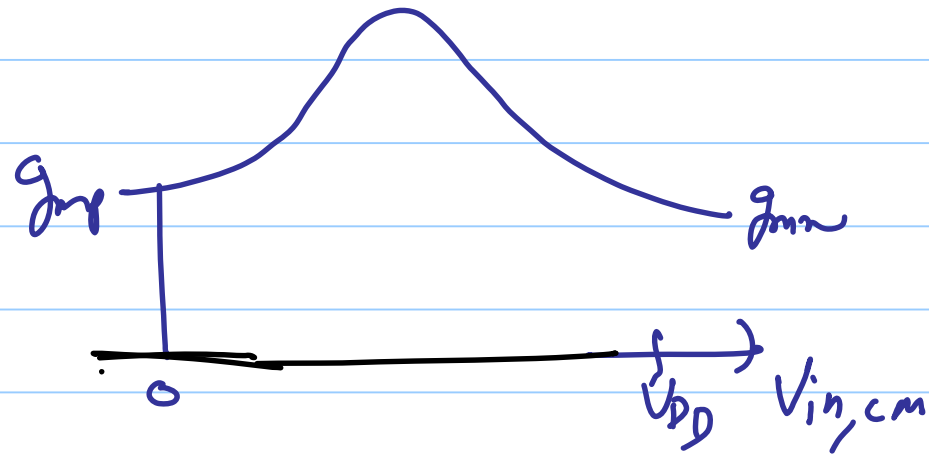
(–) Consumes more (2×) bias current


I_{SS_2}
g_{m_2}
V_{b_2}
M_9
M_{10}
M_7
M_8
V_{out}
V_m
M_2
g_{m_1}
M_1
V_p
M_3
M_4
3
X
M_5
M_6
I_{SS_1}

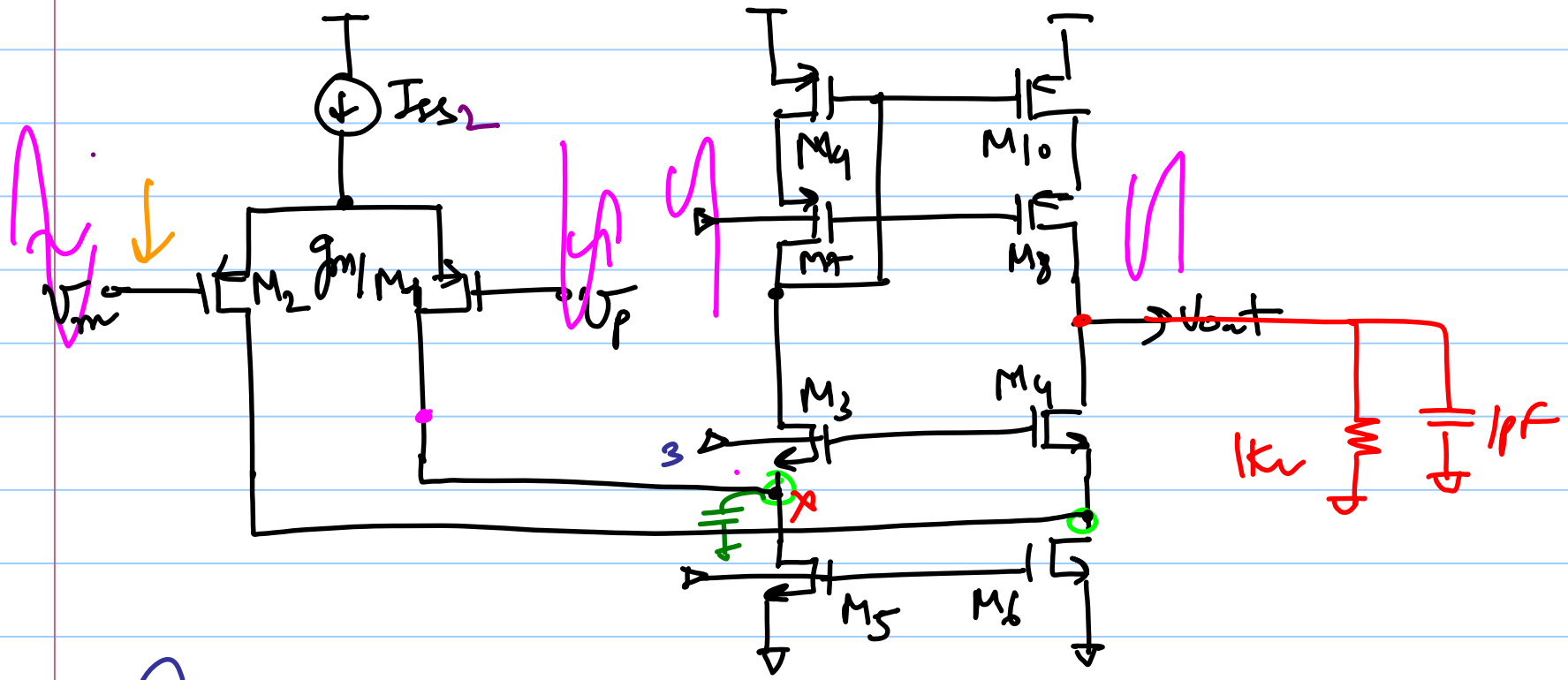


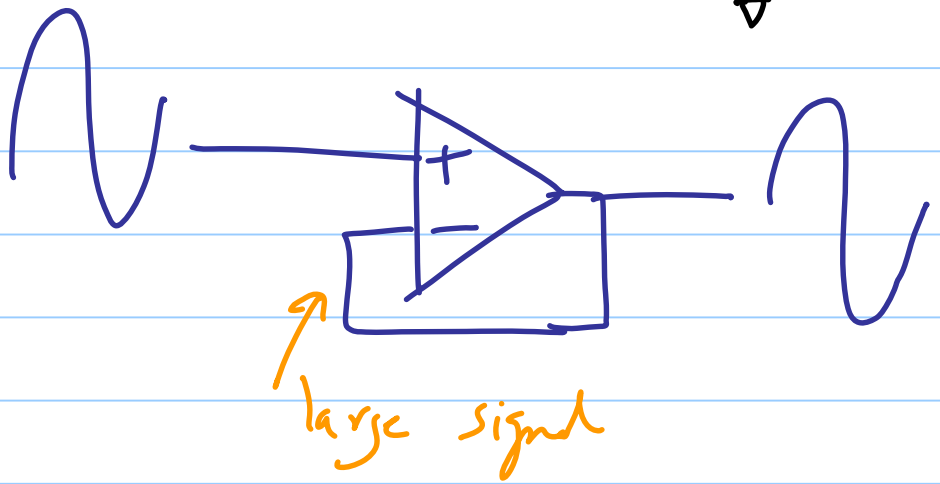
rail-to-rail input swing

$$G_{m,tot} = g_{mn} + g_{mp}$$



distortion due to crossover

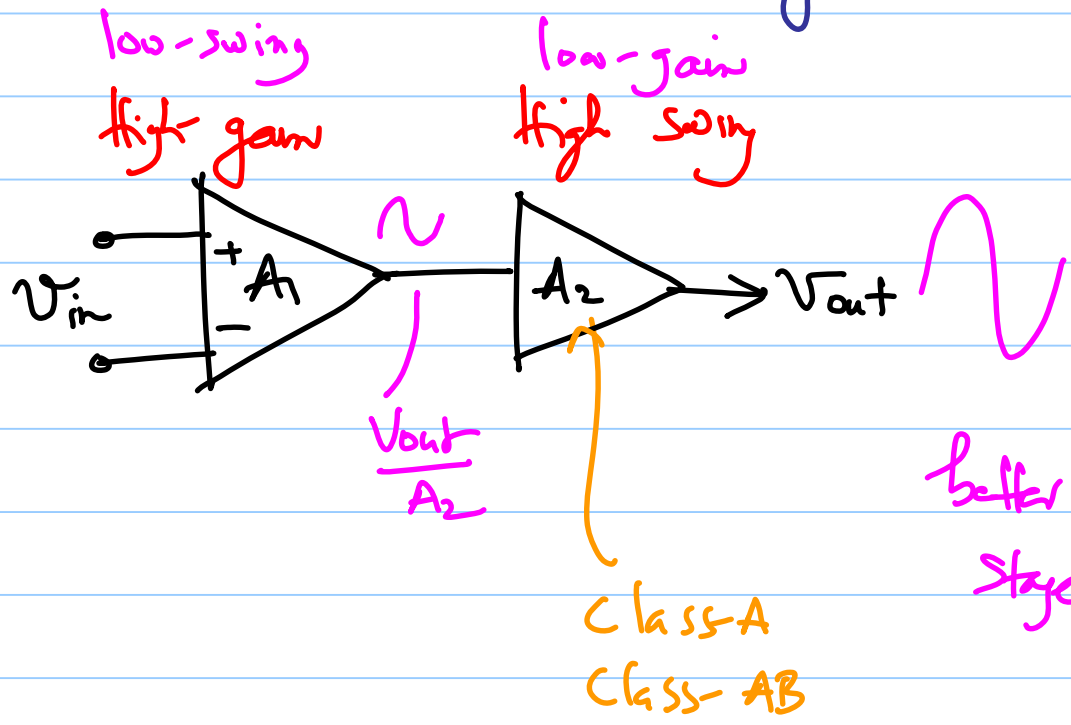




more non linear behavior

Two-stage Opamp:

2nd stage isolates gain & swing requirements



better linearity as first stage output swing is small.

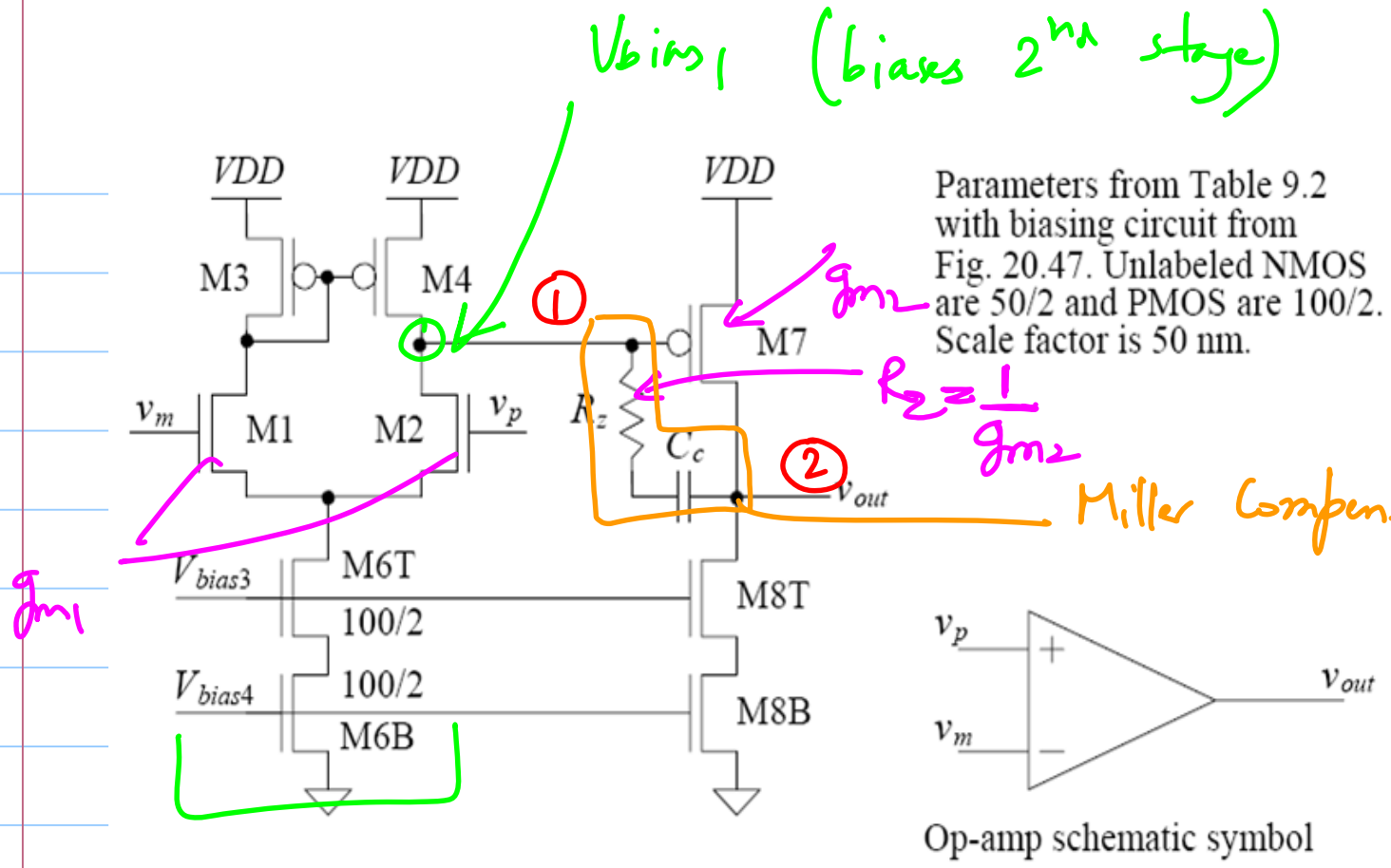
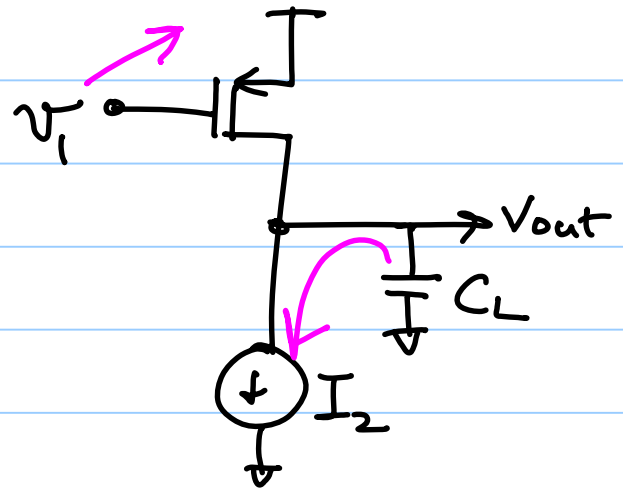
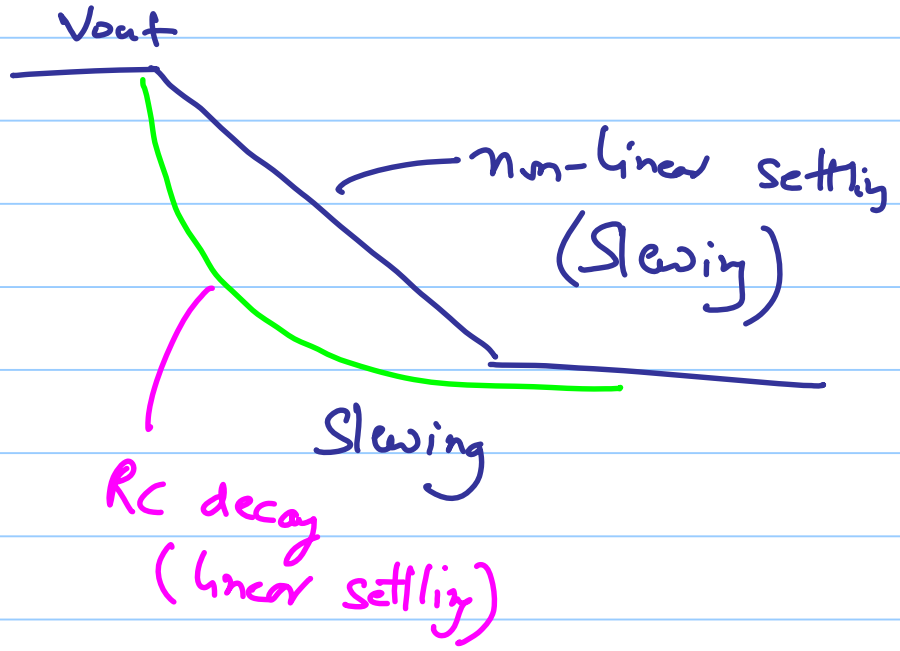


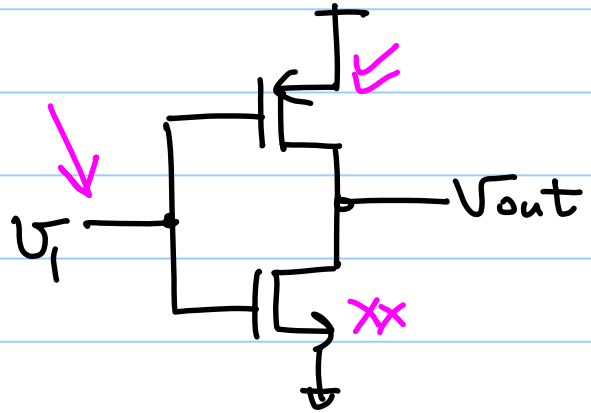
Figure 24.2 Basic two-stage op-amp.

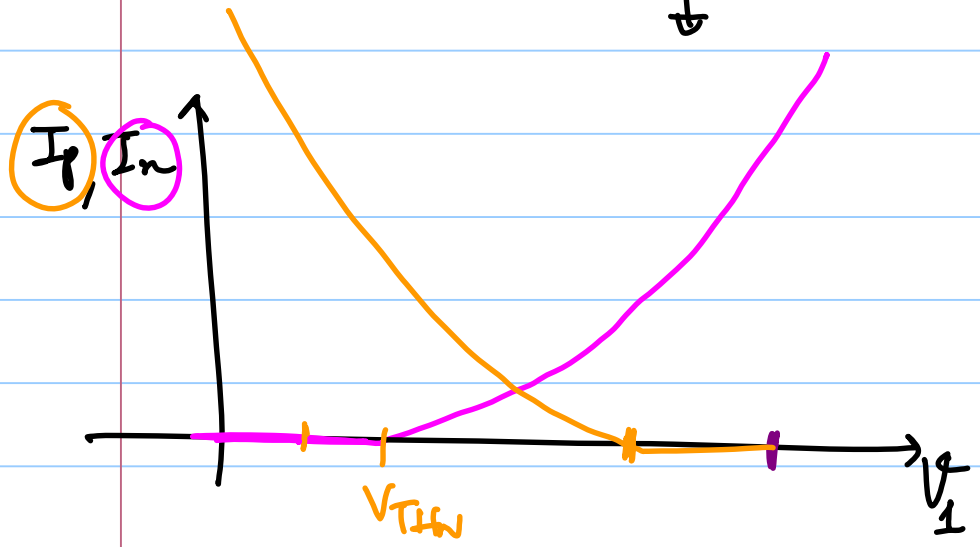
Class-A stage



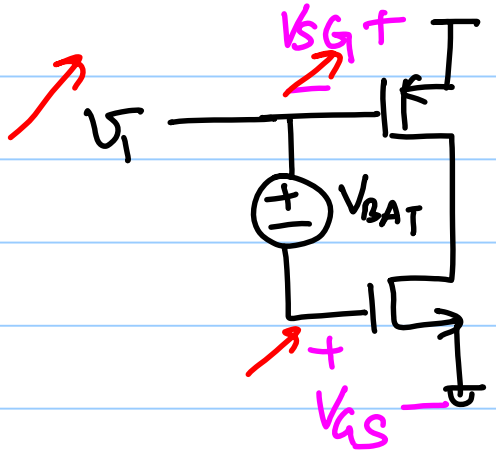
$$\frac{dV_{out}}{dt} = \frac{I_2}{C_L}$$



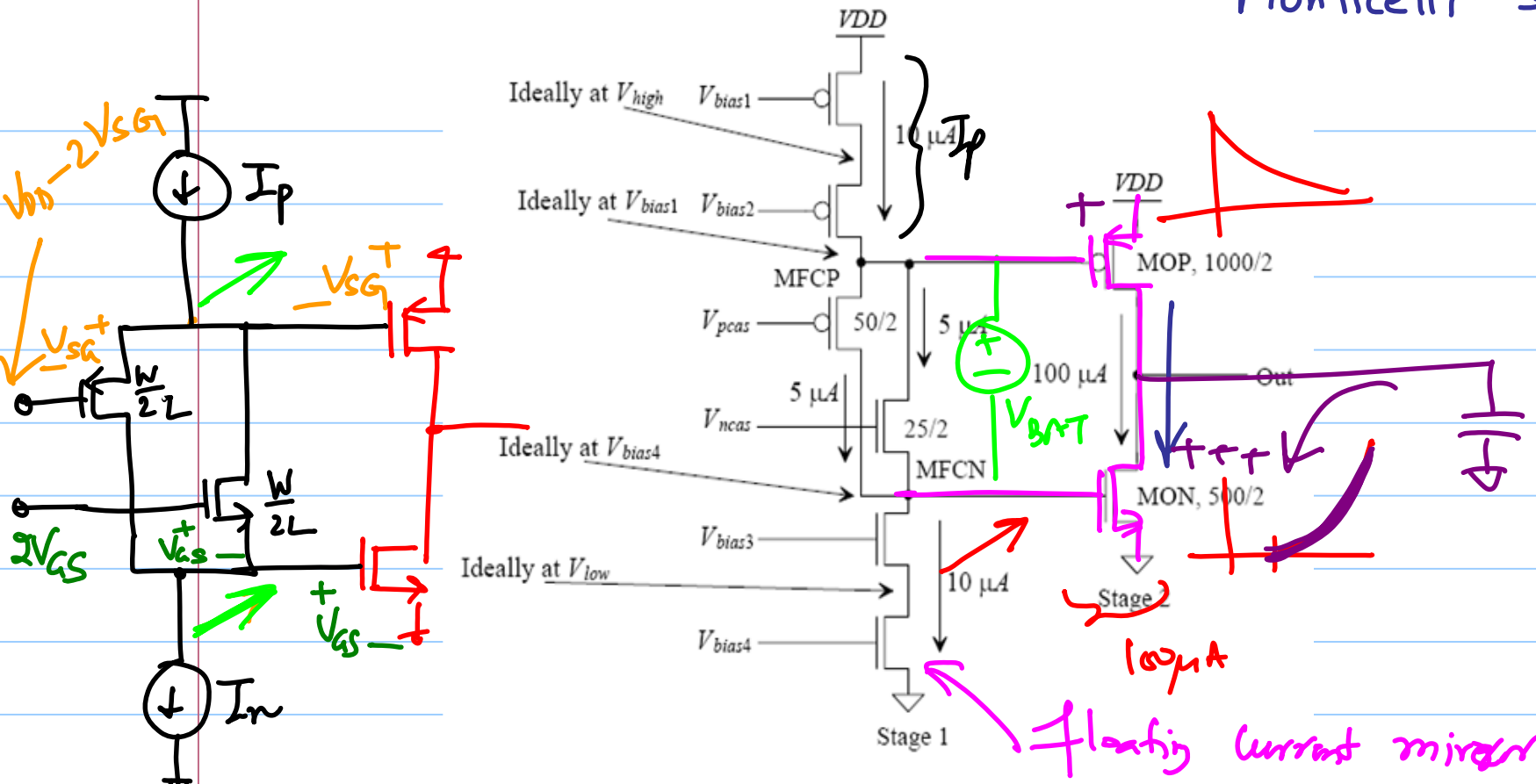




Class-AB o/p Stage



"Monticelli Style"



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2).
Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 20.49 Biasing with a floating current source.

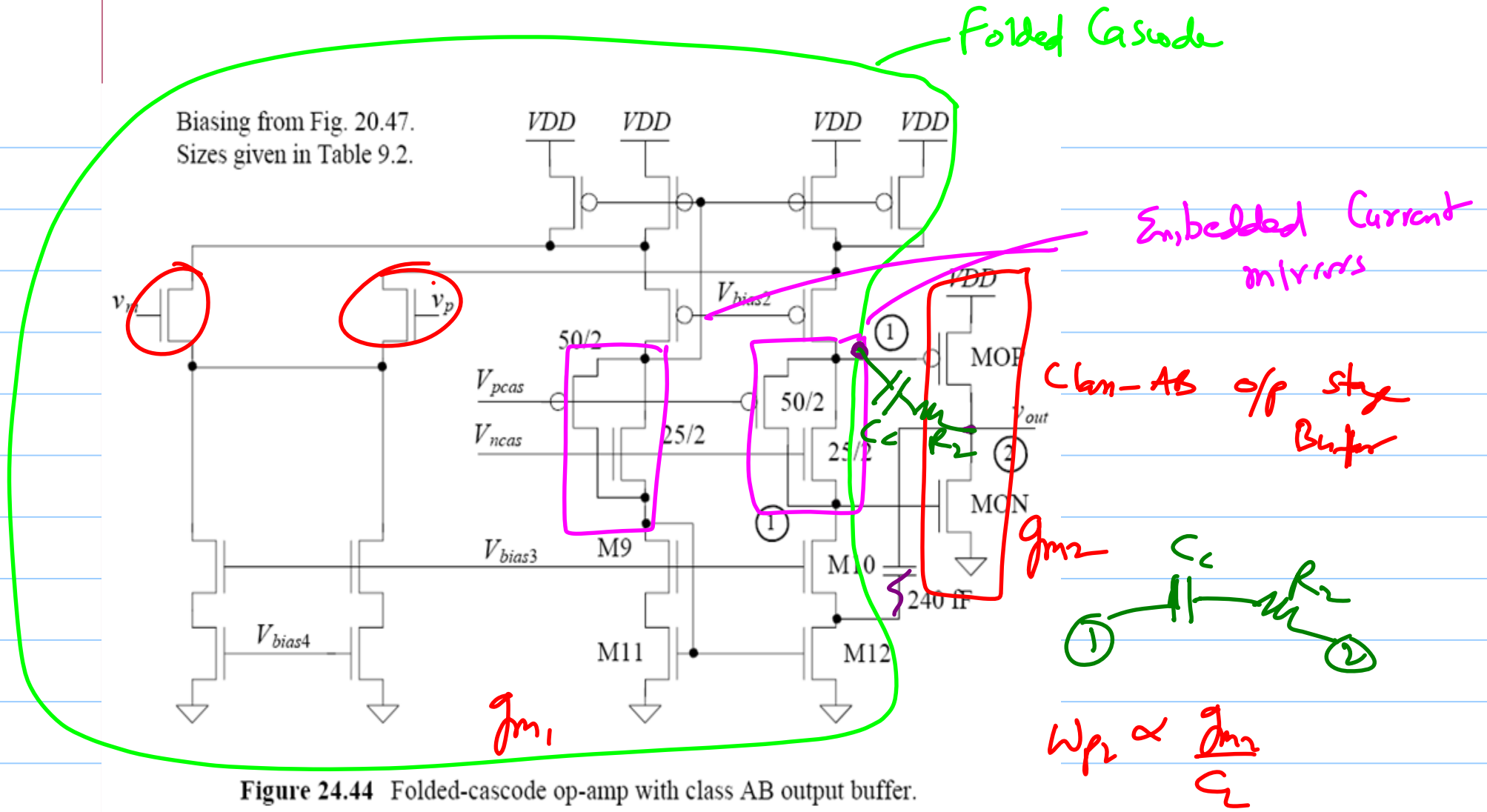
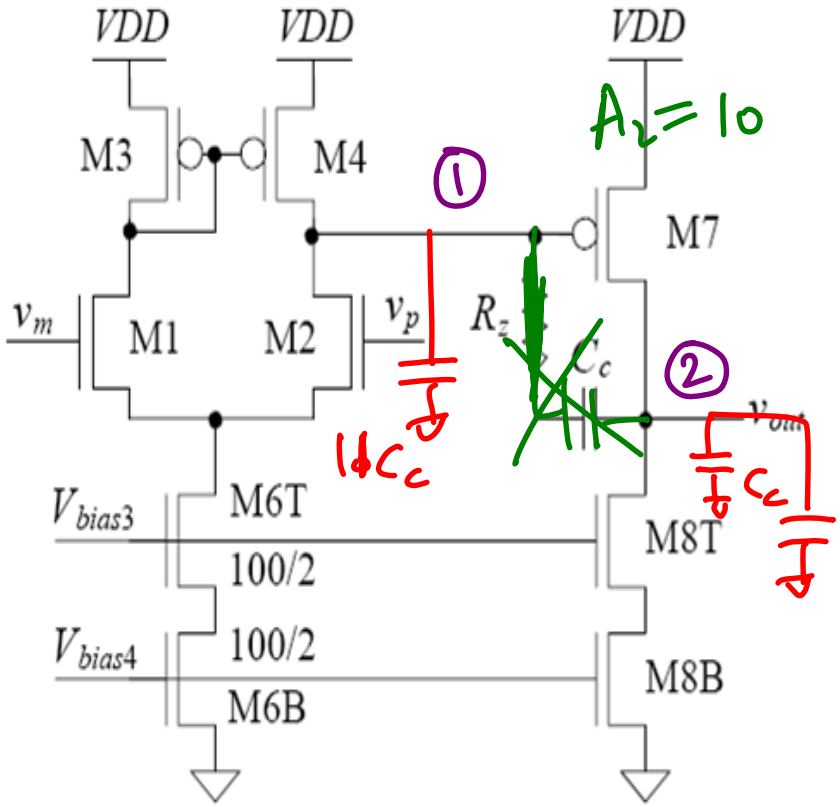
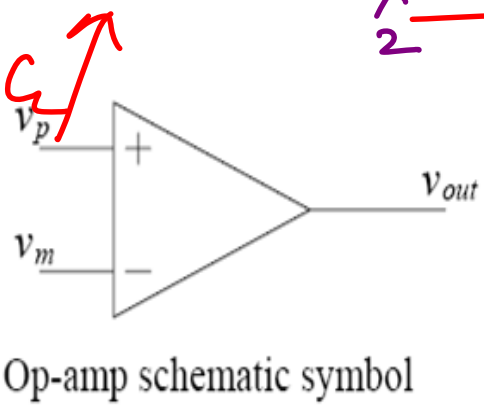


Figure 24.44 Folded-cascode op-amp with class AB output buffer.



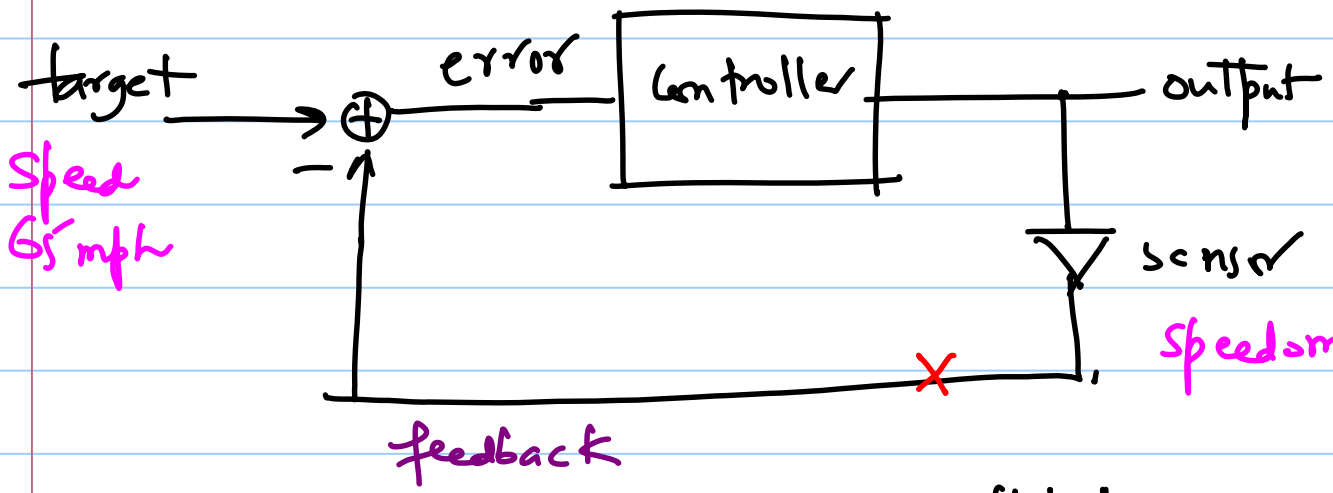
Parameters from Table 9.2 with biasing circuit from Fig. 20.47. Unlabeled NMOS are 50/2 and PMOS are 100/2. Scale factor is 50 nm.

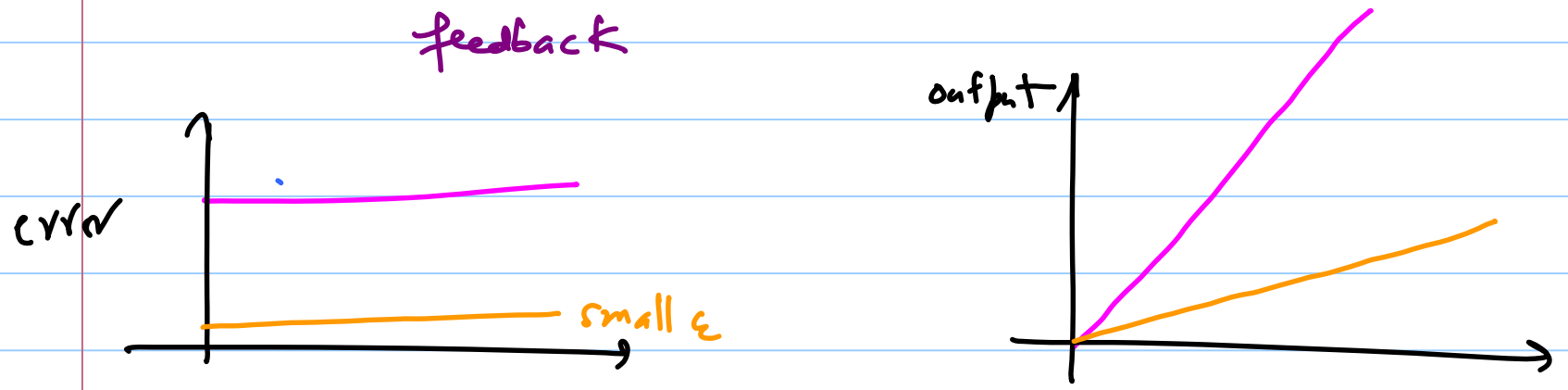


Op-amp schematic symbol

Figure 24.2 Basic two-stage op-amp.

Negative feedback loops:





an integrator as the controller