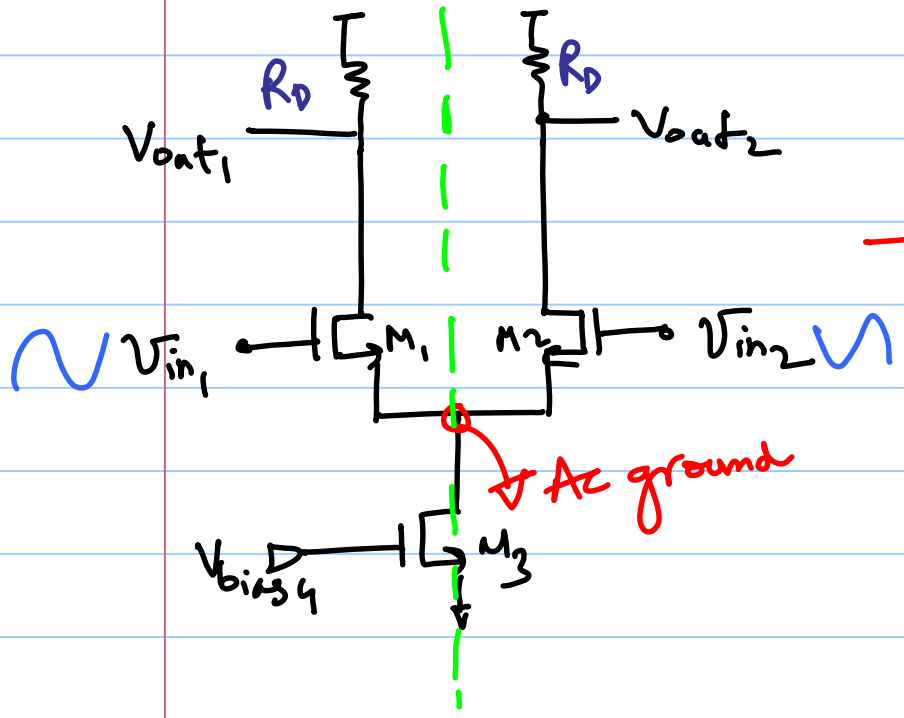
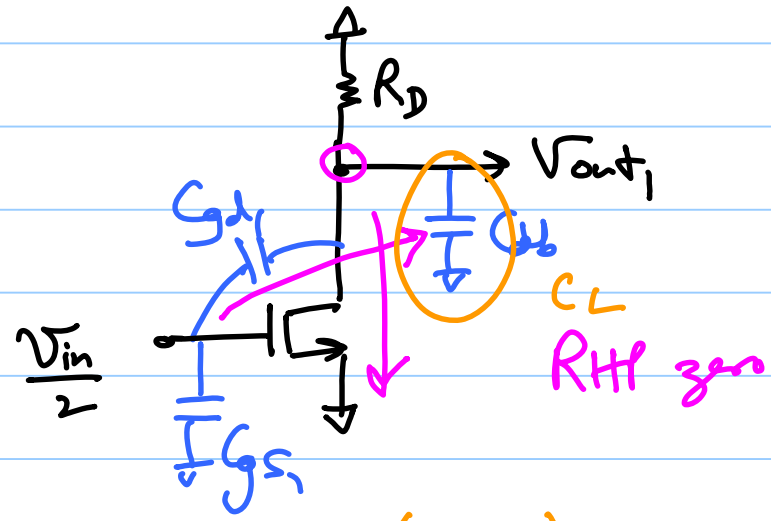
ECE 511 – Lecture 23

Note Title 4/16/2015

Differential Circuit Analysis



DM half Circuit



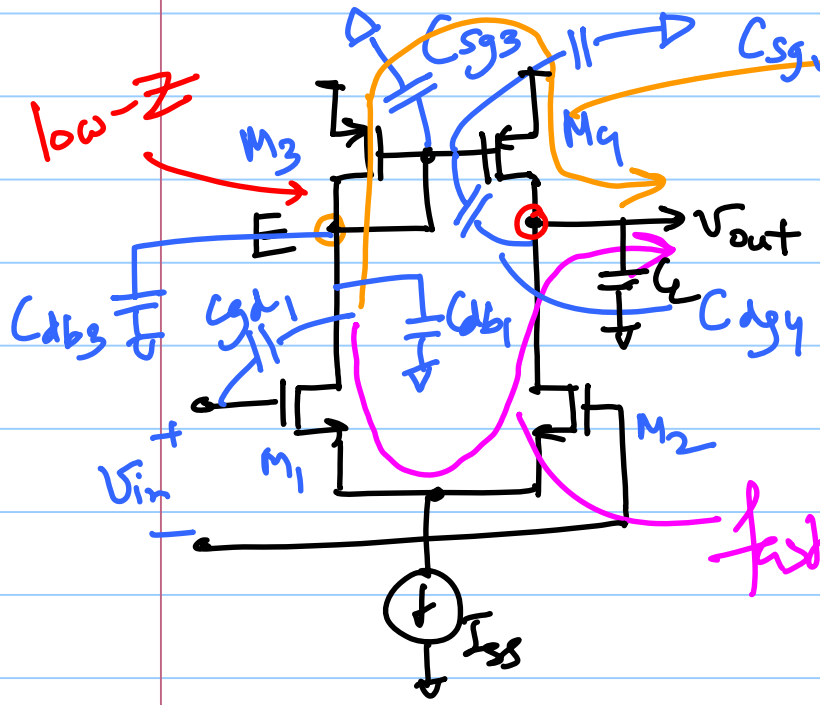
$$\frac{V_{out}}{V_{in}}(s) = -\frac{A_{v_0}\left(1 - s/\omega_z\right)}{\left(1 + s/\omega_{p_1}\right)}$$

$A_{v_0} = g_m(R_D \| r_o)$

$\omega_z = \frac{g_m}{C_{gd}}$ @ RHP

$\omega_{p_1} = \frac{1}{(r_o \| R_D) C_L}$

1st-order



Topology contains 2 signal paths to the o/p with different transfer functions

path thru $M_3 - M_4 \Rightarrow$ pole at node E

Mirror pole

$$\omega_{p2} \simeq \frac{g_{m3}}{C_E}$$

$$C_E = C_{gs_3} + C_{g_{s_4}} + C_{db_3} + C_{db_1}$$
+ Miller contributions from C_{gd_1} & C_{gd_4}

Both signal paths contain a pole at the output node ①

↳ & the slow path contains an extra pole at (E)

Skipping Algebra:

$$\omega_{p1} \approx \frac{1}{(r_{on} \| r_{op}) C_L}$$

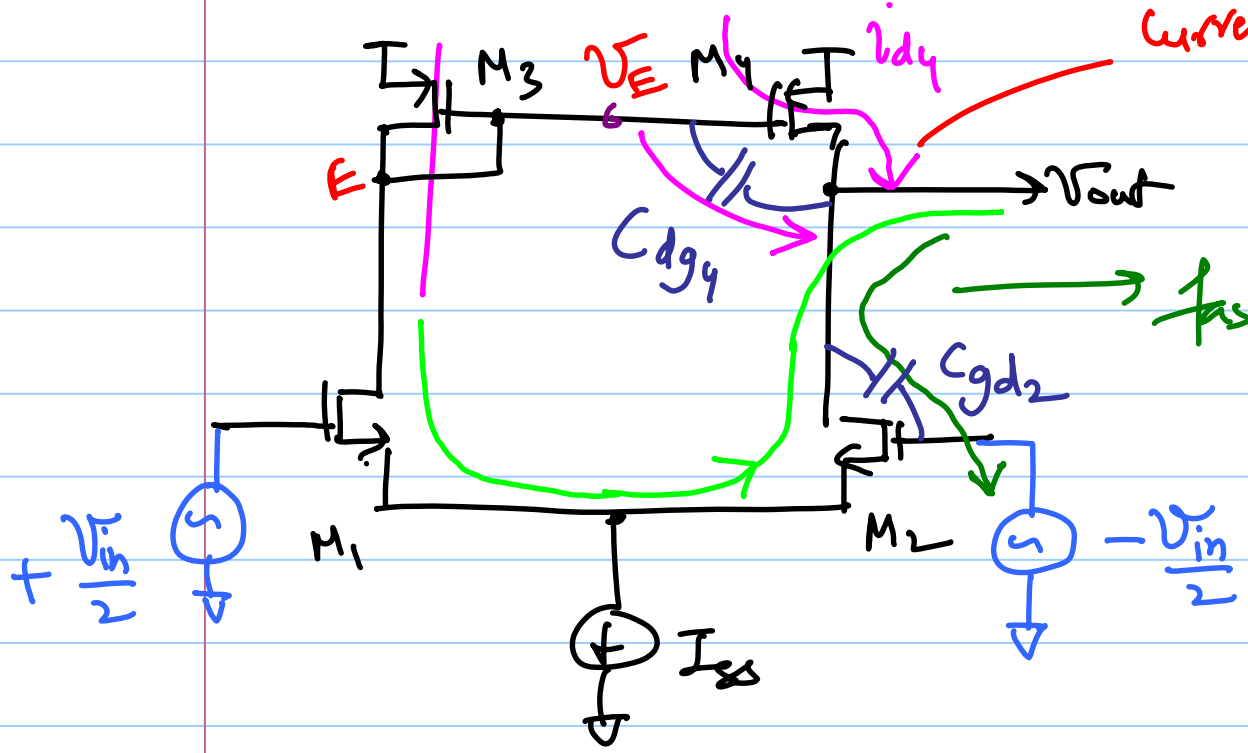
$$\omega_{p2} \approx \frac{g_{mp}}{C_E}$$

$$\omega_{z2} = \frac{g_{mn}}{C_{gdn}} \quad (@ \text{RHP})$$

$$\omega_{z1} = -\frac{2 g_{mp}}{C_E}$$

@ LHP

interesting!



Currents add with the same polarity
⇒ LHP zero!

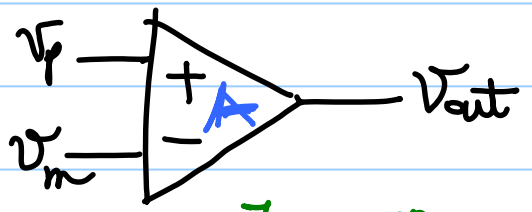
→ fast path: Currents add with opposite polarity
⇒ RHP zero

$\frac{g_{m2}}{C_{gd2}}$

Operational Amplifiers (opamps)

$v_{out} = A(v_p - v_m)$

Opamp : high-gain VCVS

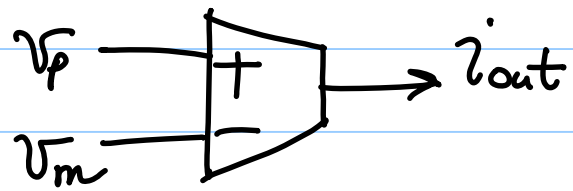


$Z_{in} \to \infty$

$Z_{out} \to 0$

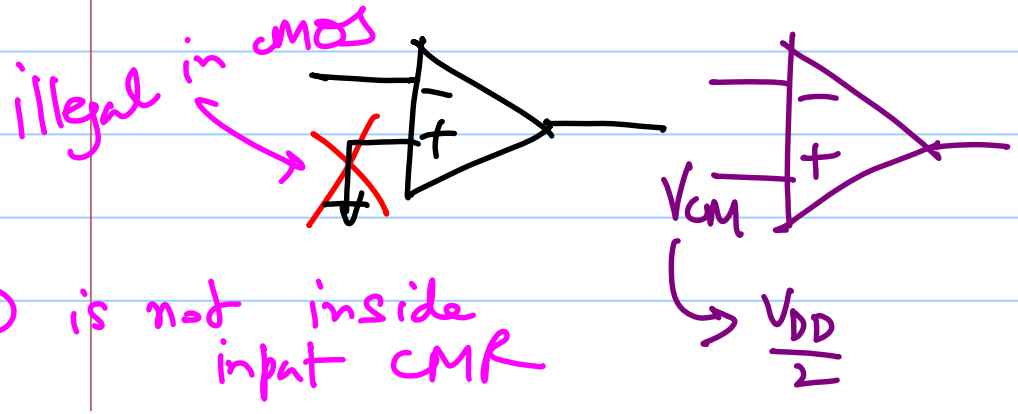
OTA : VCCS with large G_m

Op. transconductance amplifier



$i_{out} = G_m(v_p - v_m)$

In CMOS



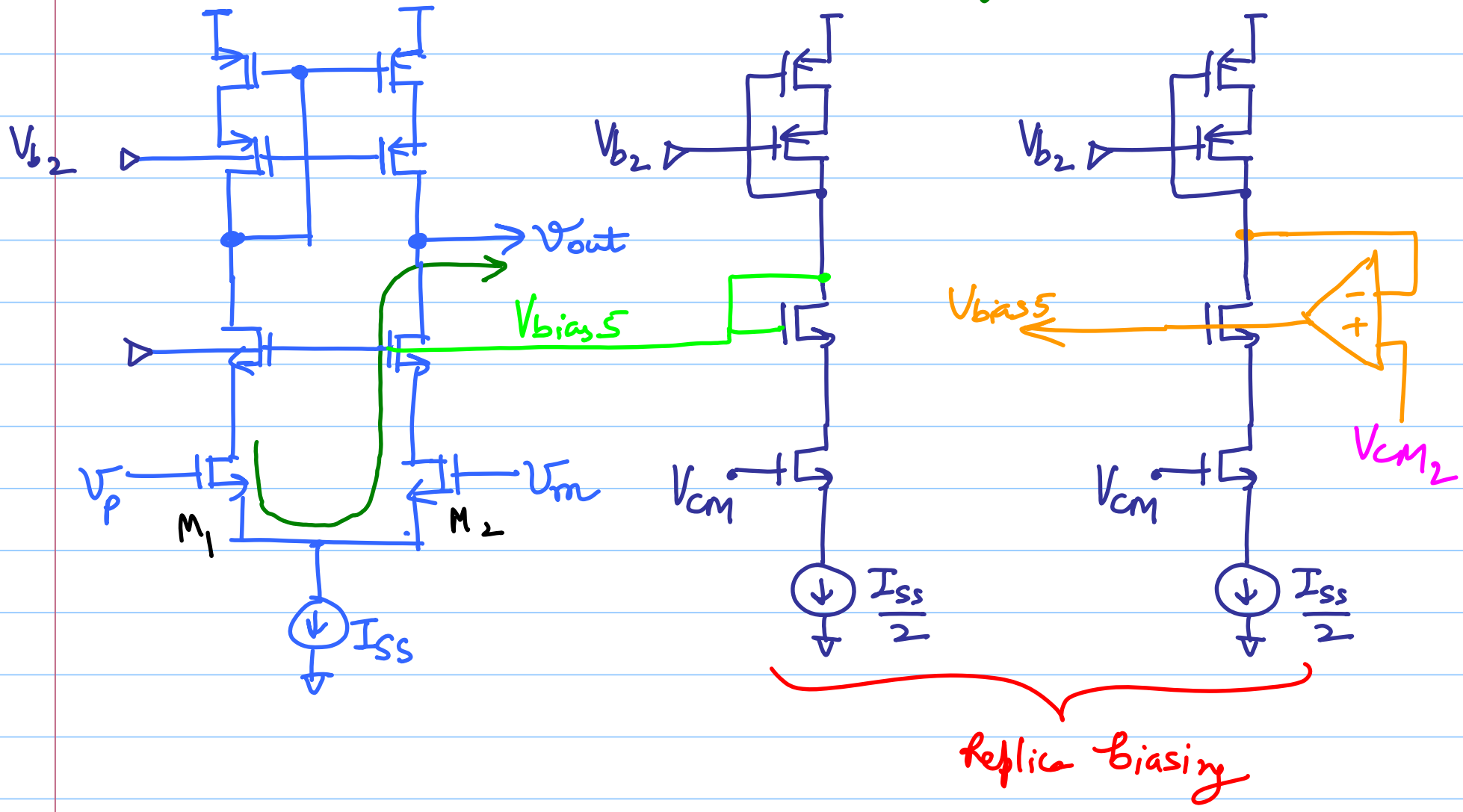
0 is not inside input CMR

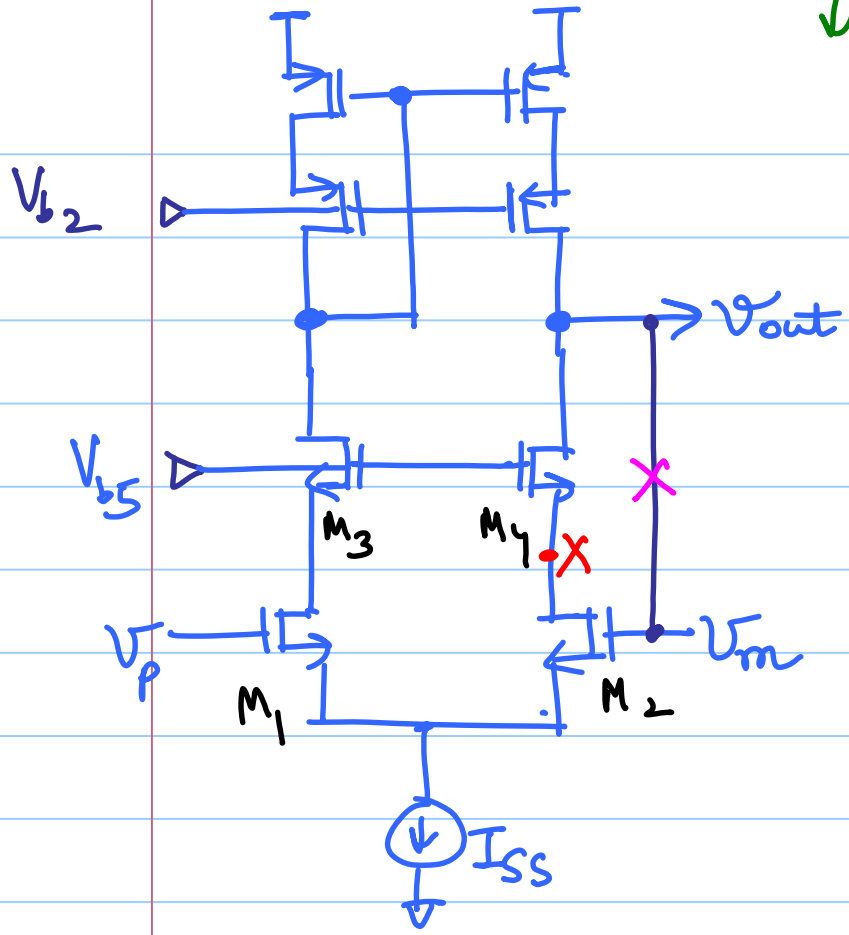
$Z_{in} \to \infty$

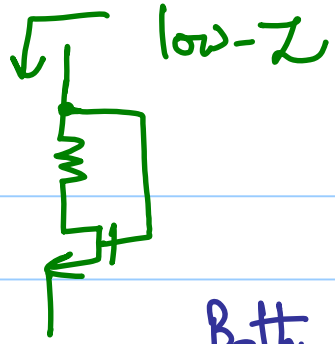
$Z_{out} \to \infty$

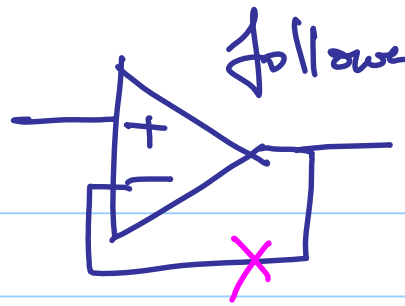
Telescopic Stage

$A_V = g_{mn} \cdot (g_{mp} r_{op}^2 \| g_{mn} r_{on}^2)$









Both M_2 & M_4 must be in SAT.

$v_{out} \le v_x + V_{THN}$: M_2

$v_{out} \ge V_{b5} - V_{THN}$: M_4

also $v_x = V_{b5} - V_{GS4}$

$$\underbrace{V_{b5} - V_{THN}}_{V_{min}} \le v_{out} \le \underbrace{V_{b5} - V_{SG4} + V_{THN}}_{V_{max}}$$

Output range:

$$V_{max} - V_{min} = 2V_{THN} - V_{SG4}$$

$$\simeq V_{THN} - V_{OV4}$$

Very small!

But, we should be able to short input & output to make a UG Buffer

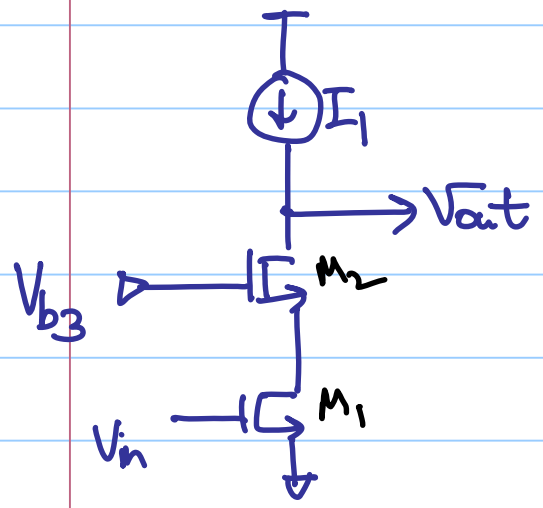
↳ A must in switched-capacitor circuit

Main drawbacks:

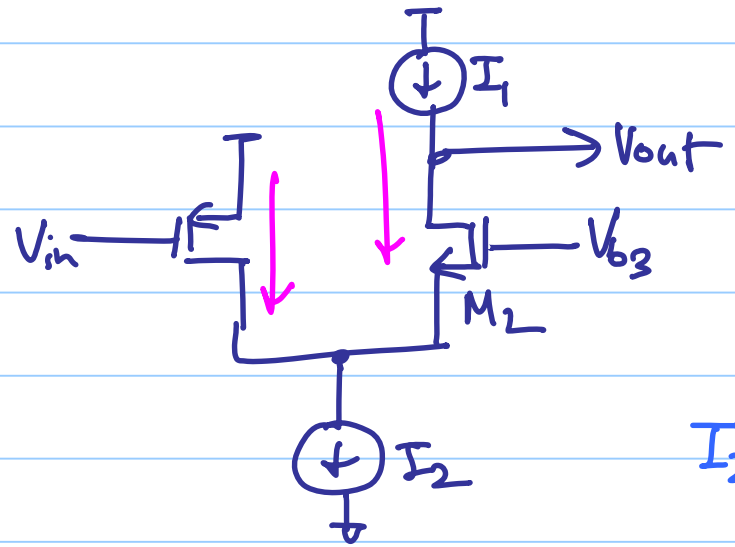
① Limited output swing

② difficulty in shorting Input & output

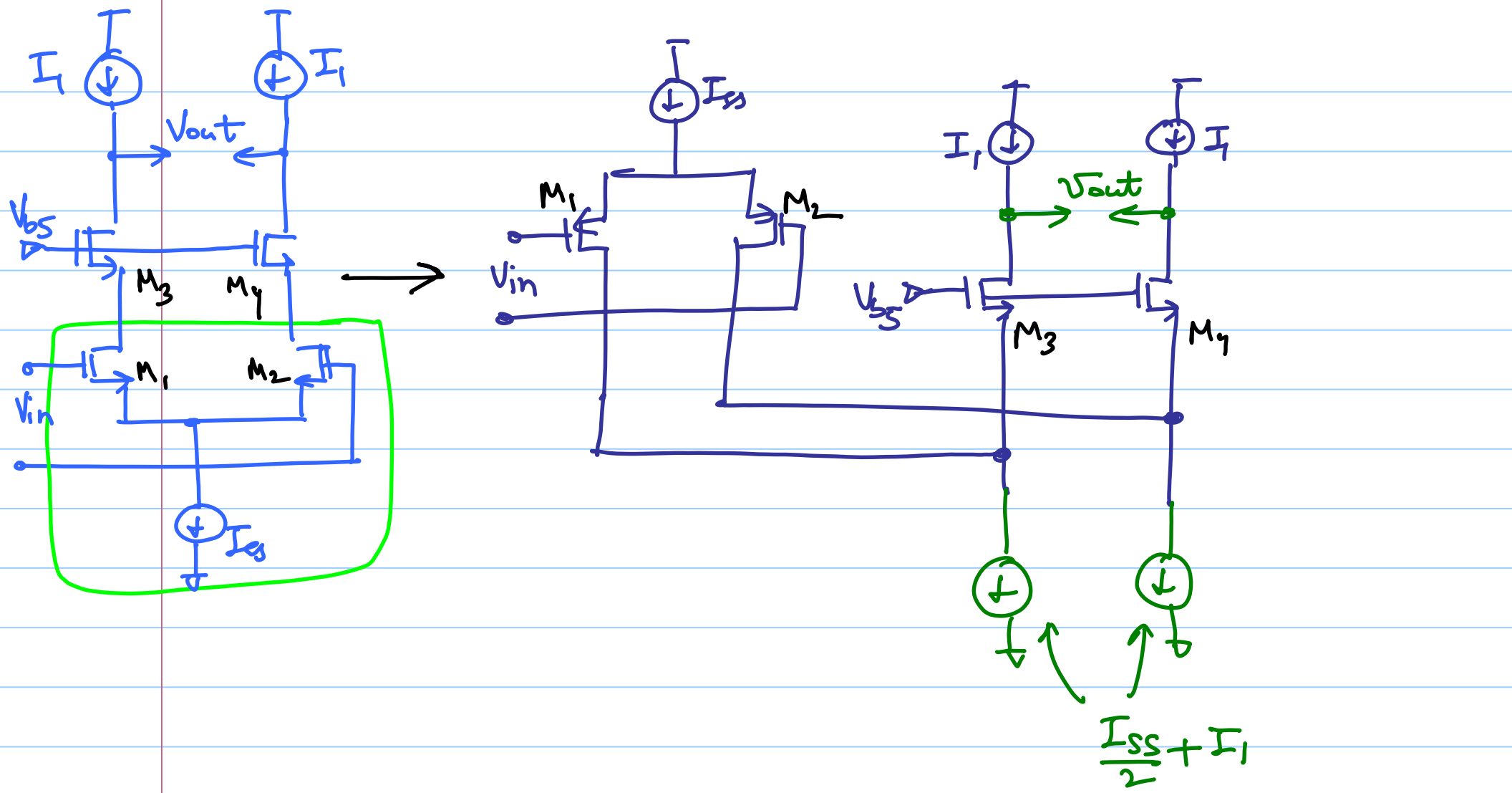
NMOS Cascode



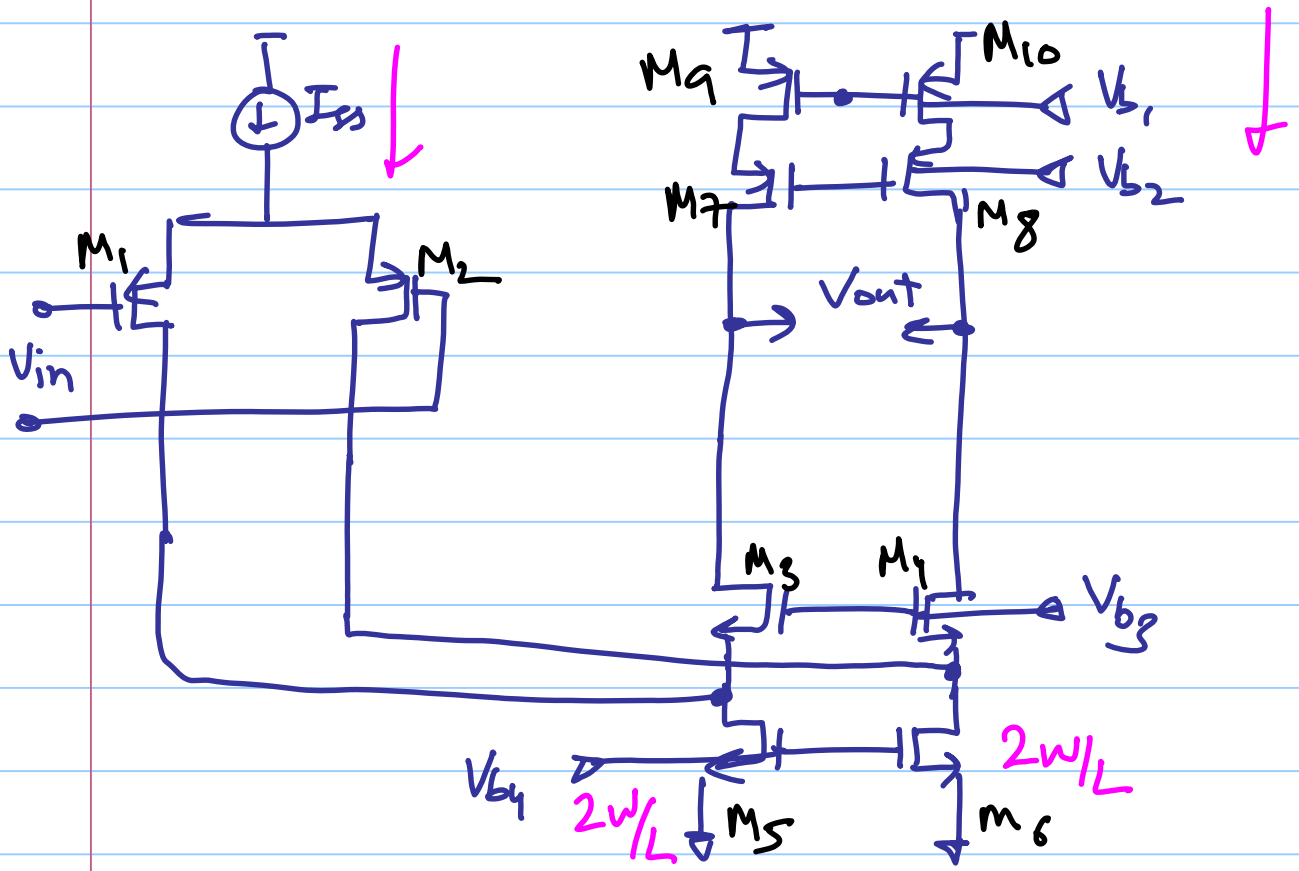
Folded Cascode



$I_2 > I_1$


I_1
I_1
V_{out}
V_{bs}
M_3
M_4
M_1
M_2
V_{in}
I_{ss}
I_{ss}
M_1
M_2
V_{in}
I_1
I_1
V_{out}
V_{bs}
M_3
M_4
$\frac{I_{ss}}{2} + I_1$

fully Differential Folded Cascode Amplifier



Single-ended Folded Cascode