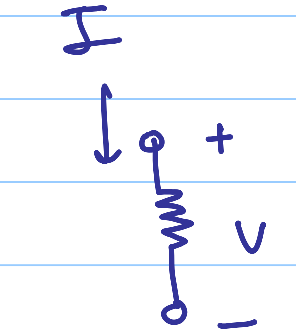
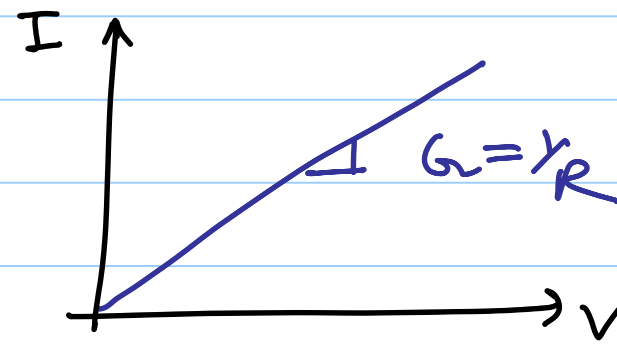
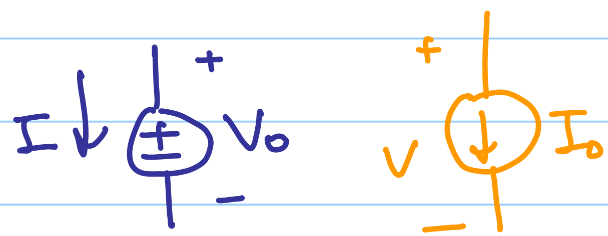
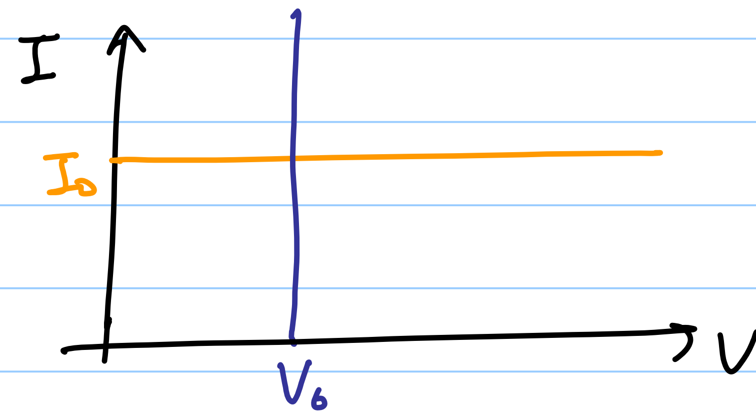
ECE 511 - Lecture 1

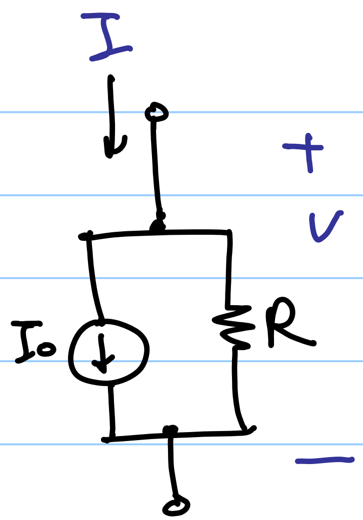
Note Title 1/13/2015





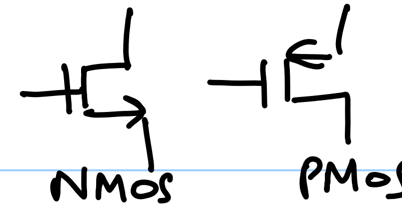


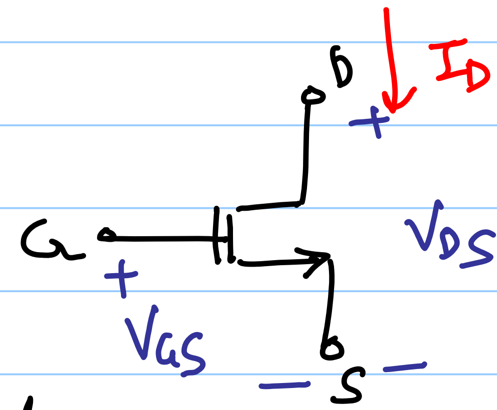


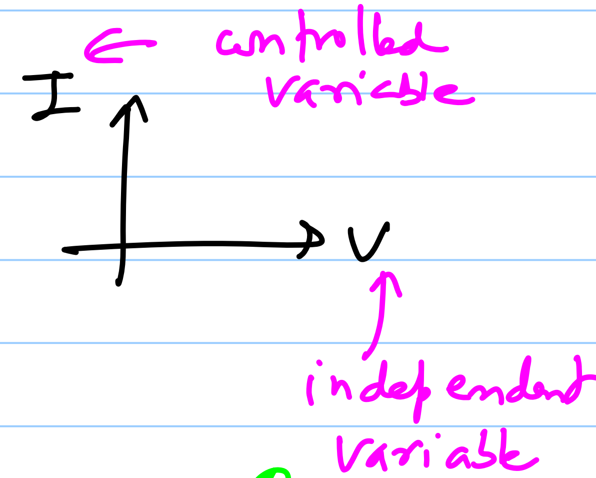


$$I = I_0 + \frac{V}{R}$$

I-V curves for a MOSFET.

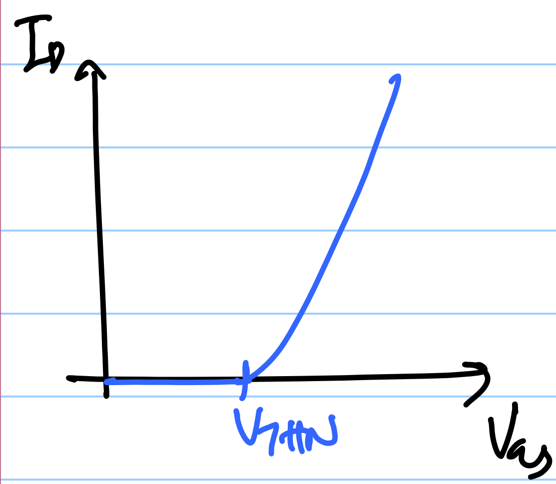


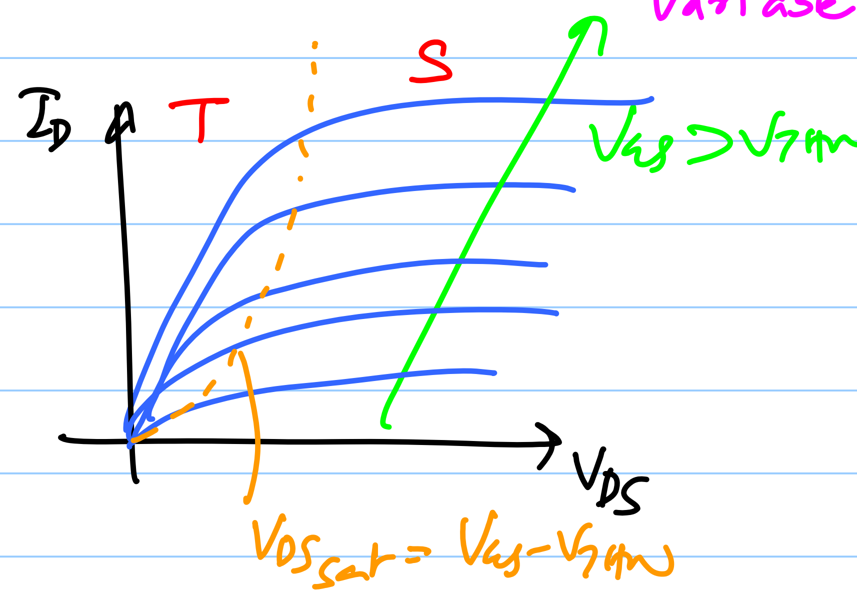




Ignoring body-effect

$$I_D = f(V_{GS}, V_{DS})$$





Long-channel equations

Cutoff: $V_{GS} < V_{THN}$

Triode: $V_{GS} > V_{THN}$ & $V_{DS} < V_{DS,sat} = V_{GS} - V_{THN}$

$$I_D = KP_n \cdot \frac{W}{L}\left[(V_{GS}-V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Sat: $V_{DS} > V_{DS,sat}$

$$I_D = \frac{KP_n}{2}\frac{W}{L}(V_{GS}-V_{THN})^2[1+\lambda V_{DS})$$

channel length modulation

overdrive voltage

$$\underbrace{V_{ov} = V_{GS} - V_{THN}}$$ $\leftarrow$ $V_{DS\,sat}$ only for long channel

$\frac{W}{L} \rightarrow$ aspect ratio $\longrightarrow$ device sizing

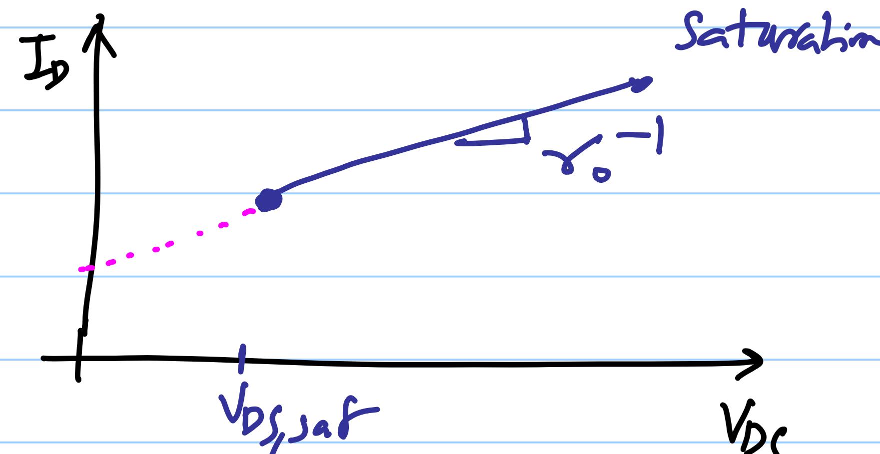
In saturation

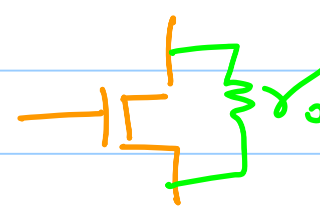
$$I_D = I_{D,sat} + I_{D,sat} \cdot \lambda \left(V_{DS} - V_{DS,sat} \right)$$

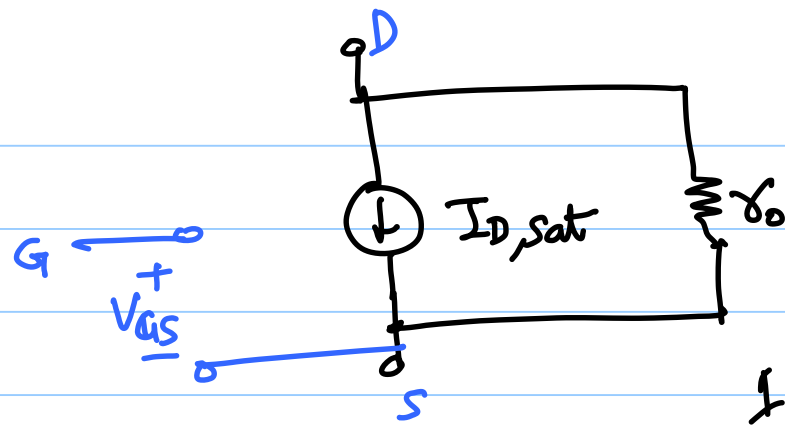
$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1}$$

$$\boxed{r_o = \frac{1}{\lambda \cdot I_{D,sat}}}$$

$$I_{D,sat} = f(V_{GS})$$





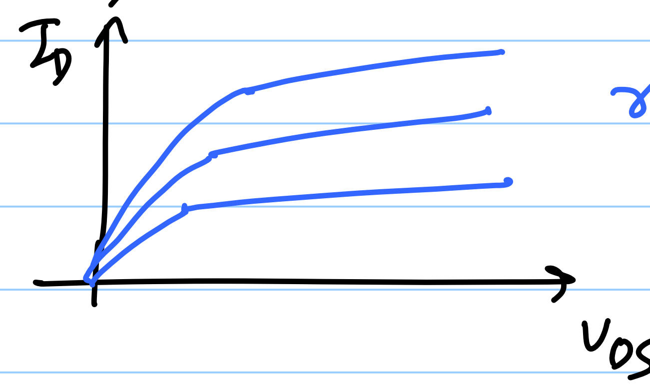


VCCS in parallel with r_o

└→ CLM

$$r_o \propto \frac{1}{\lambda}$$

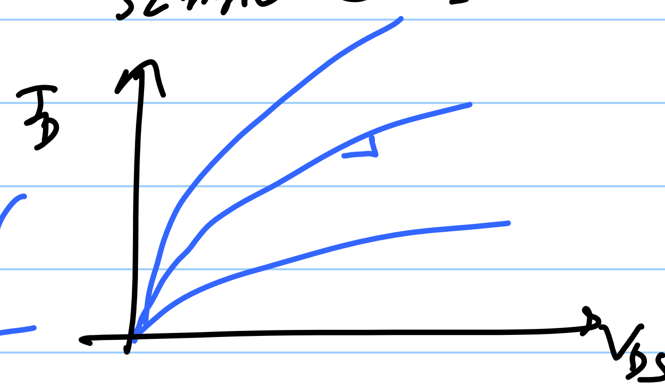
1 µm CMOS



$r_o \to 10\text{ k's}$

32 nm CMOS

r_o gets smaller with scaling



In Triode

$V_{DS} < V_{DS,sat}$

$$I_D = KP_n \frac{W}{L}\left[(V_{GS}-V_{THN})V_{DS} - \cancel{\frac{V_{DS}^2}{2}}\right]$$

$\rightarrow 0$ for $V_{DS} << V_{DS,sat}$

Assume $V_{DS} << V_{DS,sat}$: Deep triode

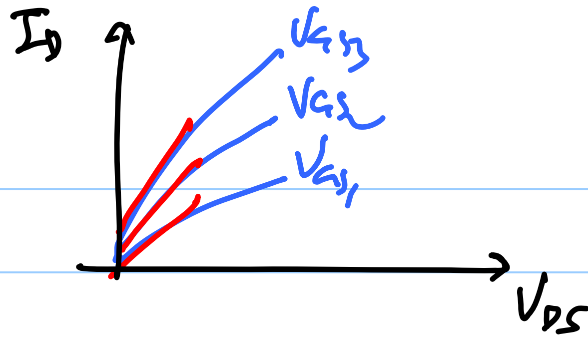
$$I_D \simeq KP_n \frac{W}{L}(V_{GS}-V_{THN})V_{DS}$$

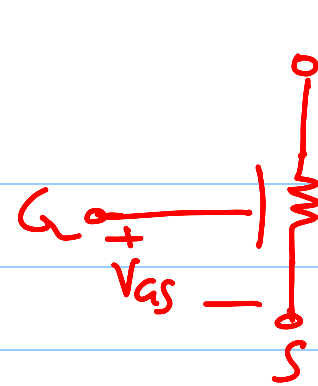
"Linear regim"

$$R_{ch} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \simeq \frac{1}{KP_n \frac{W}{L}(V_{GS}-V_{THN})}$$

$$R_{ch} \propto \frac{1}{V_{GS}-V_{THN}} \Leftarrow$$ ✓

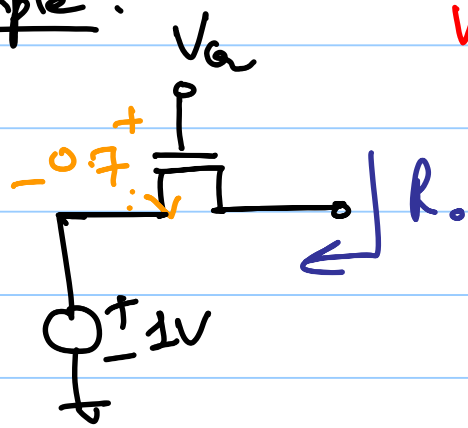
Variable resistance controlled by the gate overdrive





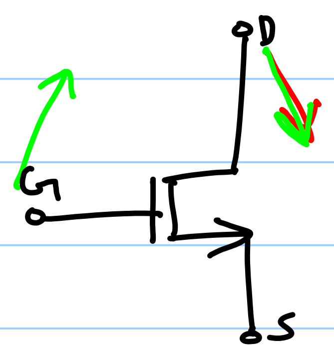
Example:

$V_{THN} = 0.7V$

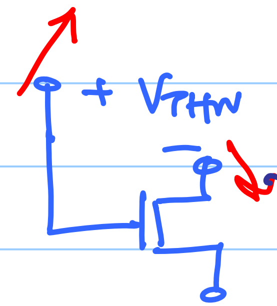


$$R_{ch} = \frac{1}{KP_n \frac{W}{L} (V_{GS} - V_{THN})}$$

$V_{DS} > V_{GS} - V_{THN}$

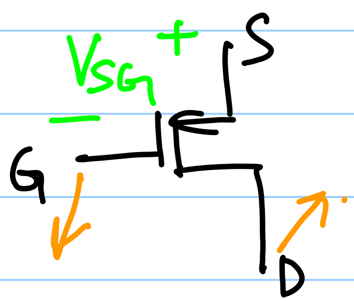


⇒

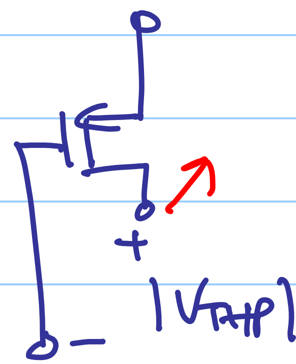


Triode

⇒ the NMOS can have the gate at max V_{THN} higher than the drain before it triodes.



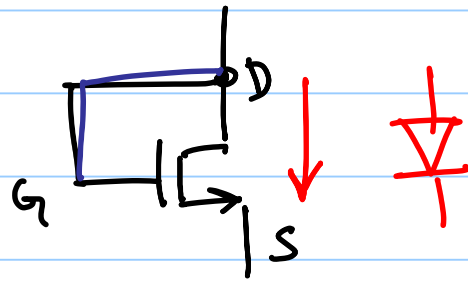
⇒



Triode

the gate can not be lower than the drain by more than $|V_{THP}|$.

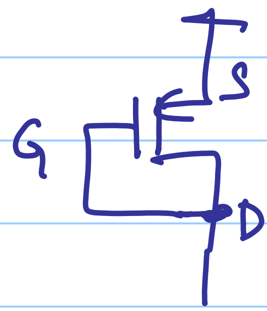
Diode Connection



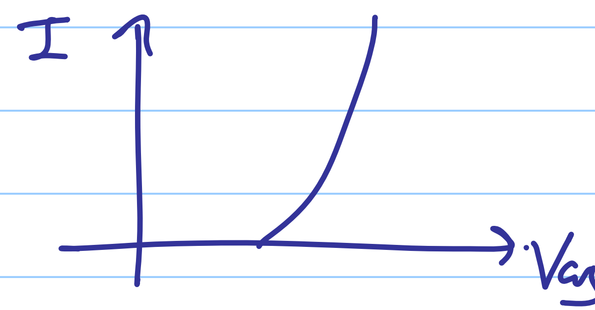
Connect gate & drain

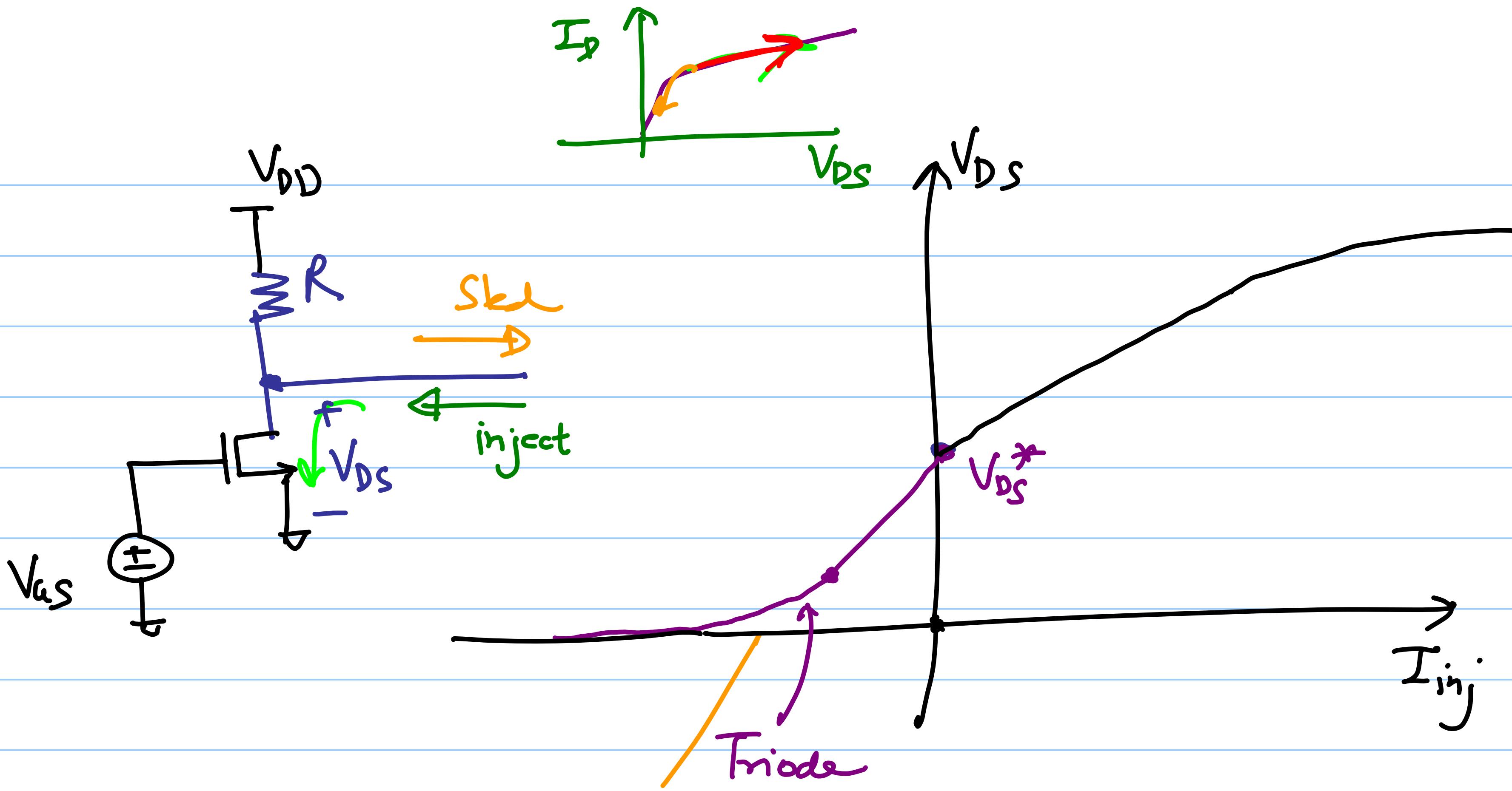
$V_{DS} = V_{GS} > V_{DS,sat}$

$\Rightarrow$ always in saturation for $V_{GS} > V_{THN}$

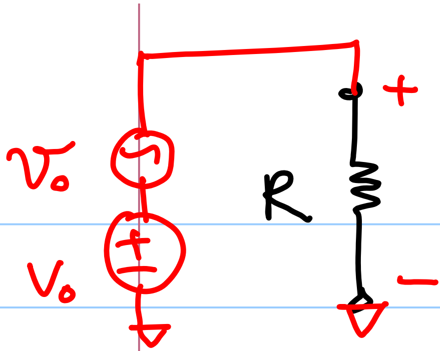


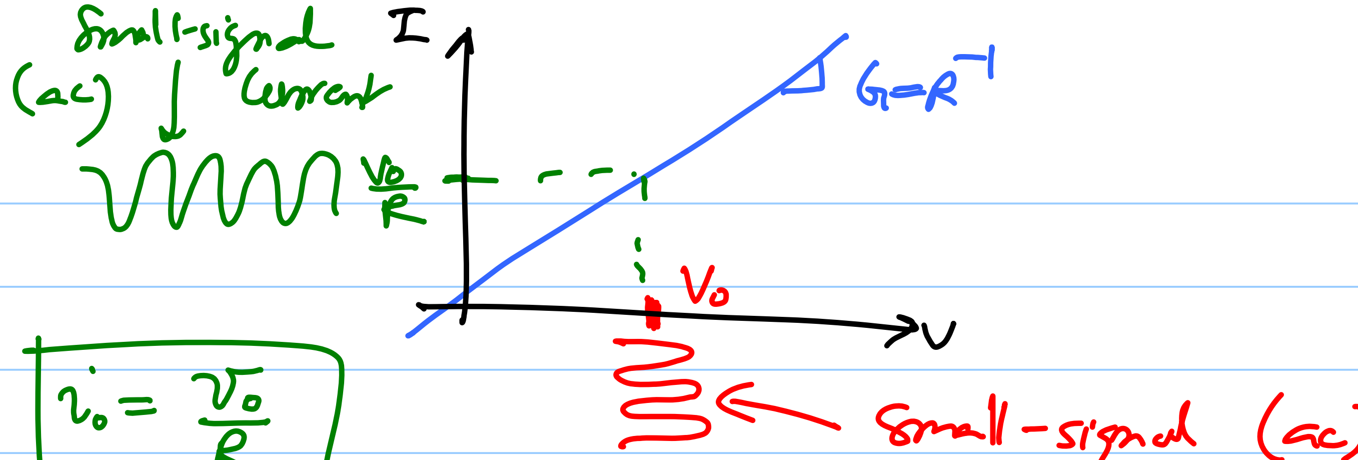
$I_D = f(V_{GS})$





NMOS enters triode and eventually enters cutoff

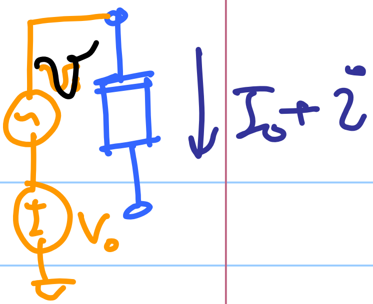


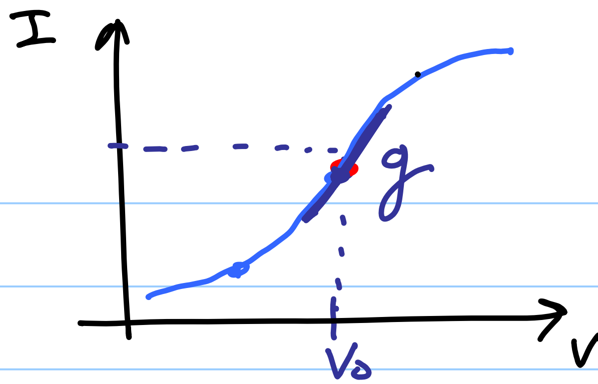


$$\boxed{i_0 = \frac{v_0}{R}}$$

linear device

$$i_0 = G v_0$$





$I = f(V)$ ✓

Bias
Operating
Q-] point

* Need to "bias" it properly
↳ setting the DC operating point for the device (V_0, I_0)

Large-signal characteristic
$I = f(V)$

Taylor Series expansion about the bias point

$$I = \underbrace{f(V_0) + \frac{f'(V_0)}{\lfloor 1}(V - V_0)} + \frac{f''(V_0)}{\lfloor 2}(V - V_0)^2 + \frac{f'''(V_0)}{\lfloor 3}(V - V_0)^3 + \dots$$

$$\underset{DC}{V = V_0} + \underset{AC}{v}$$

AC ← Small-signal

$$I = \underbrace{f(V_o)}_{I_o} + f'(V_o)\cdot \underbrace{v}_{\text{small-signal}} + \frac{f''(V_o)}{\lfloor 2} v^2 + \frac{f'''(V_o)}{\lfloor 3} \cdot v^3 + \cdots$$

$$(I - I_o) = f'(V_o)\cdot v + \ldots \text{ higher order terms}$$

$$i = f'(V_o)\, v + \cdots$$

If v is "very small", then we can ignore higher-order-terms

$$i = f'(V_o)\, v$$

$i = g \cdot v$ where $g = f'(V)\Big|_{V=V_o}$

small-signal parameter depends upon the bias-point small-signal analysis $\Rightarrow$ linearizing the device about the DC bias point